Contents

Rev	Revision History
X1	Initial Draft
X1.1	BOM changes for cost optimisation
X1.2	BOM Reduction for cost and space.
X1.3	Minor updates
X1.4	CPLD Pin Swpping to aid routing
A	Released REV A - BRA085 - ECO33160
B	Released REV B - MP2380/Ethernet Routing cleanup and errata fixes.
B1	Changed P1025 part number and some DNPs so BOM Change only no LAY change

TWR-P1025

Change List

Revisions

Rev	Description	Date	Approved
X1	DRAFT	JUL 15, 11	
X1.1		JUL 25, 11	
X1.2		JUL 27, 11	
X1.3		AUG 01, 11	
X1.4		AUG 10, 11	
A	Released REV A BRA085 - ECO33160	SEP 07, 11	
B		DEC 02, 11	
B1	Changed P1025 part number and some DNPs so BOM Change only no LAY change	DEC 22, 11	

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ICAP Classification: FCP: ___ FIUO: X PUBI: ___

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ecified:
ohms, 5%, 1/8 Watt
uF, 20%, 50V
All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _N Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

```
P1025 SPI CS allocation
-------------------------
CS0 - Elevator SPI0_CS0
CS1 - Elevator SPI0_CS1
CS2 - 1588 DAC
CS3 - Unused

P1025 I2C1 Bus
-------------------------
Address Device

0x50    Boot EEPROM
TBD     Elevator I2C Bus 0

P1025 I2C2 Bus
-------------------------
Address Device

0x1C    Accelerometer
0x23    GPIO Expander
0x52    BRD EEPROM
TBD     Mini PCIe
TBD     Elevator I2C bus 1


P1025 UART0
-------------------------
FDTI - Default


P1025 UART1
-------------------------
Elevator UART
FDTI

P1025 FLASH CS
-------------------------
CS0 - NOR FLASH
CS1 - Elevator CS0
CS2 - Elevator CS1
```

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Drawing Title: **TWR-P1025**

Page Title: **NOTES**

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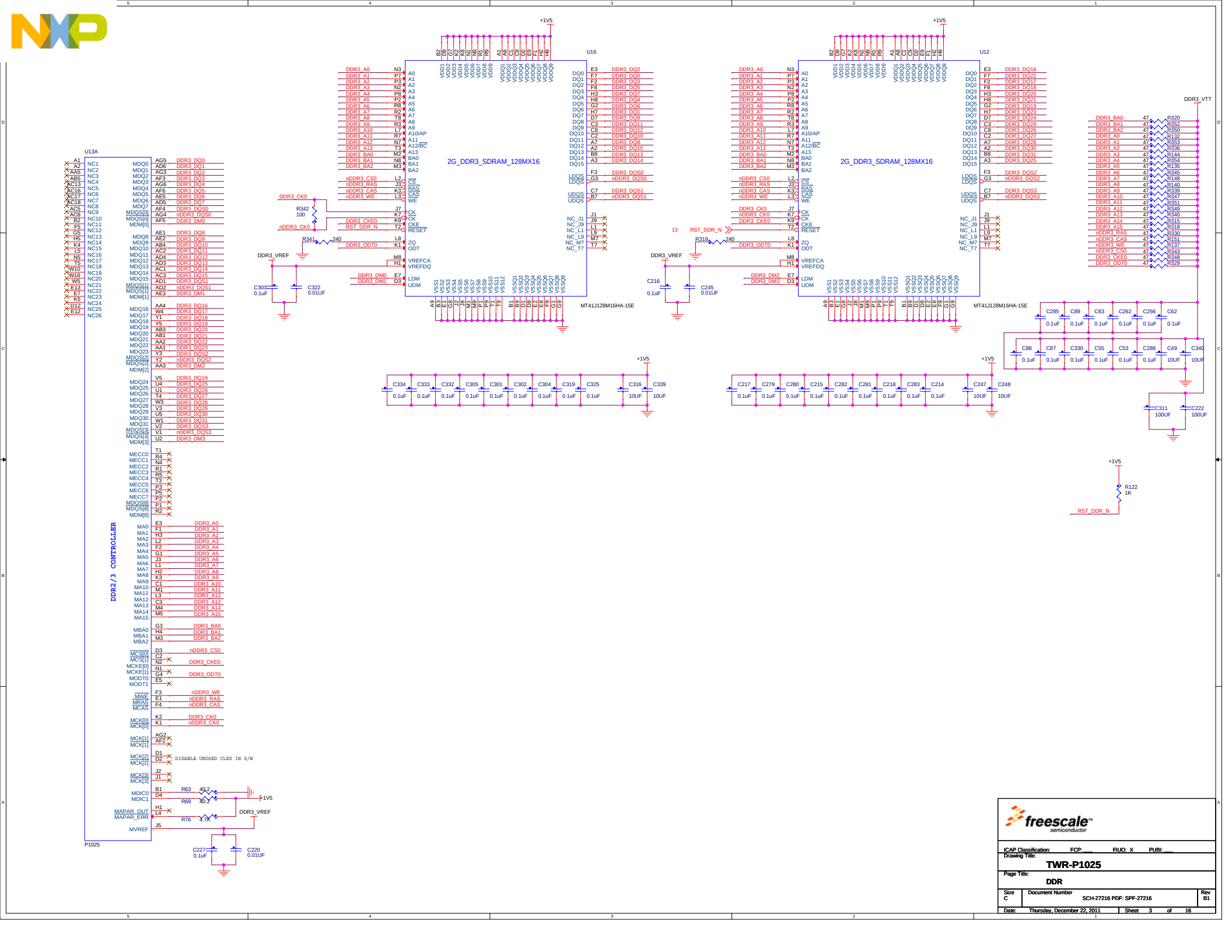
U13A
DDR2/3 CONTROLLER
P1025
DISABLE UNUSED CLKS IN S/W
U16
2G_DDR3_SDRAM_128MX16
MT41J128M16HA-15E
U12
2G_DDR3_SDRAM_128MX16
MT41J128M16HA-15E
+1V5
DDR3_VTT
DDR3_VREF
RST_DDR_N
freescale semiconductor
ICAP Classification:
FCP:
FIUO: X
PUBI:
Drawing Title:
TWR-P1025
Page Title:
DDR
Size C
Document Number
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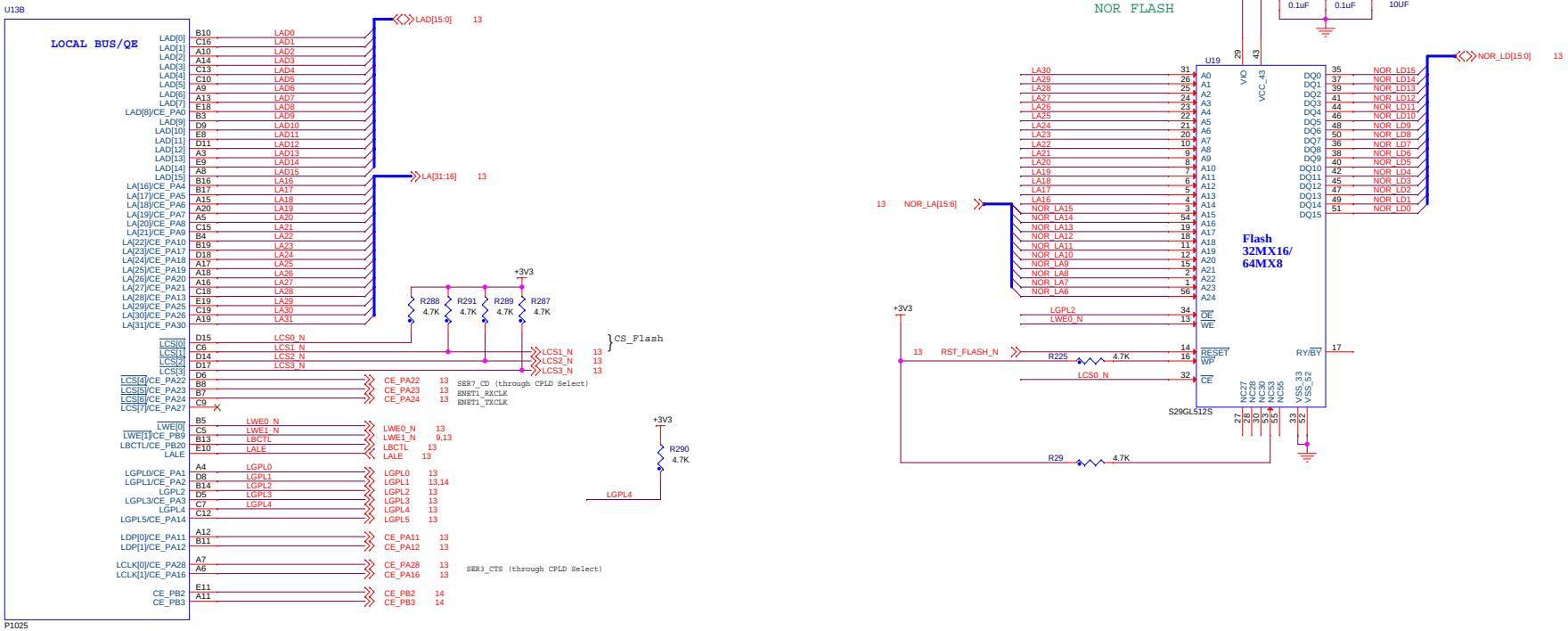

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ICAP Classification: FCP: ___ FIUO: X PUBI: ___

Drawing Title: **TWR-P1025**

Page Title: **Flash**

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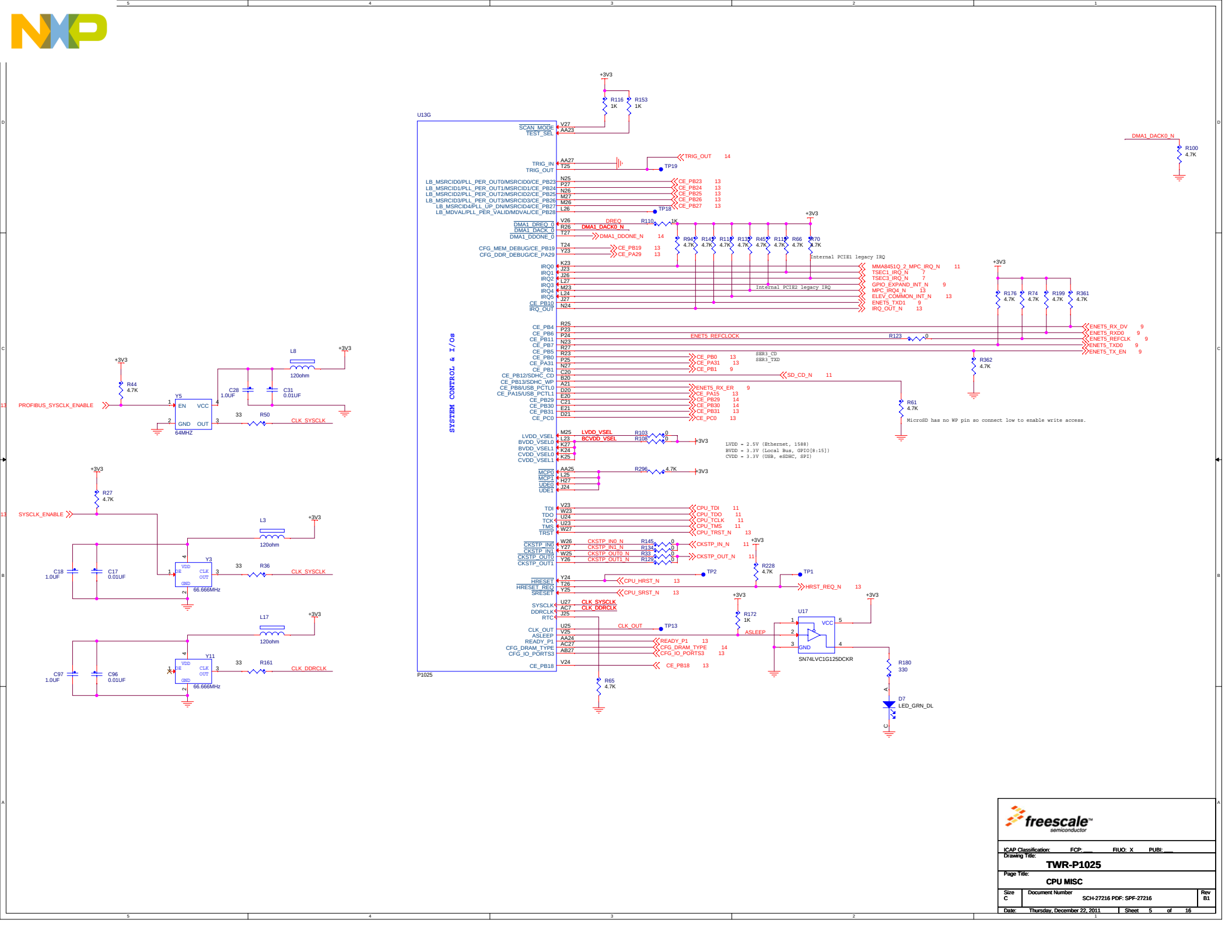

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Drawing Title:	TWR-P1025
Page Title:	CPU MISC
Size: C	Document Number: SCH-27216 PDF: SPF-27216 Rev: B1
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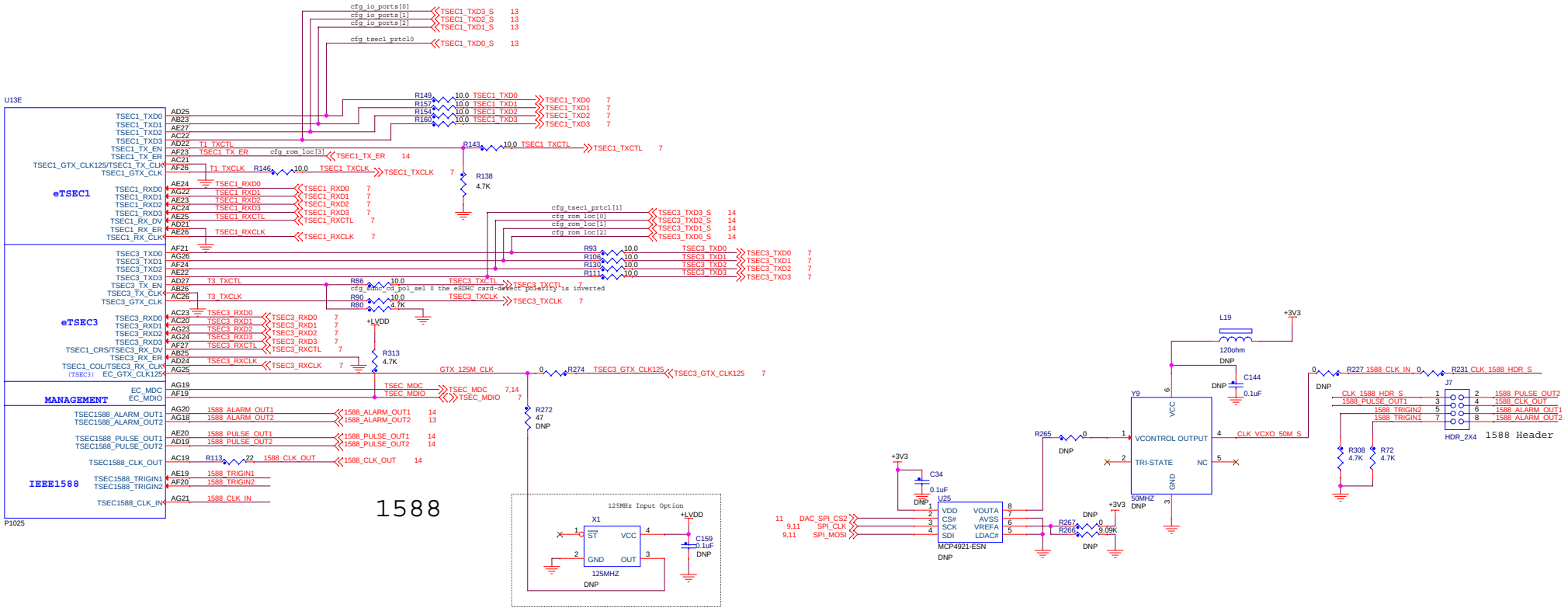

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Drawing Title:	TWR-P1025		
Page Title:	ETHERNET TSEC		
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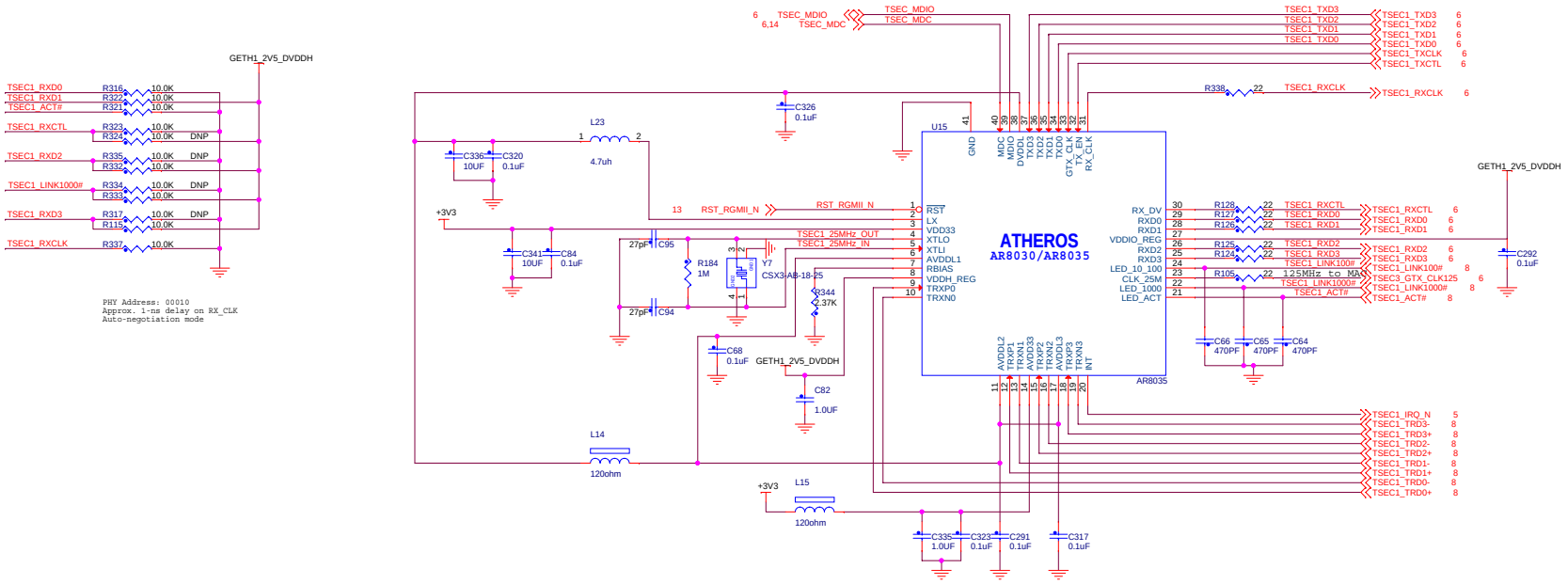
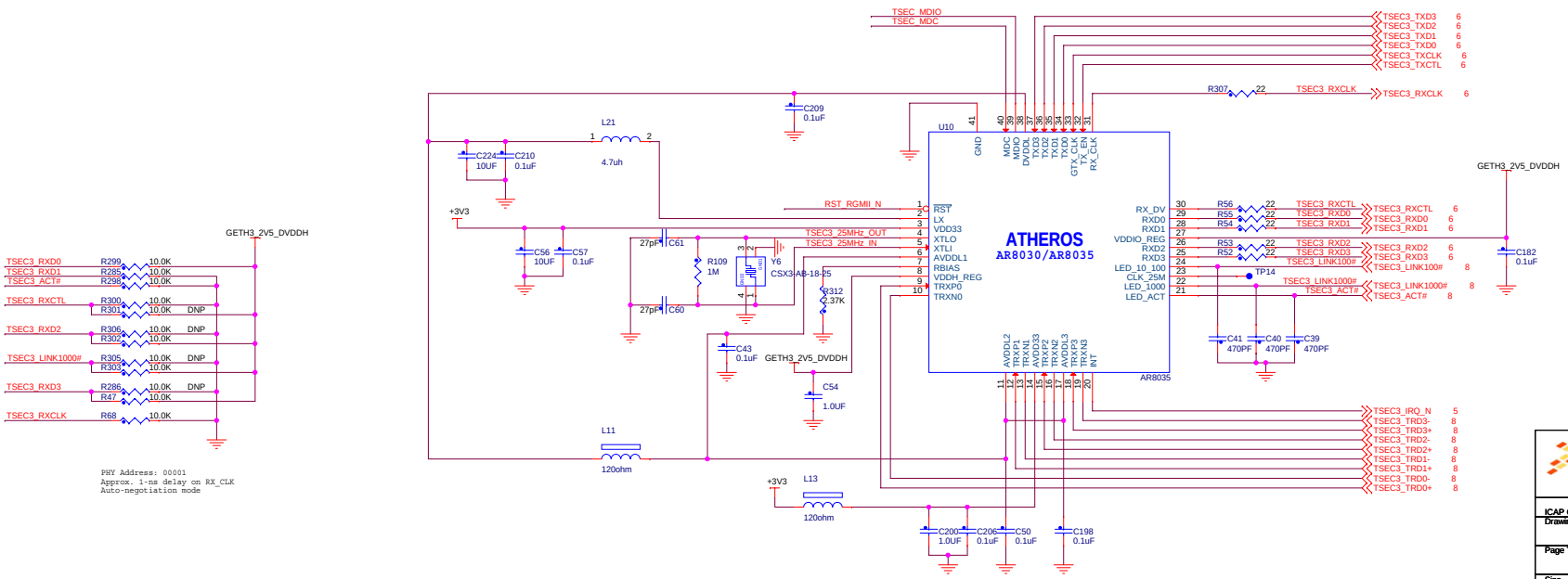
eTSEC1 RGMII PHY



eTSEC3 RGMII PHY



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Drawing Title: **TWR-P1025**

Page Title: **ETHERNET PHY1-3**

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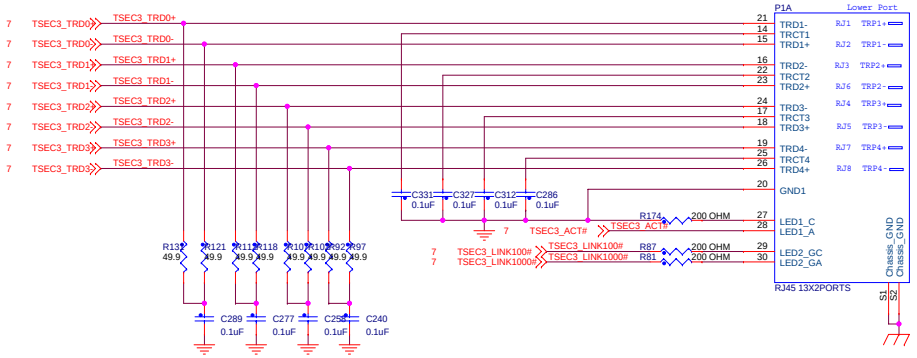
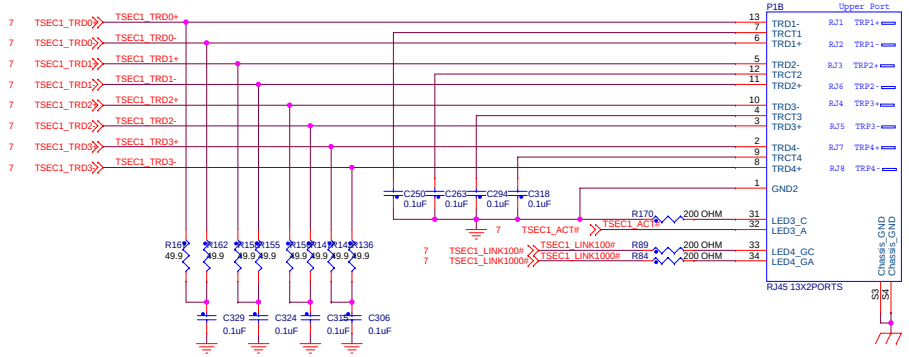
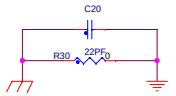
LED active High as bootstrap pins are pulled low.







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ICAP Classification: FCP: ___ FIUO: X PUBI: ___

Drawing Title:

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Page Title:

eTSEC1 & eTSEC3 PORT

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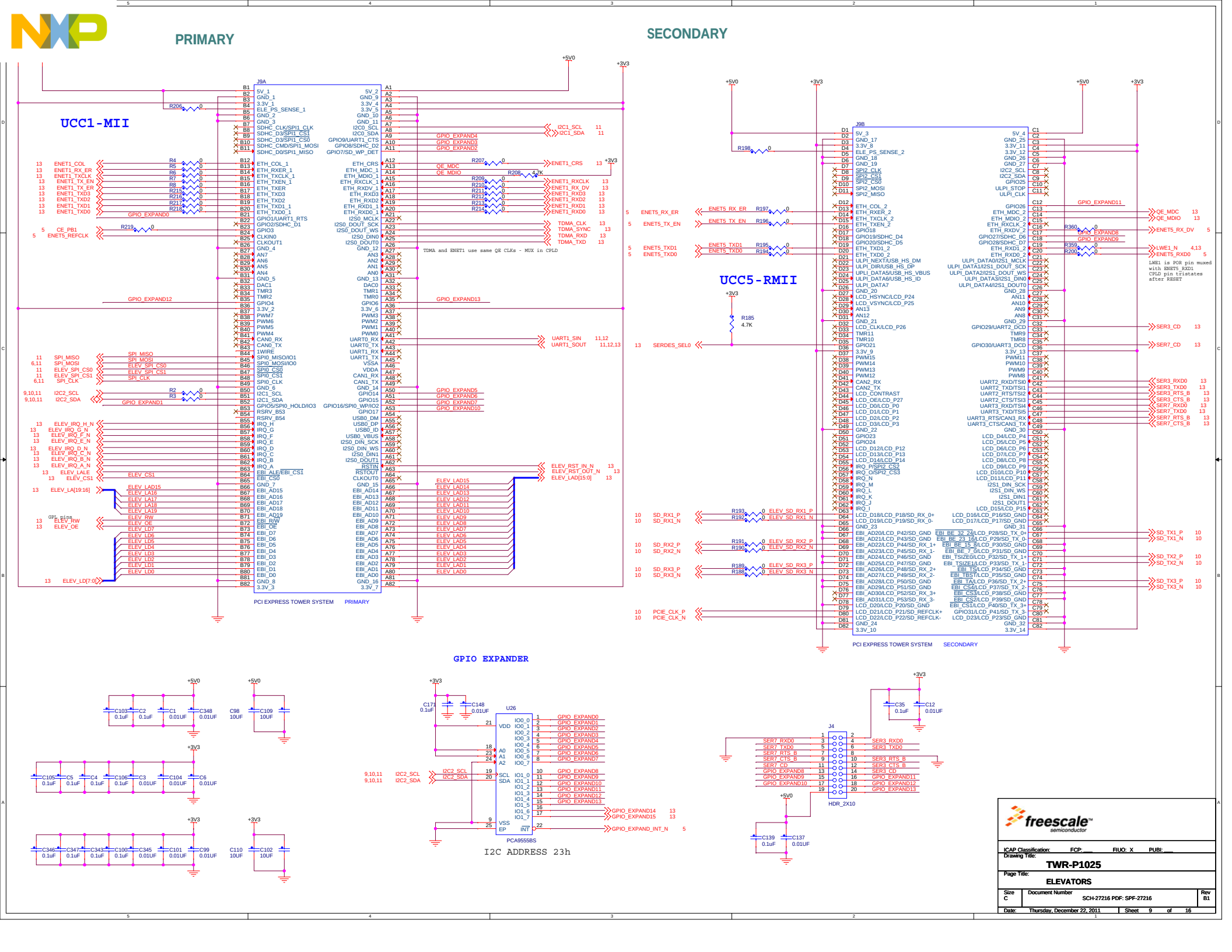
PRIMARY
SECONDARY
UCC1-MII
UCC5-RMII
J9A
J9B
PCI EXPRESS TOWER SYSTEM PRIMARY
PCI EXPRESS TOWER SYSTEM SECONDARY
TDMA and ENET1 use same QE CLKs - MUX in CPLD
LWE1 is POR pin muxed with ENET5_RXD1 CPLD pin tristates after RESET
GPIO EXPANDER
U26
PCA9555BS
I2C ADDRESS 23h
J4
HDR_2X10
freescale semiconductor
ICAP Classification: FCP: ___ FIUO: X PUBI: ___
Drawing Title: TWR-P1025
Page Title: ELEVATORS
Size C
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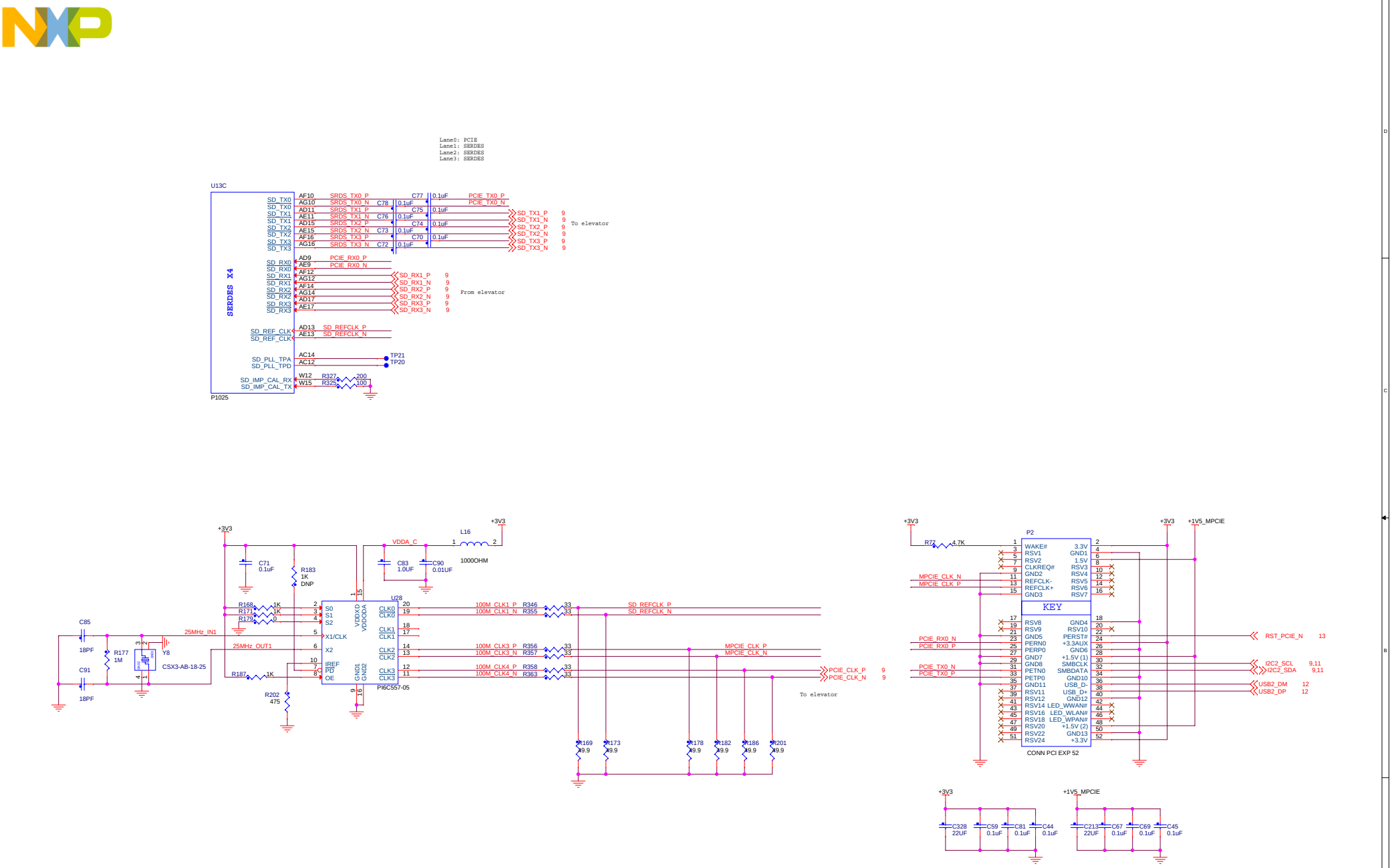

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ICAP Classification: FCP: ___ FIUO: X PUBI: ___

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Page Title: **SERDES**

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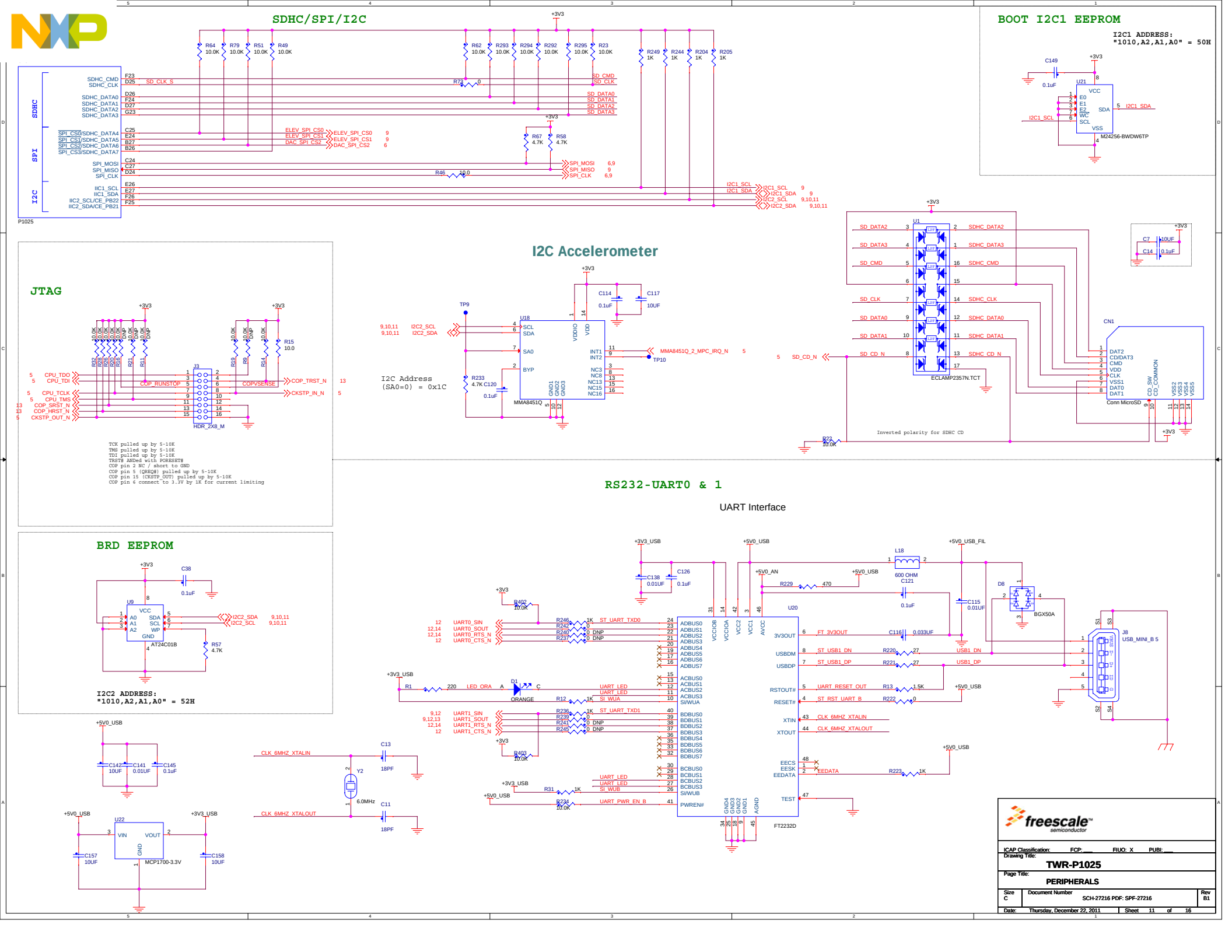
SDHC/SPI/I2C
BOOT I2C1 EEPROM
I2C1 ADDRESS:
"1010,A2,A1,A0" = 50H
M24256-BWDW6TP
I2C Accelerometer
I2C Address
(SA0=0) = 0x1C
MMA8451Q
JTAG
HDR_2X8_M
TCK pulled up by 5-10K
TMS pulled up by 5-10K
TDI pulled up by 5-10K
TRST# ANDed with PORESET#
COP pin 2 NC / short to GND
COP pin 5 (QREQ#) pulled up by 5-10K
COP pin 15 (CKSTP_OUT) pulled up by 5-10K
COP pin 6 connect to 3.3V by 1K for current limiting
ECLAMP2357N.TCT
Conn MicroSD
Inverted polarity for SDHC CD
BRD EEPROM
AT24C01B
I2C2 ADDRESS:
"1010,A2,A1,A0" = 52H
RS232-UART0 & 1
UART Interface
FT2232D
MCP1700-3.3V
USB_MINI_B 5
BGX50A
freescale semiconductor
ICAP Classification:
FCP:
FIUO: X
PUBI:
Drawing Title:
TWR-P1025
Page Title:
PERIPHERALS
Size C
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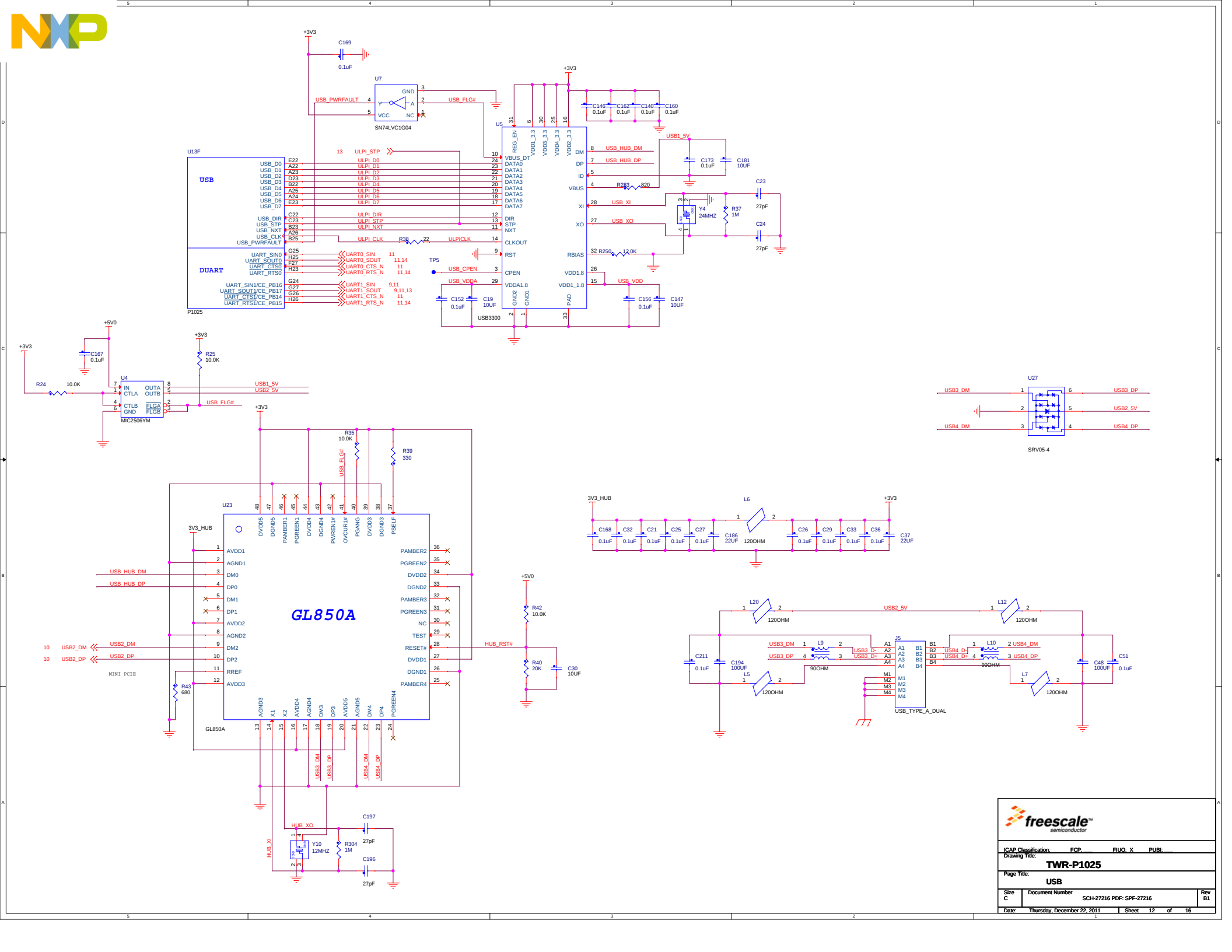

ICAP Classification:	FCP: ___	FIUO: X	PUBI: ___
Drawing Title:	TWR-P1025		
Page Title:	USB		
Size C	Document Number SCH-27216 PDF: SPF-27216		Rev B1
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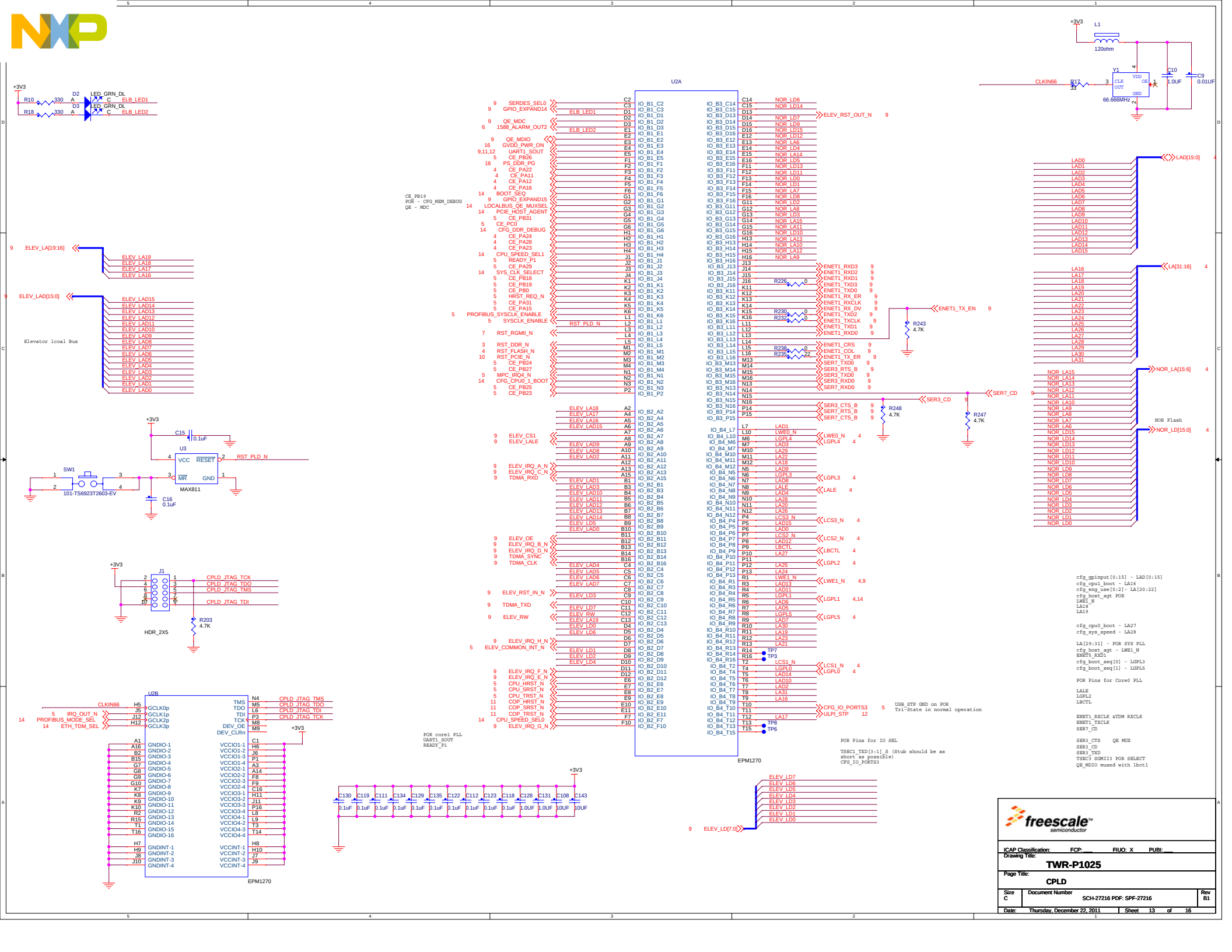
U2A
EPM1270
U2B
EPM1270
Elevator local Bus
ELEV_LA[19:16]
ELEV_LAD[15:0]
LAD[15:0]
LA[31:16]
NOR_LA[15:6]
NOR_LD[15:0]
NOR Flash
ELB_LED1
ELB_LED2
CLKIN66
66.666MHz
ELEV_RST_OUT_N
ENET1_TX_EN
SER7_CD
SER3_CD
CPLD_JTAG_TCK
CPLD_JTAG_TDI
CPLD_JTAG_TDO
CPLD_JTAG_TMS
HDR_2X5
MAX811
101-TS6923T2603-EV
ELEV_RST_IN_N
ELEV_COMMON_INT_N
TDMA_TXD
TDMA_SYNC
TDMA_CLK
ELEV_RW
ELEV_OE
ELEV_CS1
ELEV_LALE
ELEV_IRQ_A_N
ELEV_IRQ_B_N
ELEV_IRQ_C_N
ELEV_IRQ_D_N
ELEV_IRQ_E_N
ELEV_IRQ_F_N
ELEV_IRQ_G_N
ELEV_IRQ_H_N
CPU_HRST_N
CPU_SRST_N
CPU_TRST_N
COP_HRST_N
COP_SRST_N
COP_TRST_N
CPU_SPEED_SEL0
RST_PLD_N
RST_RGMII_N
RST_DDR_N
RST_FLASH_N
RST_PCIE_N
MPC_IRQ4_N
CFG_CPU0_1_BOOT
PROFIBUS_SYSCLK_ENABLE
SYSCLK_ENABLE
SERDES_SEL0
GPIO_EXPAND14
QE_MDC
1588_ALARM_OUT2
QE_MDIO
GVDD_PWR_ON
UART1_SOUT
PCIE_HOST_AGENT
LOCALBUS_QE_MUXSEL
GPIO_EXPAND15
BOOT_SEQ
CPU_SPEED_SEL1
CFG_DDR_DEBUG
PS_DDR_PG
CE_PA22
CE_PA11
CE_PA12
CE_PA16
CE_PB26
CE_PB31
CE_PC0
CE_PA24
CE_PA28
CE_PA23
CE_PA29
CE_PB18
CE_PB19
CE_PB0
CE_PA31
CE_PA15
CE_PB24
CE_PA27
CE_PB25
CE_PB23
READY_P1
IRQ_OUT_N
PROFIBUS_MODE_SEL
ETH_TDM_SEL
CLKIN66
POR core1 PLL
UART1_SOUT
READY_P1
POR Pins for IO SEL
TSEC1_TXD[3:1] S (Stub should be as short as possible)
CFG_IO_PORTS3
USB_STP GND on POR
Tri-State in normal operation
cfg_gpinput[0:15] - LAD[0:15]
cfg_cpu1_boot - LA16
cfg_eng_use[0:2] - LA[20:22]
cfg_host_agt POR
LWE1_N
LA18
LA19
cfg_cpu0_boot - LA27
cfg_sys_speed - LA28
LA[29:31] - POR SYS PLL
cfg_host_agt - LWE1_N
ENET5_RXD1
cfg_boot_seq[0] - LGPL3
cfg_boot_seq[1] - LGPL5
POR Pins for Core0 PLL
LALE
LGPL2
LBCTL
RNET1_RXCLK &TDM RXCLK
RNET1_TXCLK
SER7_CD
SER3_CTS QE MUX
SER3_CD
SER3_TXD
TSEC3_SOMI3 POR SELECT
QE_MDIO muxed with lbctl
freescale semiconductor
ICAP Classification: FCP: ___ FIUO: X PUBI: ___
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Page Title:
CPLD
Size C
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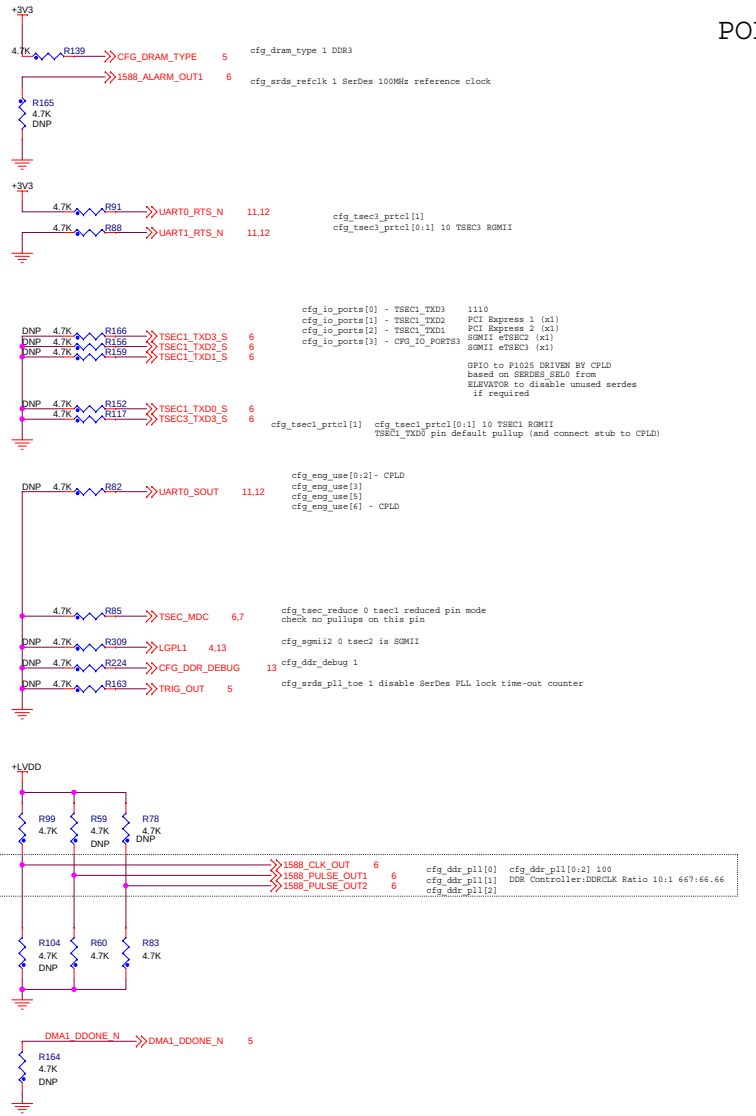
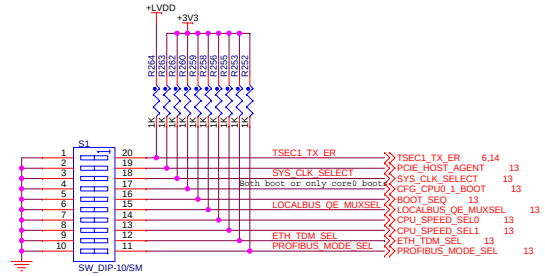
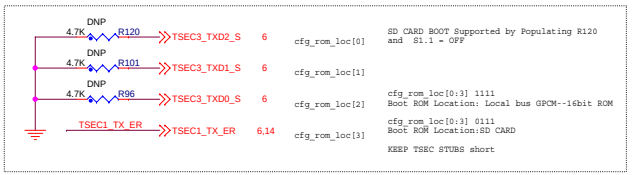
POR Configuration Options








```
        CPLD CONTROLLED POR

cfg_sys_pll[0] - LA29   cfg_sys_pll[0:2]          Options via CPU_SPEED_SEL
cfg_sys_pll[1] - LA30   CCB Clock: SYSCLK Ratio   Core      QE
cfg_sys_pll[2] - LA31                             500       333 (SYS CLK - 66.667MHz)
                                                  533       266 (SYS CLK - 66.667MHz)
cfg_core0_pll[0] - LBCTL  cfg_core0_pll[0:2]      400       400 (SYS CLK - 66.667MHz)
cfg_core0_pll[1] - LALE   e500 Core:CCB ClockRatio 384      384 (SYS CLK - 64MHz)
cfg_core0_pll[2] - LGPL2

cfg_core1_pll[0] - LWE0_N   cfg_core1_pll[0:2]
cfg_core1_pll[1] - UART1_SOUT e500 Core:CCB ClockRatio
cfg_core1_pll[2] - READY_P1

cfg_host_agt[0] - LWE1_N  cfg_host_agt[0:2] 111 -P1020 acts as the host
cfg_host_agt[1] - LA18    for all PCI Express interfaces
cfg_host_agt[2] - LA19    cfg_host_agt[0:2] 000 -P1020 acts as an agent
                          for all PCI Express interfaces

                          Controlled by PCIE_HOST_AGENT SWITCH (SW1.2)

cfg_cpu0_boot - LA27    DRIVEN BY CPLD based on CFG_CPU[1:0]_BOOT
cfg_cpu1_boot - LA16    SWITCHED (SW1.4 and SW1.5)

cfg_boot_seq[0] - LGPL3 cfg_boot_seq[0:1] 11
cfg_boot_seq[1] - LGPL5 Boot sequencer is disabled.
                        No I2C ROM is accessed.

                        01 - Normal I2C addressing
                        DRIVEN BY CPLD based on BOOT_SEQ SWITCH (SW1.6)

cfg_sgmii3 - TSEC_1588_ALARM_OUT_2
1 - tsec3 is not SGMII (default In CPLD
0- SGMII lane 3 (Note only available if SERDES Tower Card indicates it
can support SGMII on SERDES lane 3 thorugh SERDES_SEL lines. CPLD
controls this)
cfg_eng_use[0:2]- LA[20:22]
cfg_ddr_debug 1 - CE_PA29
cfg_mem_debug 1 - CE_PB19
cfg_gpinput[0:15] - LAD[0:15]

cfg_sys_speed - LA28
1 SYSCLK is at or above 66MHz

cfg_plat_speed - LA23
1 Platform Clock is at or above 300MHz

cfg_core0_speed - LA24
1 Core0 Clock is at or above 500MHz

cfg_core1_speed - LA25
1 Core0 Clock is at or above 500MHz

cfg_ddr_speed - LA26
DDR DATA rate is at or above 500Mbps

cfg_elbc_ecc  - MSRCID0
1 eLBC ECC checking is enabled

cfg_eng_use[5] - MSRCID5
cfg_eng_use[6] - MSRCID4
```

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ICAP Classification: FCP: ___ FIUO: X PUBI: ___

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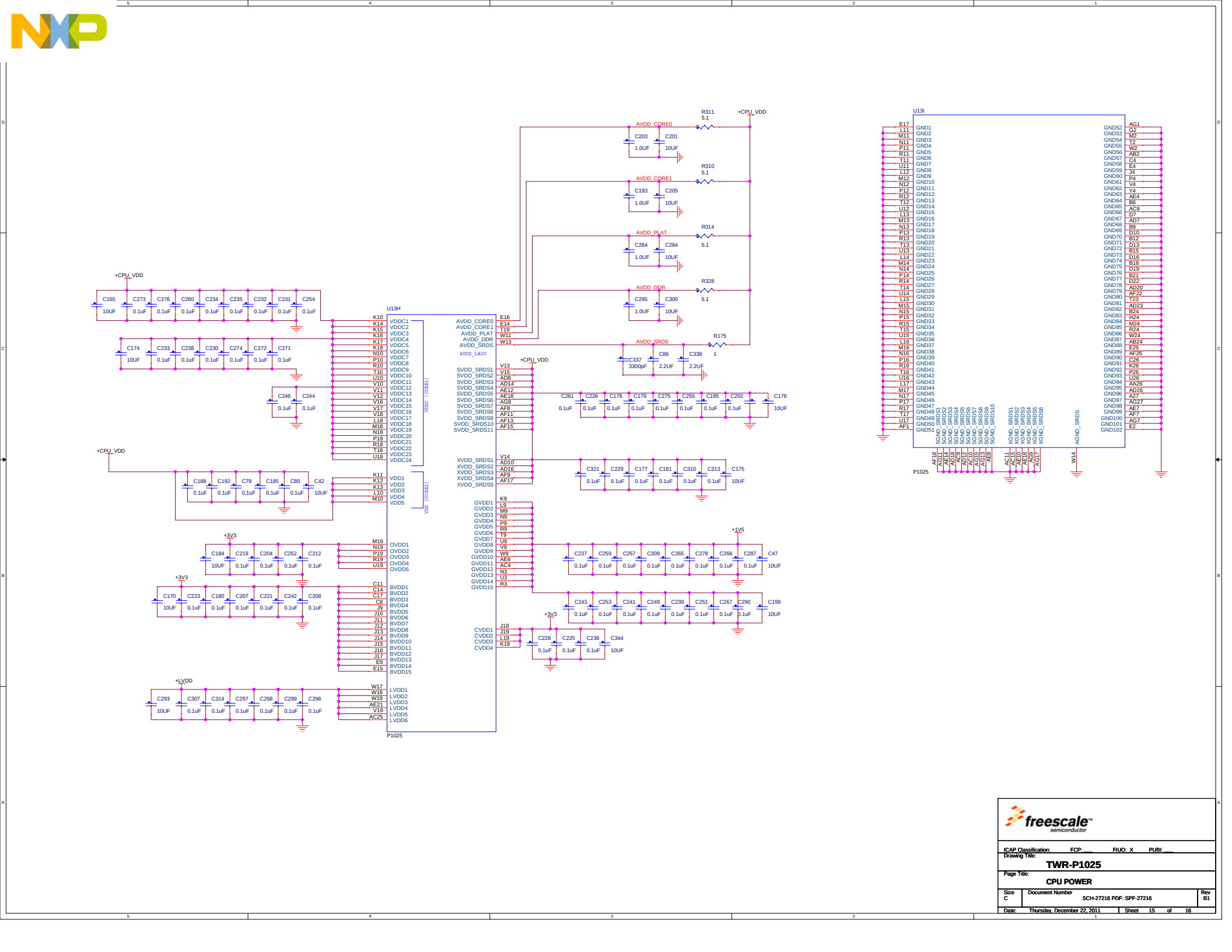
U13H
P1025
+CPU_VDD
+3V3
+1V5
+LVDD
AVDD_CORE0
AVDD_CORE1
AVDD_PLAT
AVDD_DDR
AVDD_SRDS
R311
R310
R314
R328
R175
U13I
P1025
freescale semiconductor
ICAP Classification:
FCP:
FIUO: X
PUBI:
Drawing Title:
TWR-P1025
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CPU POWER
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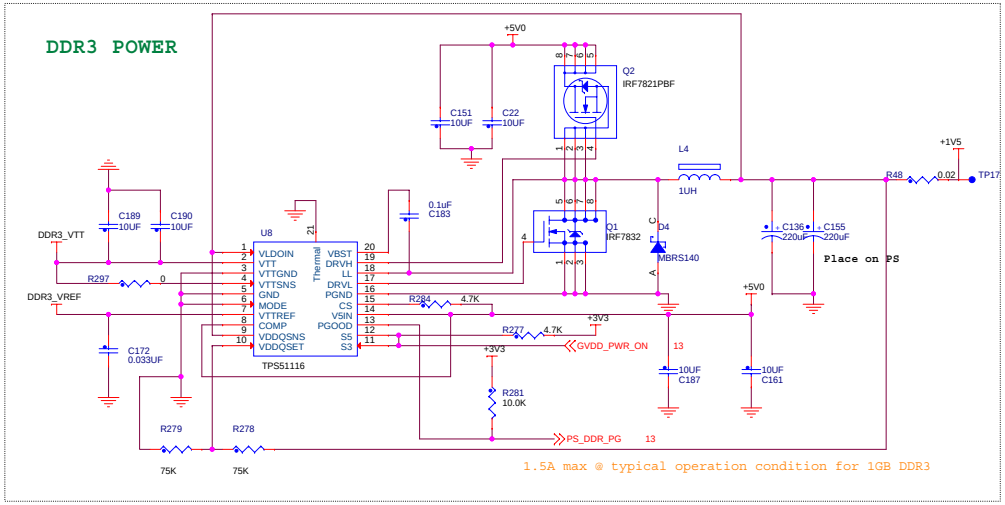
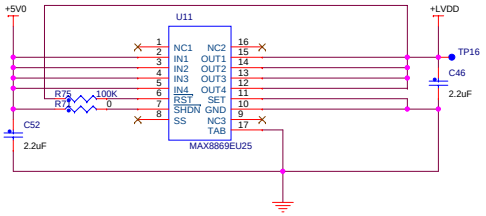
DDR3 POWER

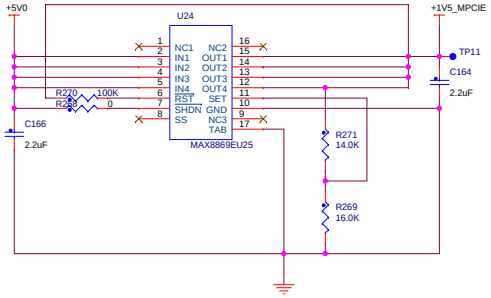


2.5V: ETHERNET PHY

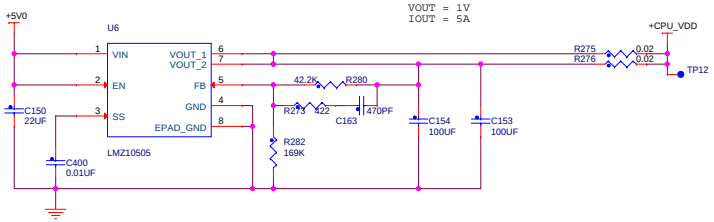


1A max @ typical operation condition

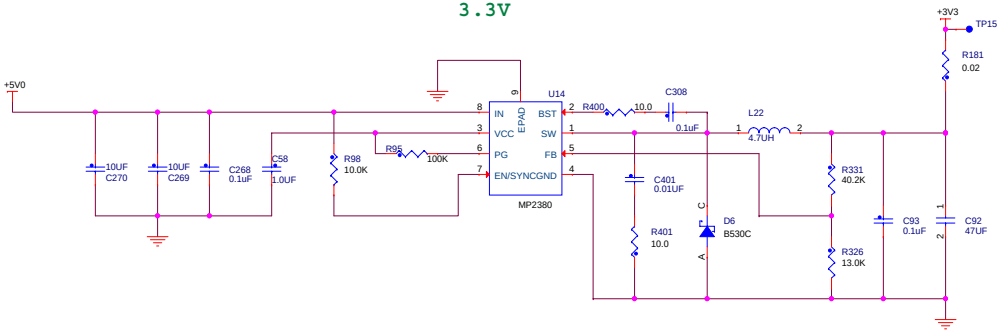
1.5V: MINI PCI-E

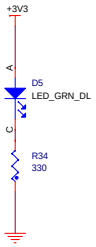


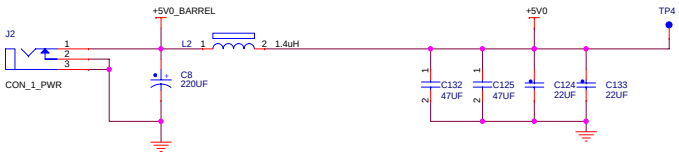
CPU VDD POWER



3.3V







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ICAP Classification: FCP: ___ FIUO: X PUBI: ___

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