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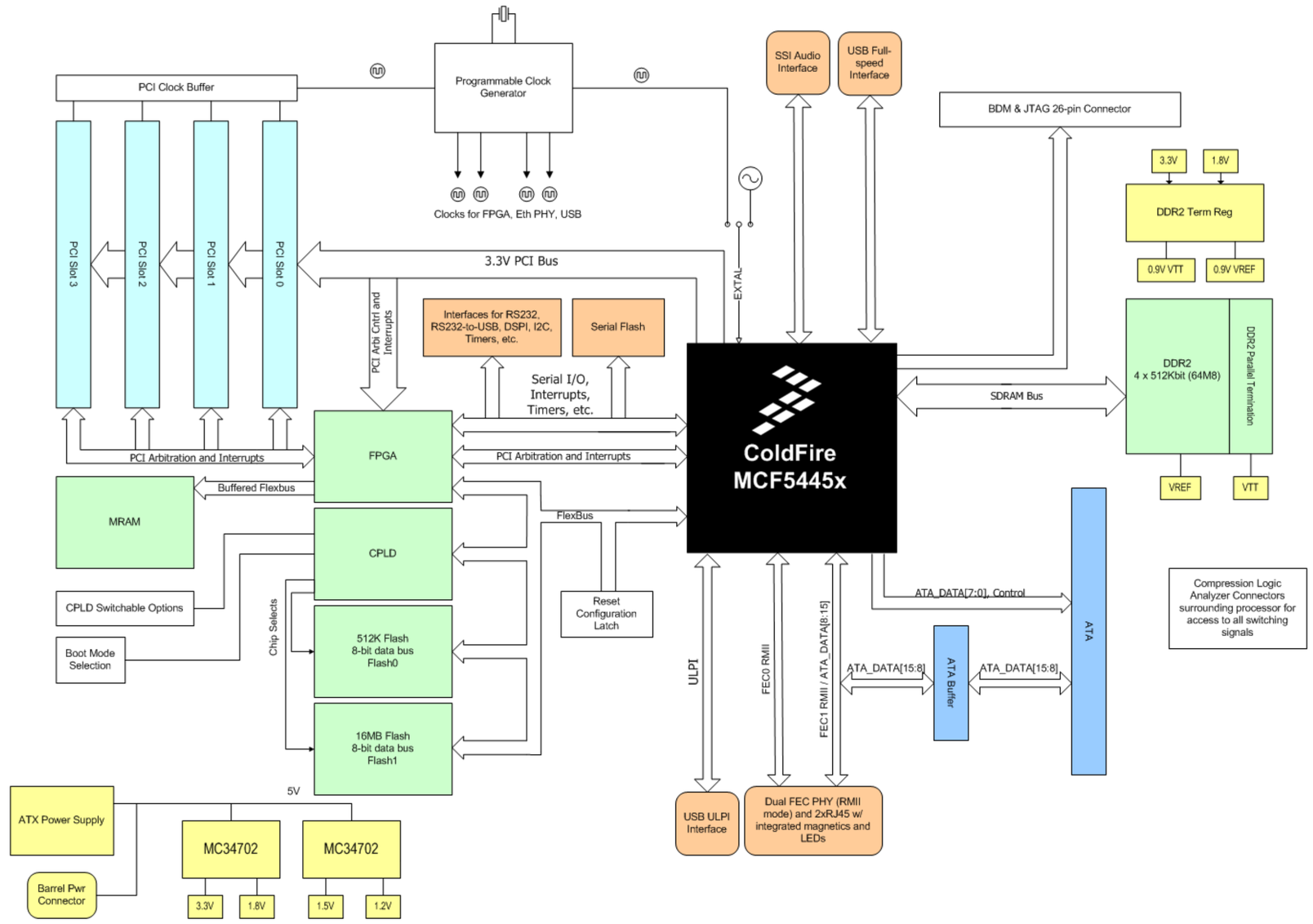
Revisions

Rev	Description	Date	Approved
X1	Original Draft	11/08/06	J.W.
X2	Fixed Flash1, serial port interfaces, etc.	07/03/07	M.N.



freescale semiconductor

Transportation & Standard Products Group
6501 William Cannon Drive West
Austin, TX 78735-8598

Designer: M.Norman & J.Smith	Drawing Title: **M54455EVB**		
Drawn by: DEVTECH CAD - RO	Page Title: **TITLE PAGE**		
Approved: JOHN WEIL	Size C	Document Number PDF: SPF-22131 SOURCE: SCH-22131	Rev C
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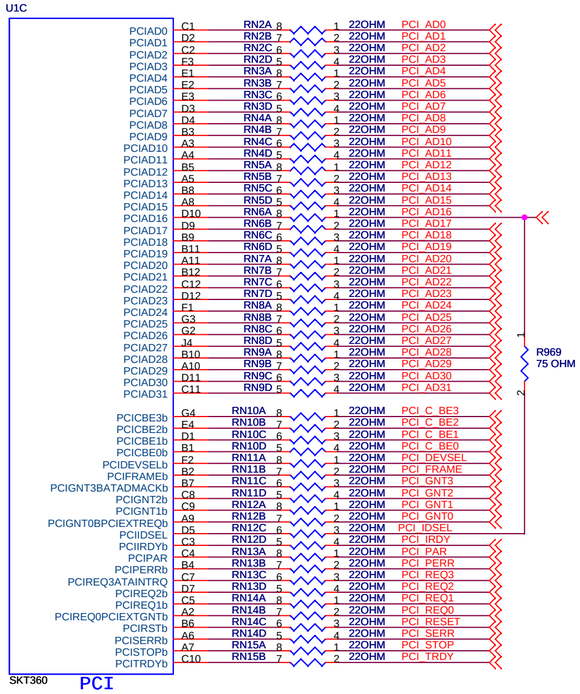
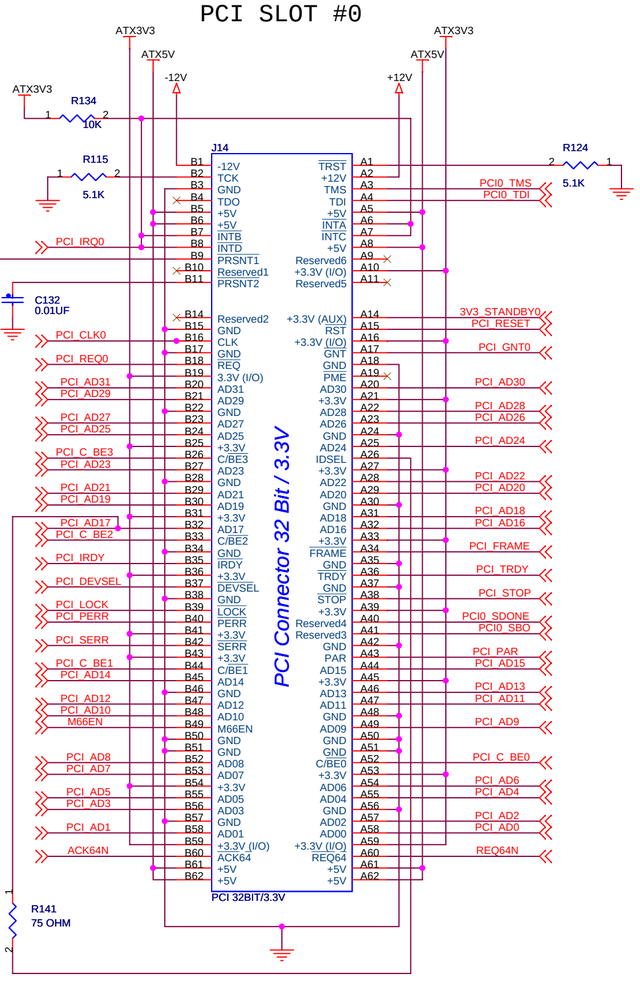
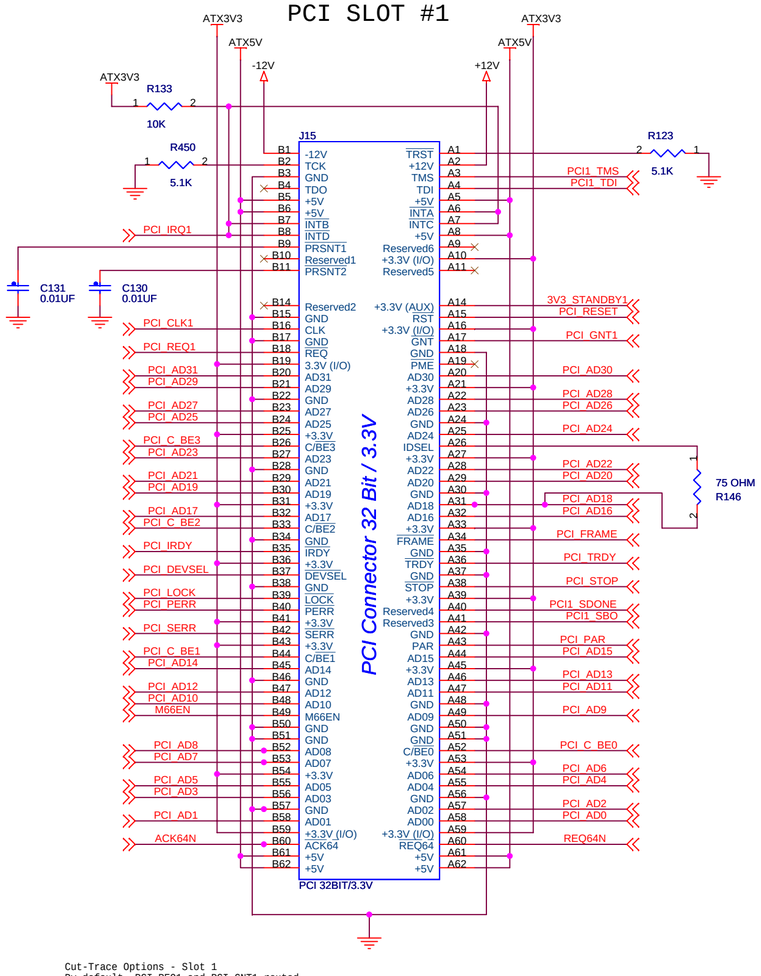
PCI SLOT #0



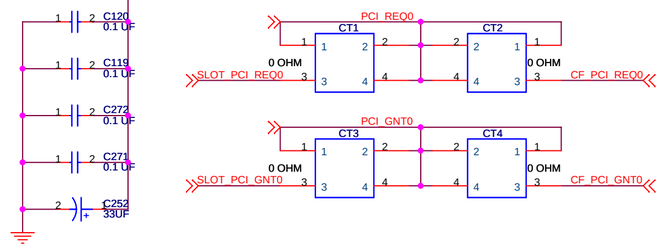
Cut-Trace Options - Slot 0
By default, PCI_REQ0 and PCI_GNT0 routed directly to PCI Slot 0.
To route through FPGA, cut trace between 1 and 2 on CT1 and solder 1 to 3. Then, cut trace between 1 and 2 on CT2 and solder 1 to 3. Repeat this process for CT3 and CT4.

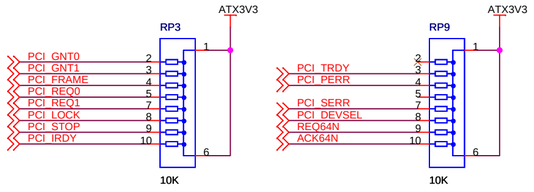


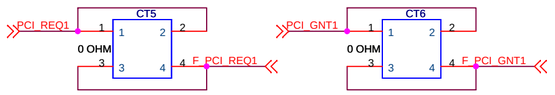
PCI SLOT #1

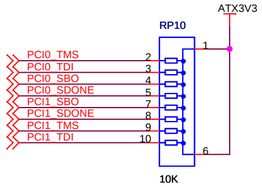


Cut-Trace Options - Slot 1
By default, PCI_REQ1 and PCI_GNT1 routed directly to PCI Slot 1 from U1.
To route through FPGA, cut trace between 1 and 2 on CT5 and solder 1 to 3. Then, cut trace between 1 and 2 on CT6 and solder 1 to 3.

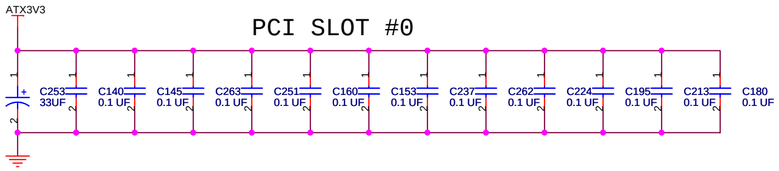




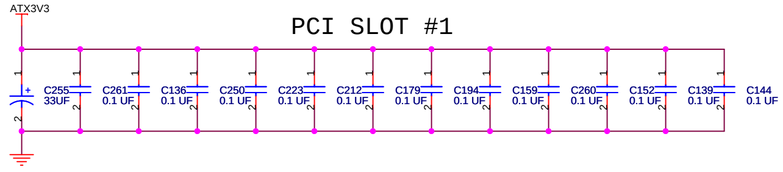


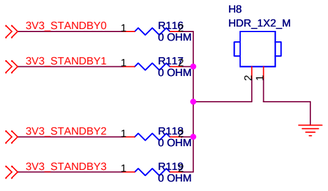


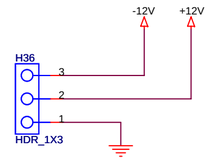
PCI SLOT #0



PCI SLOT #1



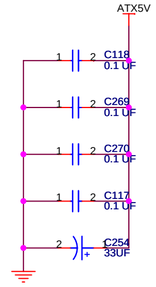




The ATX power supply provides +/- 12V power to the connectors. This header can be used to monitor the supply.

PCI Notes:

1. CF_PCI_GNTn and CF_PCI_REQn signals connect to the FPGA. PCI_GNTn and PCI_REQn signals are connected from the FPGA to the PCI slots.
2. PCI Slot #0 uses PCI_REQ0 and PCI_GNT0
   PCI Slot #1 uses PCI_REQ1 and PCI_GNT1
   PCI Slot #2 uses PCI_REQ2 and PCI_GNT2
   PCI Slot #3 uses PCI_REQ3 and PCI_GNT3
3. MCF5445x IDSEL connected to PCI_AD16
   PCI Slot #0 IDSEL connected to PCI_AD17
   PCI Slot #1 IDSEL connected to PCI_AD18
   PCI Slot #2 IDSEL connected to PCI_AD19
   PCI Slot #3 IDSEL connected to PCI_AD20
4. The FPGA gathers interrupts from the PCI slots.
5. JTAG is unusable on PCI connectors



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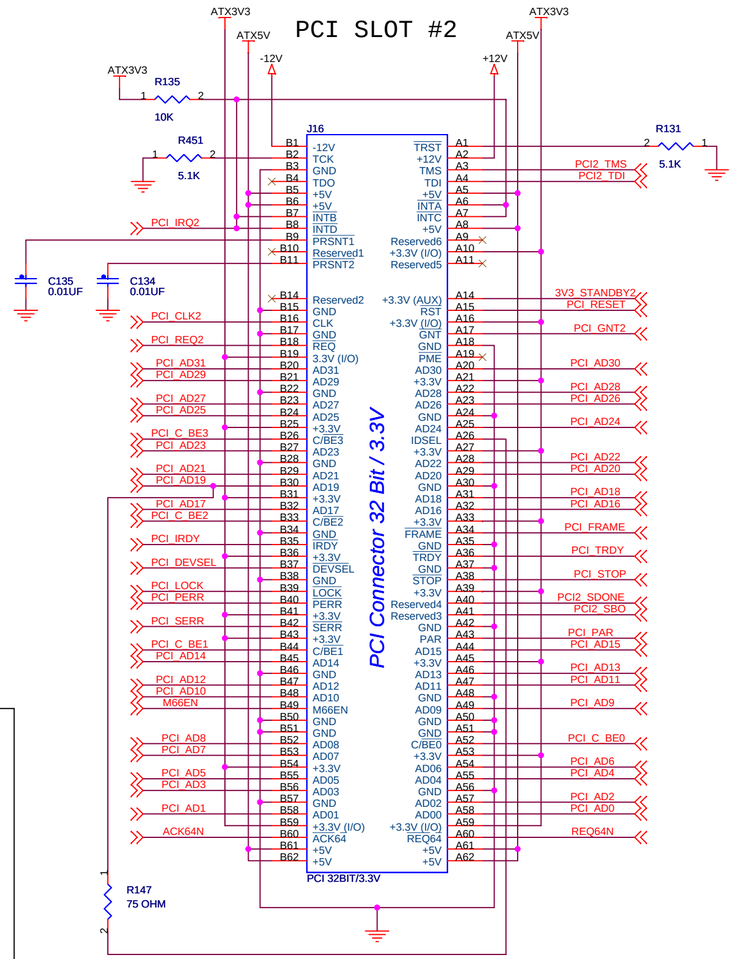
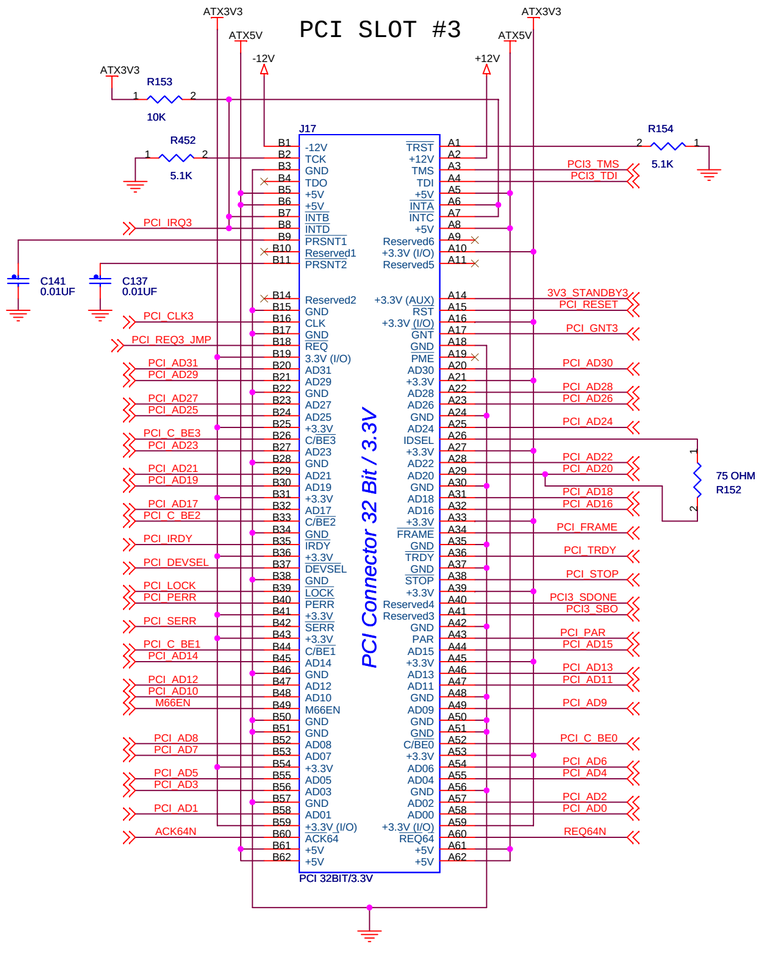




PCI Notes:

1. CF_PCI_GNTn and CF_PCI_REQn signals connect to the FPGA. PCI_GNTn and PCI_REQn signals are connected from the FPGA to the PCI slots.

2. PCI Slot #0 uses PCI_REQ0 and PCI_GNT0
   PCI Slot #1 uses PCI_REQ1 and PCI_GNT1
   PCI Slot #2 uses PCI_REQ2 and PCI_GNT2
   PCI Slot #3 uses PCI_REQ3 and PCI_GNT3

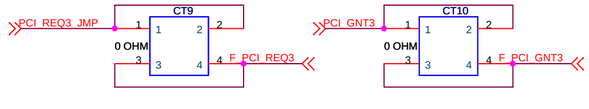
3. MCF5445x IDSEL connected to PCI_AD16
   PCI Slot #0 IDSEL connected to PCI_AD17
   PCI Slot #1 IDSEL connected to PCI_AD18
   PCI Slot #2 IDSEL connected to PCI_AD19
   PCI Slot #3 IDSEL connected to PCI_AD20

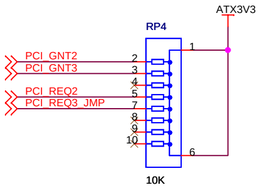
4. The FPGA gathers interrupts from the PCI slots.

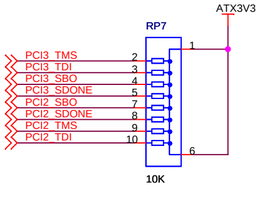
5. JTAG is unusable on PCI connectors

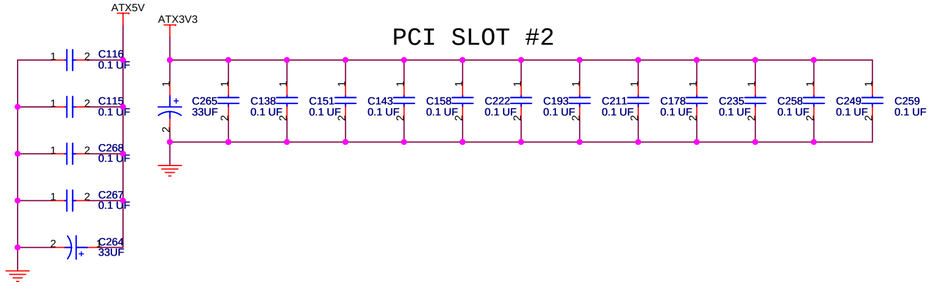
Cut-Trace Options - Slot 2
By default, PCI_REQ2 and PCI_GNT2 routed directly to PCI Slot 2 from U1.
To route through FPGA, cut trace between 1 and 2 on CT7 and solder 1 to 3. Then, cut trace between 1 and 2 on CT8 and solder 1 to 3.

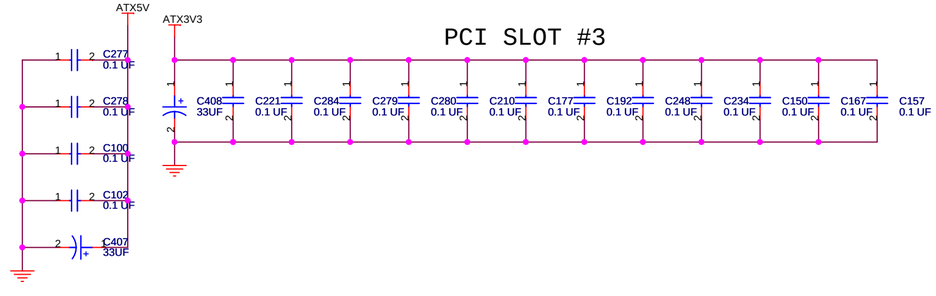
Cut-Trace Options - Slot 3
By default, PCI_REQ3 and PCI_GNT3 routed directly to PCI Slot 3 from U1.
To route through FPGA, cut trace between 1 and 2 on CT9 and solder 1 to 3. Then, cut trace between 1 and 2 on CT10 and solder 1 to 3.











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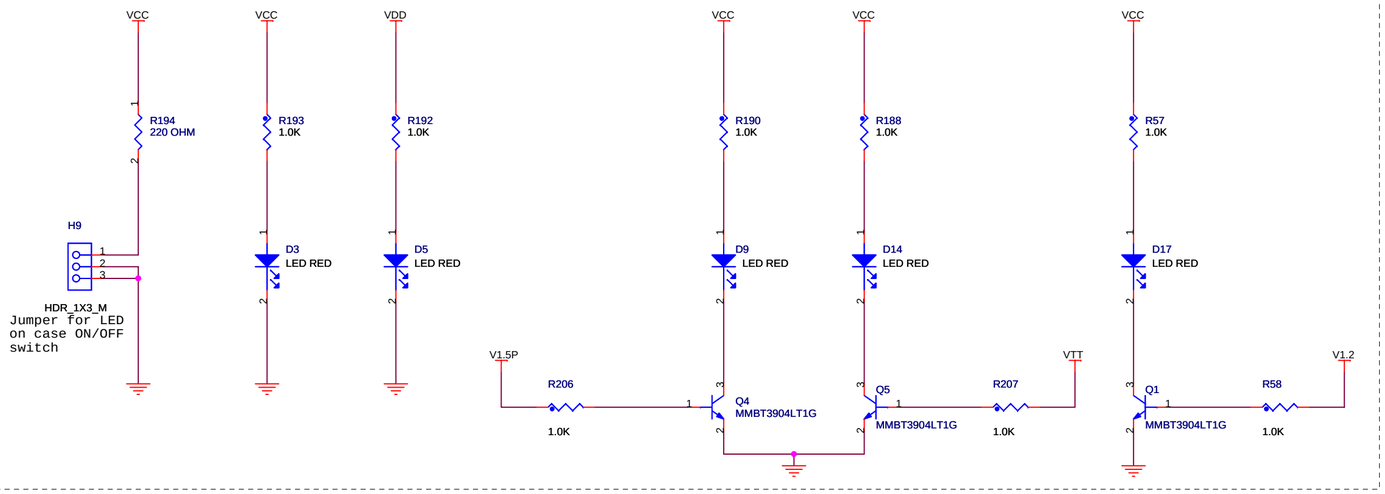
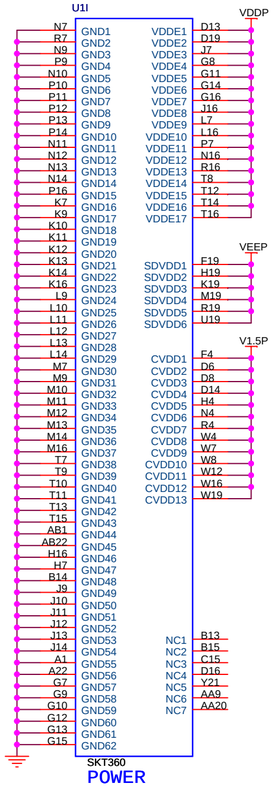
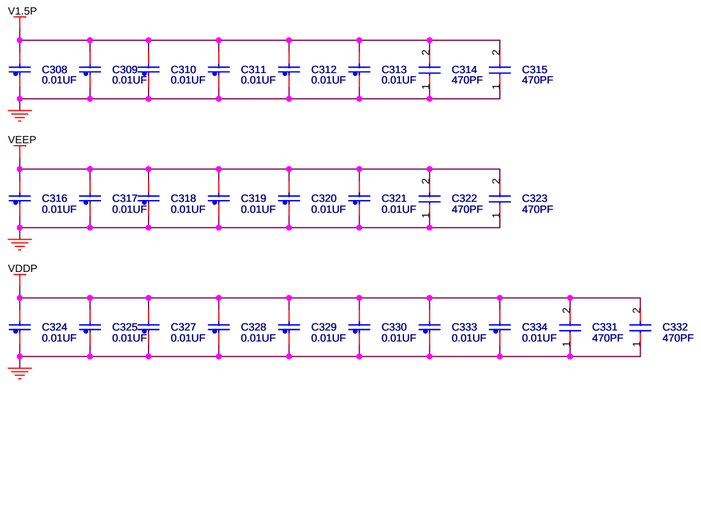
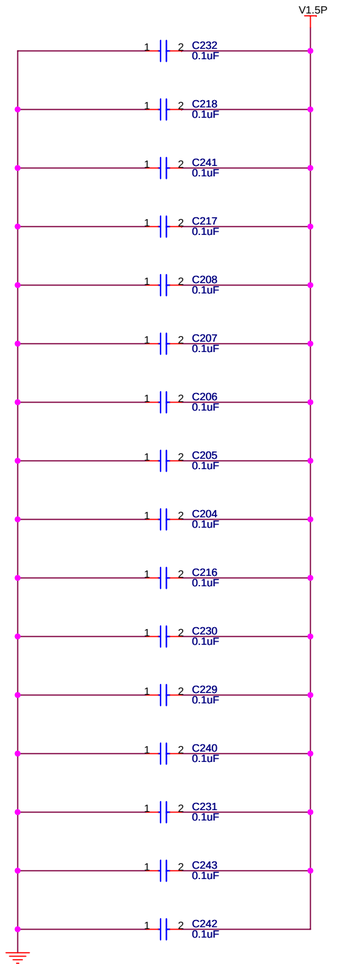
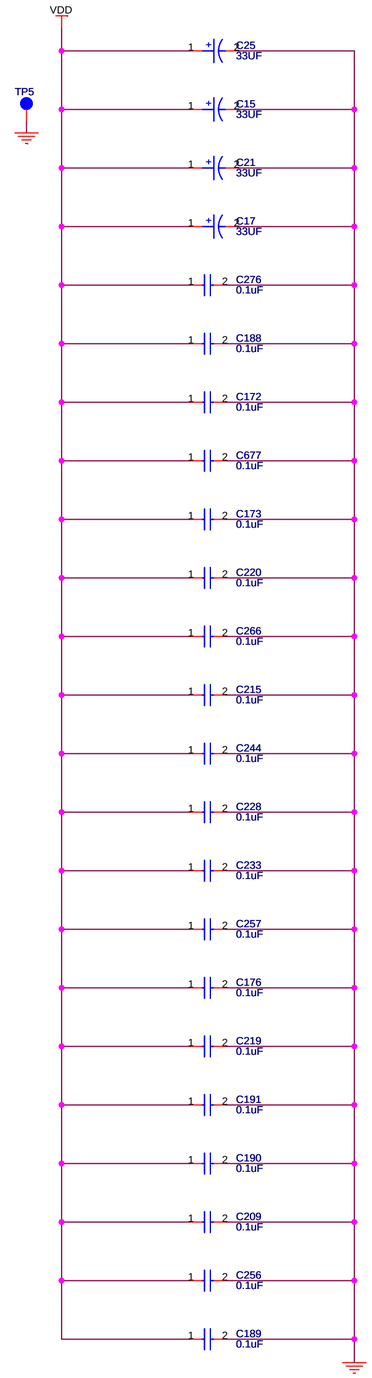
Power Indicators

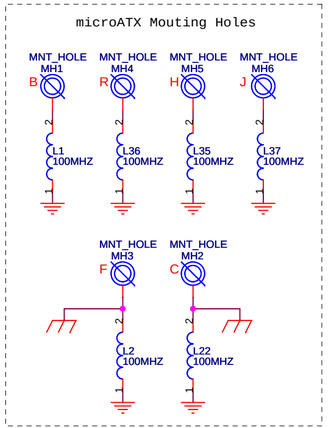












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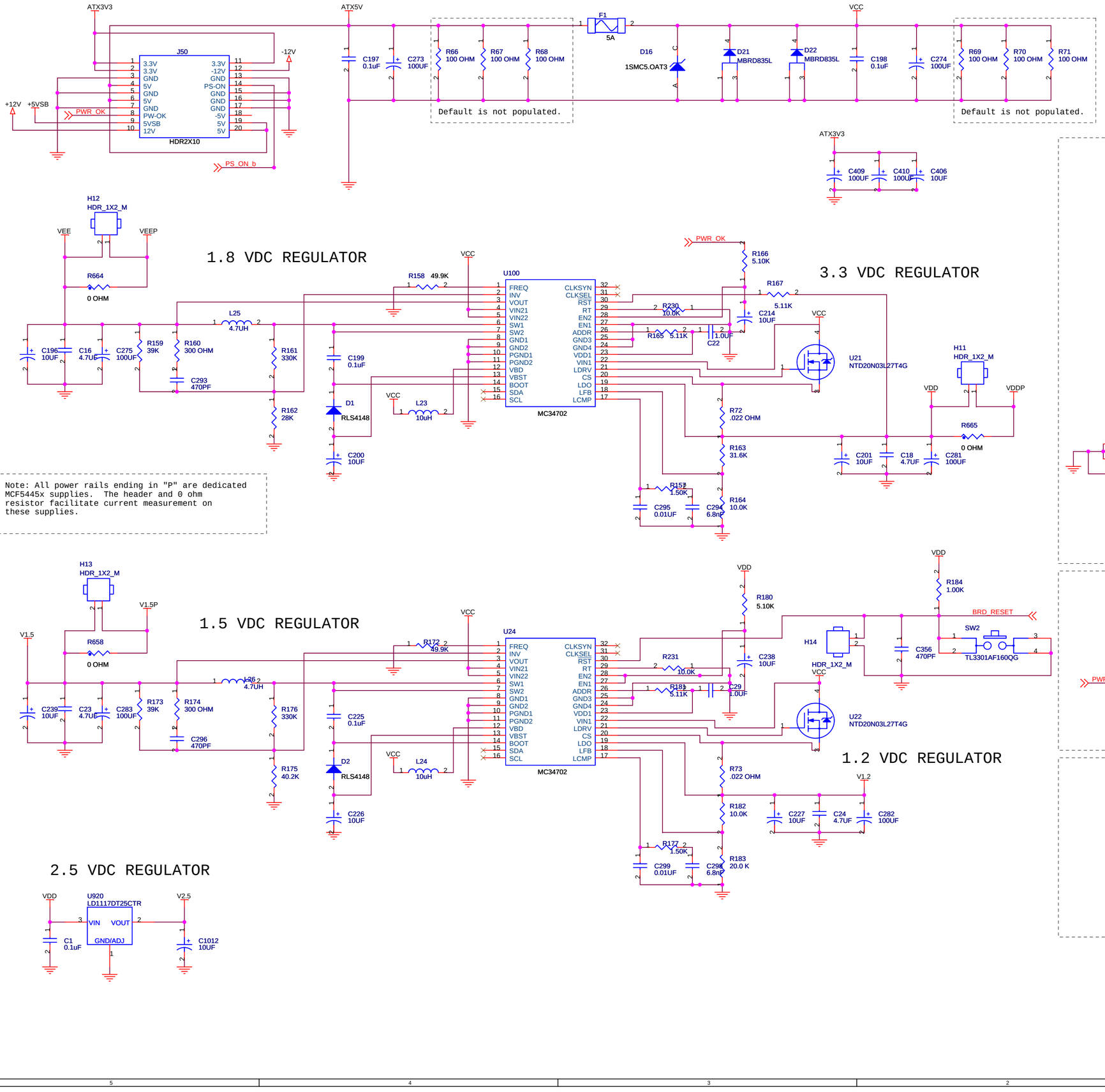

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To ATA Interface

FEC1_RMII_TXD1
FEC1_RMII_TXD0
FEC1_RMII_TXEN
FEC1_RMII_RXD1
FEC1_RMII_RXD0
FEC1_RMII_RXER
FEC1_RMII_CRS_DV
FEC1_RMII_REF_CLK
RMIICLK2

U1Q
FEC1TXCLKFEC1RMIIREFCLKATADATA11 AB19 FEC1_RMII_REF_CLK
FEC1TXENFEC1RMIITXENATADATA8 AA21 FEC1_RMII_TXEN
FEC1TXD0FEC1RMIITXD0ATADATA9 Y20 FEC1_RMII_TXD0
FEC1TXD1FEC1RMIITXD1ATADATA10 AA19 FEC1_RMII_TXD1
FEC1RXDVFEC1RMIICRSDVATADATA15 AB15 FEC1_RMII_CRS_DV
FEC1RXERFEC1RMIIRXERATADATA12 W17 FEC1_RMII_RXER
FEC1RXD0FEC1RMIIRXD0ATADATA13 Y17 FEC1_RMII_RXD0
FEC1RXD1FEC1RMIIRXD1ATADATA14 AA17 FEC1_RMII_RXD1
SKT360
FEC1_RMII

U1B
FEC0MDC AB8 FEC0_MDC
FEC0MDIO Y7 FEC0_MDIO
FEC0RXDVFEC0RMIICRSDV Y8 FEC0_RMII_CRS_DV
FEC0RXD0FECRMIIRXD0 AB10 FEC_RMII_RXD0
FEC0RXD1FEC0RMIIRXD1 W9 FEC0_RMII_RXD1
FEC0RXERFECRMIIRXER AA10 FEC_RMII_RXER
FEC0TXCLKFEC0RMIIREFCLK Y10
FEC0TXD0FEC0RMIITXD0 Y11 FEC_RMII_TXD0
FEC0TXD1FECRMIITXD1 AA11 FEC_RMII_TXD1
FEC0TXENFEC0RMIITXEN W11 FEC0_RMII_TXEN
SKT360
FECO/RMII

RMIICLK1
RMIICLK0
CPU_RSTOUT

R944 4.7K
R946 4.7K
R945 4.7K
R947 4.7K
R948 4.7K
R949 4.87K

U901
DP83849

MDIO 66
MDC 67
TXD3_B/SNI_MODE_B 45
TXD2_B 46
TXD1_B 47
TXD0_B 48
TX_EN_B 49
TX_CLK_B 50
RXD3_B/ED_EN_B 53
RXD2_B/EXTENDER_EN 56
RXD1_B/PHYAD4 57
RXD0_B/PHAD3 58
COL_B/FX_EN_B 59
RX_ER_B/MDIX_EN_B 60
CRS_B/CRS_DV_B/LED_CFG_B 61
RX_DV_B/MII_MODE_B 62
RX_CLK_B 63
RX_CLK_A 79
RX_DV_A/MII_MODE_A 80
CRS_A/CRS_DV_A/LED_CFG_A 1
RX_ER_A/MDIX_EN_A 2
COL_A/FX_EN_A 3
RXD0_A/PHYAD1 4
RXD1_A/PHYAD2 5
RXD2_A/CLK2MAC_DIS 8
RXD3_A/ED_EN_A 9
TX_CLK_A 12
TX_EN_A 13
TXD0_A 14
TXD1_A 15
TXD2_A 16
TXD3_A/SNI_MODE_A 17
X2 69
X1 70
RESET_N 71

ANA33V/DD 30
IOVDD1 11
IOVDD2 55
IOVDD3 65
IOVDD4 78
PFBOUT 31
PFBN2 28
PFBN3 24
PFBN1 7
PFBN4 54
ANAGND1 22
ANAGND2 29
ANAGND3 33
ANAGND4 40
IOGND1 10
IOGND2 52
IOGND3 64
IOGND4 77
CDGND1 25
CDGND2 37
COREGND1 6
COREGND2 55

CLK2MAC 68
PWRDOWN_INT_B 44 PHY1_PWRDN
PWRDOWN_INT_A 18 PHY0_PWRDN
LED_LINK_B/AN0_B 43
LED_SPEED_B/FXSD_B/AN1_B 42
LED_ACT/COL_B/AN_EN_B 41
TPRDM_B/FXRDM_B 39
TPRDP_B/FXRDP_B 38
TPTDM_B/FXTDM_B 36
TPTDP_B/FXTDP_B 35
TPTDP_A/FXTDP_A 27
TPTDM_A/FXTDM_A 26
TPRDP_A/FXRDP_A 24
TPRDM_A/FXRDM_A 23
LED_ACT/COL_A/AN_EN_A 21
LED_SPEED_A/FXSD_A/AN1_A 20
LED_LINK_A/AN0_A 19
TDI 76
TRSTN 75
TMS 74
TDO 73
TCK 72
RBIAS 32

R301 22 OHM
R302 22 OHM
R303 22 OHM
R304 22 OHM
R305 22 OHM
R306 22 OHM
R307 22 OHM
R740 33 OHM
R741 33 OHM
R742 33 OHM
R743 33 OHM

R951 49.9 OHM
R765 49.9 OHM
C950 0.1 UF
R952 49.9 OHM
R953 49.9 OHM
C766 0.1 UF
R950 220 OHM
C952 0.1 UF
C765 0.1 UF

P5B Upper Port
ETH1_TXD- 13 TRD1- RJ1 TRP1+
ETH1_TXD_CT 7 TRCT1
ETH1_TXD+ 6 TRD1+ RJ2 TRP1-
ETH1_RXD- 5 TRD2- RJ3 TRP2+
ETH1_RXD_CT 12 TRCT2
ETH1_RXD+ 11 TRD2+ RJ6 TRP2-
10 TRD3- RJ4 TRP3+
4 TRCT3
3 TRD3+ RJ5 TRP3-
2 TRD4- RJ7 TRP4+
9 TRCT4
8 TRD4+ RJ8 TRP4-
1 GND2
ETH1_LED_LINK- 31 LED3_C
ETH1_LED_LINK+ 32 LED3_A
R587 220 OHM
ETH1_LED_SC- 33 LED4_GC
ETH1_LED_SC+ 34 LED4_GA
Chassis_GND
Chassis_GND
S3
S4
0845-2R1T-E4

Ethernet Channel 1

LED1 indicates a LINK and blinks for activity.

LED2 indicates Speed (10/100 Mbps) and Collision (when in 10 Mbps mode). LED2 is GREEN for 100Mbps mode, OFF for 10Mbps, and blinking ORANGE for Collisions.

R955 49.9 OHM
R956 49.9 OHM
C957 0.1 UF
R958 49.9 OHM
R957 49.9 OHM
C954 0.1 UF
R959 220 OHM
C955 0.1 UF
C956 0.1 UF

P5A Lower Port
ETH0_TXD- 21 TRD1- RJ1 TRP1+
ETH0_TXD_CT 14 TRCT1
ETH0_TXD+ 15 TRD1+ RJ2 TRP1-
ETH0_RXD- 16 TRD2- RJ3 TRP2+
ETH0_RXD_CT 22 TRCT2
ETH0_RXD+ 23 TRD2+ RJ6 TRP2-
24 TRD3- RJ4 TRP3+
17 TRCT3
18 TRD3+ RJ5 TRP3-
19 TRD4- RJ7 TRP4+
25 TRCT4
26 TRD4+ RJ8 TRP4-
20 GND1
ETH0_LED_LINK- 27 LED1_C
ETH0_LED_LINK+ 28 LED1_A
R954 220 OHM
ETH0_LED_SC- 29 LED2_GC
ETH0_LED_SC+ 30 LED2_GA
Chassis_GND
Chassis_GND
S1
S2
0845-2R1T-E4

Ethernet Channel 0

LED1 indicates a LINK and blinks for activity.

LED2 indicates Speed (10/100 Mbps) and Collision (when in 10 Mbps mode). LED2 is GREEN for 100Mbps mode, OFF for 10Mbps, and blinking ORANGE for Collisions.

C11 0.1 UF
C12 0.1 UF
C14 0.1 UF
C31 0.1 UF
C2 0.1 UF
C6 0.1 UF
C7 0.1 UF
C8 0.1 UF
C9 0.1 UF
C3 10UF
C4 0.1 UF

Both ports of the Ethernet PHY are placed into RMII mode. The MII management channel is connected to the FEC0 MDC/MDIO interface only (e.g. all MII management communications must go through FEC0). The default PHY addresses of 0x0 (FEC0) and 0x1 (FEC1) are used.

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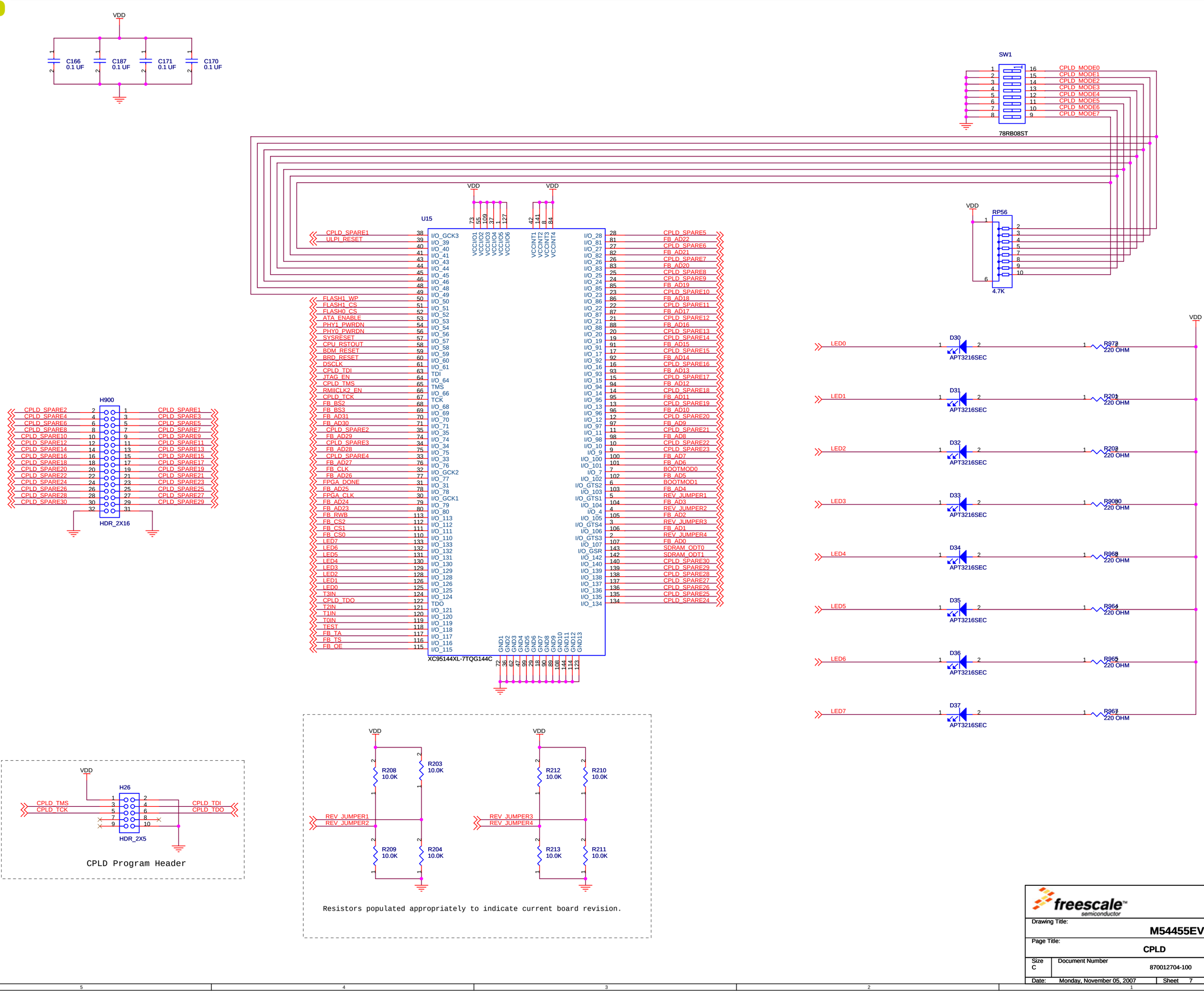

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SERIAL BOOT FLASH

PARALLEL BOOT CONFIGURATION

SW3
78RB08ST
RN16
4.7K
U902
74LV541/SO
FB_AD0
FB_AD1
FB_AD2
FB_AD3
FB_AD4
FB_AD5
FB_AD6
FB_AD7

DSPI/SBF

U1E
SKT360
DSPISCKSBFCK
DSPISINSBFDI
DSPISOUTSBFDO
DSPIPCS0DSPISSb
DSPIPCS1SCFCSb
DSPIPCS2
DSPIPCS5DSPIPCSSb
DSPI_SCK
DSPI_SOUT
DSPI_SIN
DSPI_PCS0
DSPI_PCS1
DSPI_PCS2
DSPI_PCS5
R971 4.7K
R970 4.7K
U905
M25P16-SO16
DSPI_PCS1
DSPI_SIN
DSPI_SCK
DSPI_SOUT
U906
M25P16-VMW6G
ALTERNATIVE PART, DNP
CPU_RSTOUT

RESET/BOOT MODE

U1D
SKT360
RESETb
RSTOUTb
BOOTMOD0
BOOTMOD1
TEST
TEST
BOOTMOD1
BOOTMOD0
SYSRESET

BDM/JTAG

U1F
SKT360
PSTDDATA7
PSTDDATA6
PSTDDATA5
PSTDDATA4
PSTDDATA3
PSTDDATA2
PSTDDATA1
PSTDDATA0
JTAGEN
TCLKPSTCLK
TDIDSI
TDODSO
TMSBKPTb
TRSTBDSCLK
DSCLK
JTAG_EN
FB_TA

BDM

RN17
4.7K
JP903
HDR_1X3
R976 4.7K
R977 4.7K
R9083
22 OHM
TP1
JP904
HDR_1X3
R979 10K
R9084 100 OHM
Default is DNP
TCLK_PSTCLK

J24
HDR_2X13
BDM_RESET
BKPT
DSCLK
TCLK
EXTERNAL_DSI
DSO
PSTDDATA7
PSTDDATA5
PSTDDATA3
PSTDDATA1
PSTCLK
FB_TA
DSI
EXTERNAL_DSI
BKPT
DSO
PSTDDATA0
PSTDDATA1
PSTDDATA2
PSTDDATA3
TCLK_PSTCLK

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Drawing Title:	M54455EVB
Page Title:	BOOT, SBF & BDM
Size C	Document Number 870012704-100 Rev C
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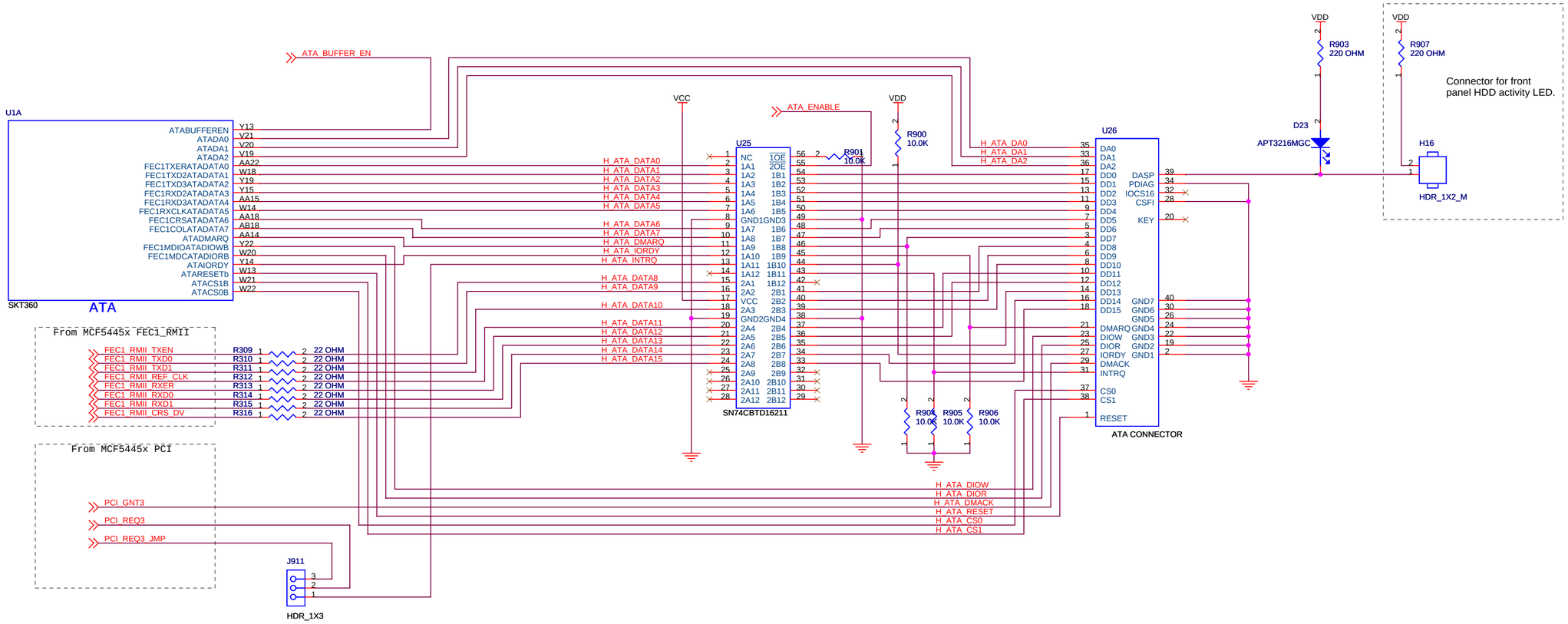

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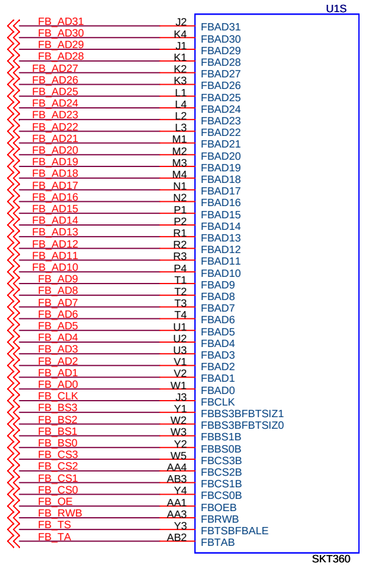
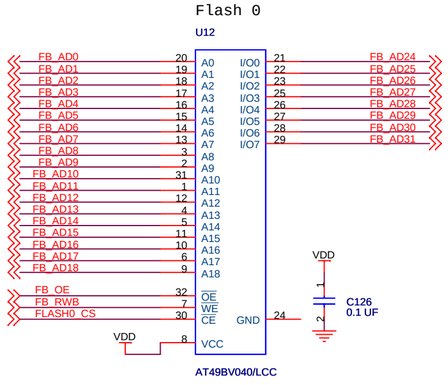
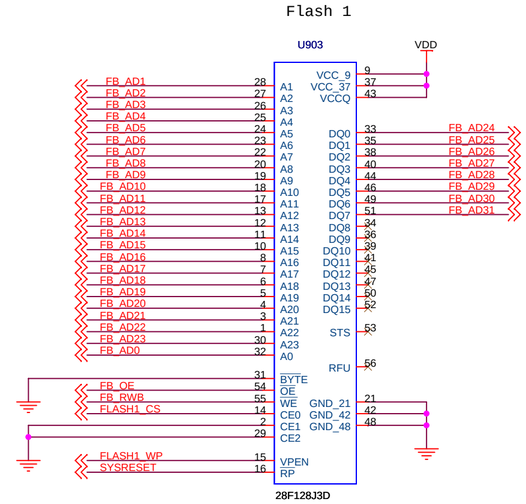
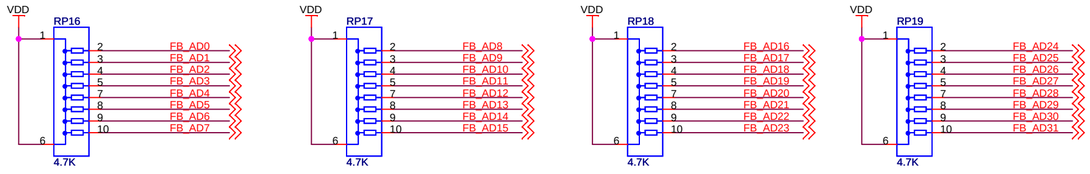
Drawing Title:	M54455EVB	
Page Title:	ATA	
Size: C	Document Number: 870012704-100	Rev: C
Date: Monday, November 05, 2007	Sheet 9 of 17	

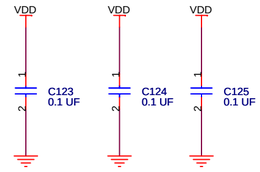






The CPLD_MODE[2] setting determines which flash device gets which chip-select (FB_CS0 or FB_CS1). The device connected to FB_CS0 is the boot device.





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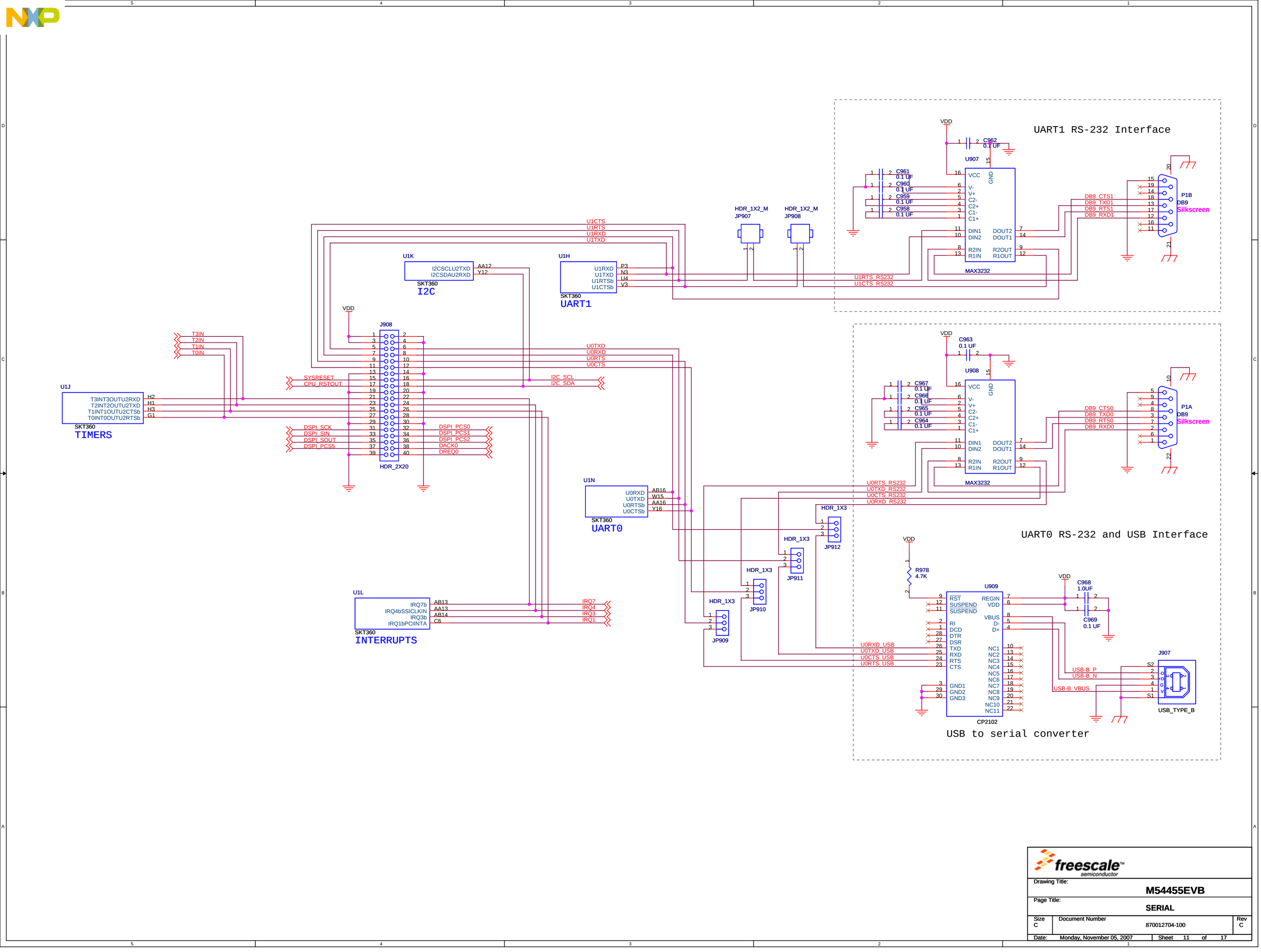
Drawing Title:	M54455EVB	
Page Title:	FLASH	
Size C	Document Number 870012704-100	Rev C
Date: Monday, November 05, 2007	Sheet 10 of 17	



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Drawing Title:	**M54455EVB**	
Page Title:	**SERIAL**	
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CLOCKING

U1G
SKT360
XTAL32K
EXTAL32K
EXTAL
XTAL
VDDOSC
VDDRTC
VDDAPLL
VSSOSC
PLLTEST
A12 XTAL32K
A13 EXTAL32K
A16 EXTAL
A17 XTAL
B16 VDD_OSC
C13 VDD_RTC
C14 VDD_A_PLL
C16 VSS_OSC
D15

CT11
EXTAL
CPUCLK
EXTAL_OSC
0 OHM

VDDP
R139 10.0 OHM
C555 1.0UF
C556 0.1 UF
L27 2 100MHZ
R137 18M
X2 32.768MHz
C1011 15PF
C1010 15PF
R136 1.0M
X1 25MHZ
C975 33PF
C974 33PF

V1.5P
R139 10.0 OHM
C557 1.0UF
C559 0.1 UF
V1.5P
R140 10.0 OHM
C558 1.0UF
C560 0.1 UF

H4
HDR 2X2

CLK_GEN_S2
I2C_SCL
I2C_SDA

VDD
C127 0.1 UF
C326 0.1 UF
X3 25MHZ

U8
CY22393
SDAT/S0
SCLK/S1
S2/SUSPEND
SHUTDOWN/OE
VDD
AVDD
AGND
GND
XTALIN
XTALOUT
CLKA
CLKB
CLKC
CLKD
CLKE
XBUF

R128 22 OHM
R318 22 OHM
R35 22 OHM
R126 22 OHM
R317 22 OHM
CPUCLK
USBCLK_60
USBCLK_24

VDD
C128 0.1 UF
C335 0.1 UF

U3
CY2309ZXC-1H
VDD
VDD
REF
S2
S1
GND
GND
CLKOUT
CLKA1
CLKA2
CLKA3
CLKA4
CLKB1
CLKB2
CLKB3
CLKB4

22OHM
RN59A RMIICLK0
RN59B RMIICLK1
RN59C RMIICLK2
RN59D

RMIICLK2_EN

VDD
RP78
4.7K

VDD
C84 0.1 UF
C96 0.1 UF

U2
CY2309ZXC-1H
RN57A PCI_CLK0
RN57B PCI_CLK1
RN57C PCI_CLK2
RN57D PCI_CLK3
RN58A PCI_CLK4
RN58B FPGA_CLK
RN58C PCI_CLK5
RN58D
22OHM

C85 47PF

PCI CLOCK BUFFER

J10 SMA
R142 51 OHM
R122 0 OHM
CPUCLK

J11 SMA
R143 51 OHM
R125 0 OHM

TP4
J12 SMA
R144 51 OHM
R127 0 OHM
USBCLK_24

J13 SMA
R145 51 OHM
R129 0 OHM
USBCLK_60

TP3
J18 SMA
R149 51 OHM
R130 0 OHM

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Drawing Title:	M54455EVB		
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DDR2 Parallel Termination - place near DDR2 devices

T1	SD_D17	RN101A 51 OHM VTT	T13	SD_A7	RN104A 51 OHM VTT	T25	SD_A11	RN107A 51 OHM VTT	T37	SD_D31	RN110A 51 OHM VTT
T2	SD_D16	RN101B 51 OHM VTT	T14	SD_A3	RN104B 51 OHM VTT	T26	SD_CKE	RN107B 51 OHM VTT	T38	SD_D30	RN110B 51 OHM VTT
T3	SD_DQS2	RN101C 51 OHM VTT	T15	SD_A10	RN104C 51 OHM VTT	T27	SD_A2	RN107C 51 OHM VTT	T39	SD_DM3	RN110C 51 OHM VTT
T4	SD_DM2	RN101D 51 OHM VTT	T16	SD_CAS	RN104D 51 OHM VTT	T28	SD_A0	RN107D 51 OHM VTT	T40	SD_DQS3	RN110D 51 OHM VTT
T5	SD_D22	RN102A 51 OHM VTT	T17	SD_BA0	RN105A 51 OHM VTT	T29	SD_A4	RN108A 51 OHM VTT	T41	SD_D24	RN111A 51 OHM VTT
T6	SD_D23	RN102B 51 OHM VTT	T18	SD_A6	RN105B 51 OHM VTT	T30	SD_A8	RN108B 51 OHM VTT	T42	SD_D25	RN111B 51 OHM VTT
T7	SD_D20	RN102C 51 OHM VTT	T19	SD_WE	RN105C 51 OHM VTT	T31	SD_A13	RN108C 51 OHM VTT	T43	SD_CLK_N	
T8	SD_D18	RN102D 51 OHM VTT	T20	SD_A9	RN105D 51 OHM VTT	T32	SD_CS1	RN108D 51 OHM VTT	T44	SD_CLK_P	
T9	SD_D21	RN103A 51 OHM VTT	T21	SD_A1	RN106A 51 OHM VTT	T33	SD_D27	RN109A 51 OHM VTT			
T10	SD_D19	RN103B 51 OHM VTT	T22	SD_BA1	RN106B 51 OHM VTT	T34	SD_D29	RN109B 51 OHM VTT			
T11	SD_CS0	RN103C 51 OHM VTT	T23	SD_A5	RN106C 51 OHM VTT	T35	SD_D26	RN109C 51 OHM VTT			
T12	SD_A12	RN103D 51 OHM VTT	T24	SD_RAS	RN106D 51 OHM VTT	T36	SD_D28	RN109D 51 OHM VTT			

Place series termination resistors as close to U1 as possible

U1O — SKT360

SDD31	L21	RN91A 8 1	22OHM	SD_D31
SDD30	K22	RN90B 7 2	22OHM	SD_D30
SDD29	K21	RN90A 8 1	22OHM	SD_D29
SDD28	K20	RN91B 7 2	22OHM	SD_D28
SDD27	J20	RN91D 5 4	22OHM	SD_D27
SDD26	J19	RN91C 6 3	22OHM	SD_D26
SDD25	J21	RN90C 6 3	22OHM	SD_D25
SDD24	J22	RN90D 5 4	22OHM	SD_D24
SDD23	H20	RN92A 8 1	22OHM	SD_D23
SDD22	G22	RN94C 6 3	22OHM	SD_D22
SDD21	G21	RN94D 5 4	22OHM	SD_D21
SDD20	G20	RN92B 7 2	22OHM	SD_D20
SDD19	G19	RN92C 6 3	22OHM	SD_D19
SDD18	F22	RN93A 8 1	22OHM	SD_D18
SDD17	F21	RN93B 7 2	22OHM	SD_D17
SDD16	F20	RN92D 5 4	22OHM	SD_D16
SDDM3	H21	RN94B 7 2	22OHM	SD_DM3
SDDM2	E21	RN93D 5 4	22OHM	SD_DM2
SDDQS3	H22	RN94A 8 1	22OHM	SD_DQS3
SDDQS2	E22	RN93C 6 3	22OHM	SD_DQS2
SDRASb	N21	RN100C 6 3	22OHM	SD_RAS
SDCASb	L19	RN100D 5 4	22OHM	SD_CAS
SDWEb	N20	RN100A 8 1	22OHM	SD_WE
SDCS0b	M20	RN95C 6 3	22OHM	SD_CS0
SDCS1b	L20	RN95D 5 4	22OHM	SD_CS1
SDA13	V22	RN96A 8 1	22OHM	SD_A13
SDA12	U20	RN97D 5 4	22OHM	SD_A12
SDA11	U21	RN96B 7 2	22OHM	SD_A11
SDA10	U22	RN96C 6 3	22OHM	SD_A10
SDA9	T19	RN97C 6 3	22OHM	SD_A9
SDA8	T20	RN99A 8 1	22OHM	SD_A8
SDA7	T21	RN96D 5 4	22OHM	SD_A7
SDA6	T22	RN98A 8 1	22OHM	SD_A6
SDA5	R20	RN99B 7 2	22OHM	SD_A5
SDA4	R21	RN98B 7 2	22OHM	SD_A4
SDA3	R22	RN98C 6 3	22OHM	SD_A3
SDA1	P20	RN99C 6 3	22OHM	SD_A1
SDA2	N19	RN95B 7 2	22OHM	SD_A2
SDA0	P21	RN98D 5 4	22OHM	SD_A0
SDBA0	P19	RN95A 8 1	22OHM	SD_BA0
SDBA1	P22	RN99D 5 4	22OHM	SD_BA1
SDCKE	N22	RN100B 7 2	22OHM	SD_CKE
SDCLK	L22	R148 1 2	22 OHM	SD_CLK_P
SDCLKb	M22	R150 1 2	22 OHM	SD_CLK_N
SDVREF	M21	VREF RN97B 7 2	22OHM	
		RN97A 8 1	22OHM	

R687 100 OHM

Place R687 close to the DDR2 devices

VEE: C976 100PF, C981 1000PF, C983 0.1 UF, C984 0.1 UF, C985 1000PF, C982 1000PF, C977 100PF, C986 100PF, C988 1000PF, C989 0.1 UF, C987 100PF, C990 1000PF, C991 0.1 UF, C979 10UF

VTT: C980 100PF, C1003 1000PF, C993 0.1 UF, C994 0.1 UF, C995 1000PF, C992 1000PF, C978 100PF, C996 100PF, C1004 0.1 UF, C999 0.1 UF, C1005 1000PF, C1000 1000PF, C997 100PF, C998 100PF, C1001 1000PF, C1006 0.1 UF, C1007 100PF, C1008 1000PF, C1009 0.1 UF, C1002 10UF

DDR2 SDRAMs

U911 — MT47H64M8 — VEE, VREF, C5 0.1 UF

SD_D31 SD_D30 SD_D29 SD_D28 SD_D27 SD_D26 SD_D25 SD_D24 — SD_RAS SD_CAS SD_WE SD_CS0 — SD_DM3 SD_DQS3 — SDRAM_ODT0 — R555 4.7K

CKE SD_CKE; CK SD_CLK_P; CK# SD_CLK_N; BA0 SD_BA0; BA1 SD_BA1; BA2 G1

A0 SD_A0; A1 SD_A1; A2 SD_A2; A3 SD_A3; A4 SD_A4; A5 SD_A5; A6 SD_A6; A7 SD_A7; A8 SD_A8; A9 SD_A9; A10 SD_A10; A11 SD_A11; A12 SD_A12; A13 SD_A13; A14 L3; A15 L7

U912 — MT47H64M8 — VEE, VREF, C10 0.1 UF

SD_D23 SD_D22 SD_D21 SD_D20 SD_D19 SD_D18 SD_D17 SD_D16 — SD_RAS SD_CAS SD_WE SD_CS0 — SD_DM2 SD_DQS2 — SDRAM_ODT0 — R556 4.7K

CKE SD_CKE; CK SD_CLK_P; CK# SD_CLK_N; BA0 SD_BA0; BA1 SD_BA1; BA2 G1

A0 SD_A0; A1 SD_A1; A2 SD_A2; A3 SD_A3; A4 SD_A4; A5 SD_A5; A6 SD_A6; A7 SD_A7; A8 SD_A8; A9 SD_A9; A10 SD_A10; A11 SD_A11; A12 SD_A12; A13 SD_A13; A14 L3; A15 L7

SDRAM_ODTn signals are controlled by the CPLD and are for test purposes only. The MCF5445x does not provide control signals for DDR2 on-die termination. Discrete parallel terminators are used in this design.

U913 — MT47H64M8 — VEE, VREF, C13 0.1 UF

SD_D31 SD_D30 SD_D29 SD_D28 SD_D27 SD_D26 SD_D25 SD_D24 — SD_RAS SD_CAS SD_WE SD_CS1 — SD_DM3 SD_DQS3 — SDRAM_ODT1 — R557 4.7K

CKE SD_CKE; CK SD_CLK_P; CK# SD_CLK_N; BA0 SD_BA0; BA1 SD_BA1; BA2 G1

A0 SD_A0; A1 SD_A1; A2 SD_A2; A3 SD_A3; A4 SD_A4; A5 SD_A5; A6 SD_A6; A7 SD_A7; A8 SD_A8; A9 SD_A9; A10 SD_A10; A11 SD_A11; A12 SD_A12; A13 SD_A13; A14 L3; A15 L7

U914 — MT47H64M8 — VEE, VREF, C19 0.1 UF

SD_D23 SD_D22 SD_D21 SD_D20 SD_D19 SD_D18 SD_D17 SD_D16 — SD_RAS SD_CAS SD_WE SD_CS1 — SD_DM2 SD_DQS2 — SDRAM_ODT1 — R558 4.7K

CKE SD_CKE; CK SD_CLK_P; CK# SD_CLK_N; BA0 SD_BA0; BA1 SD_BA1; BA2 G1

A0 SD_A0; A1 SD_A1; A2 SD_A2; A3 SD_A3; A4 SD_A4; A5 SD_A5; A6 SD_A6; A7 SD_A7; A8 SD_A8; A9 SD_A9; A10 SD_A10; A11 SD_A11; A12 SD_A12; A13 SD_A13; A14 L3; A15 L7

DDR2 termination and reference voltage regulator.

J906 HDR_1X2_M — VDD — R922 4.7K

Vsense should be connected to the center of the Vtt termination bus.

U900 LP2997MR NOPB: SD, AVin, Vddq, PVin, GND1, GND2, Vref, Vsense, Vtt

VDD, VEE, VTT, VREF

C922 47UF; C920 0.01UF; C921 220UF

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Drawing Title:	M54455EVB
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FPGA Platform Flash

U917 — XCF02SVOG20C

Pin	Net
3 CLK	FPGA_CCLK
4 TDI	XPF_TDI
17 TDO	XPF_TDO
5 TMS	XPF_TMS
6 TCK	XPF_TCK
8 OE/RESET	FPGA_INIT_b
13 CEO	XPF_D0
1 D0	XPF_CF_b
7 CF	FPGA_DONE
10 CE	
18 VCCINT, 19 VCCO, 20 VCCJ	VDD
11 GND	
2, 9, 12, 14, 15, 16 NC1–NC6	

FPGA Program Header

H20 — HDR_2X5

XPF_TMS	3	4	XPF_TDI
XPF_TCK	5	6	FPGA_TDO

VDD

FPGA_M2 / FPGA_M1 / FPGA_M0

FPGA_M2	R673 0 OHM
FPGA_M1	R674 0 OHM
FPGA_M0	R675 0 OHM

RN114 (4.7K)

VDD

1	
2	XPF_TDO
3	XPF_TMS
4	XPF_TCK
5	XPF_CF_b
7	FPGA_INIT_b
8	FPGA_DONE
9	FPGA_CCLK
10	
6	

D958 / D957 / D956

VDD

FPGA_LED0	D958 APT3216MGC	R444 220 OHM
FPGA_LED1	D957 APT3216MGC	R445 220 OHM
FPGA_LED2	D956 APT3216MGC	R446 220 OHM

H21 — HDR_2X4

I2C_SCL	1	2	XPF_TCK
I2C_SDA	3	4	XPF_TMS
ATA_BUFFER_EN	5	6	XPF_TDI
DSPI_PCS2	7	8	FPGA_TDO

These jumpers provide connections from GPIO signals on the MCF5445x to the JTAG interface of the FPGA platform flash.

U919 — XC3S400-4FTG256C

V2.5, V1.2, VDD

Pin	Net
T16	GND1
T15	CCLK
T14	IO1
T13	IO_L01P_4/VRN_4
T12	IO2
T11	VCCAUX1
T10	IO/VREF_41
T9	IO_L32P_4/GCLK0
T8	IO/VREF_5
T7	IO_L31N_5/D4
T6	VCCAUX2
T5	IO3
T4	IO_L10N_5/VRP_5
T3	IO_L01N_5/RDWR_B
T2	M1
T1	GND2
R16	IO_L01P_3/VRN_3
R15	GND3
R14	DONE
R13	IO_L01N_4/VRP_4
R12	IO_L25P_4
R11	IO_L28P_4
R10	IO_L30P_4/D3
R9	IO_L32N_4/GCLK1
R8	GND4
R7	IO_L31P_5/D5
R6	IO_L29N_5
R5	IO_L27N_5/VREF_5
R4	IO_L10P_5/VRN_5
R3	IO_L01P_5/CS_B
R2	GND5
R1	IO_L01N_6/VRP_6
P16	IO_L01N_3/VRP_3
P15	IO_L16N_3
P14	IO_L16P_3
P13	IO/VREF_42
P12	IO_L25N_4
P11	IO_L28N_4
P10	IO_L30N_4/D2
P9	IO_L31P_4/DOUT/BUSY
P8	IO_L32N_5/GCLK3
P7	IO4
P6	IO_L29P_5/VREF_5
P5	IO_L27P_5
P4	M2
P3	MO
P2	IO_L16N_6
P1	IO_L01P_6/VRN_6
N16	IO_L17N_3
N15	IO_L17P_3/VREF_3
N14	IO_L19P_3
N13	VCCINT7
N12	IO/VREF_43
N11	IO_L27P_4/D1
N10	IO_L29P_4
N9	IO_L31N_4/INIT_B
N8	IO_L32P_5/GCLK2
N7	IO_L30N_5
N6	IO_L28N_5/D6
N5	IO5
N4	VCCINT8
N3	IO_L16P_62
N2	IO_L17N_6
N1	IO_L17P_6/VREF_6
M16	IO_L20N_3
M15	IO_L20P_3
M14	IO_L19N_3
M13	IO_L21P_3
M12	VCCINT1
M11	IO_L27N_4/DIN/D0
M10	IO_L29N_4
M9	VCCO_4
M8	VCCO_5
M7	IO_L30P_5
M6	IO_L28P_5/D7
M4	IO_L19N_6
M3	IO_L19P_6
M2	IO_L20N_6
M1	IO_L20P_6
M5	VCCINT2
L16	VCCAUX3
L15	IO_L22N_3
L14	IO_L22P_3
L13	IO_L21N_3
L12	IO_L23P_3/VREF_3
L11	GND6
L10	VCCO_4
L9	VCCO_4
L8	VCCO_5
L7	VCCO_5
L6	GND7
L5	IO_L21N_6
L4	IO_L21P_6
L3	IO_L22N_6
L2	IO_L22P_6
L1	VCCAUX4
A1	GND8
A2	TDI
A3	IO/VREF_01
A4	IO_L01P_0/VRN_0
A5	IO6
A6	VCCAUX5
A7	IO7
A8	IO_L32P_0/GCLK6
A9	IO8
A10	IO_L31N_1/VREF_1
A11	VCCAUX6
A12	IO9
A13	IO_L10N_1/VREF_1
A14	IO_L01N_1/VRP_1
A15	TDO
A16	GND9
B1	IO_L01P_7/VRN_7
B2	GND10
B3	PROG_B
B4	IO_L01N_0/VRP_0
B5	IO_L25P_0
B6	IO_L28P_0
B7	IO_L30P_0
B8	IO_L32N_0/GCLK7
B9	GND11
B10	IO_L31P_1
B11	IO_L29N_1
B12	IO_L27N_1
B13	IO_L10P_1
B14	IO_L01P_1/VRN_1
B15	GND12
B16	IO_L01N_2/VRP_2

FPGA_CCLK	
MEM_ADDR4	
MEM_ADDR8	
MEM_ADDR12	
FPGA_CFG2	
PCI_CLK4	
FPGA_SPARE0	
FPGA_SPARE1	
FB_AD19	
FB_AD11	
FB_AD7	
FPGA_M1	
MEM_DATA29	
FPGA_DONE	R2 56 OHM
MEM_ADDR16	
MEM_BE1_b	
FPGA_CFG3	
FPGA_CFG1	
CF_PCI_REQ0	
FB_AD27	
FB_AD23	
FB_AD15	
FB_AD3	
M66EN	
MEM_DATA25	
CLK_GEN_S2	
BRD_RESET	
MEM_DATA18	
MEM_DATA22	
MEM_DATA30	
FPGA_CFG0	
FPGA_CLK	
PCI_IRQ0	
FB_CS3	
FB_AD31	
FPGA_M2	
FPGA_M0	
DREQ0	
MEM_DATA17	
MEM_RW	
MEM_DATA26	
FPGA_INIT_b	
PCI_IRQ1	
FB_TS	
FB_BS3	
LED2_SEG7	
DACK0	
FB_AD30	
MEM_BE0_b	
MEM_DATA21	
FPGA_UDTR	
XPF_D0	
PCI_IRQ2	
PCI_IRQ3	
CF_PCI_GNT0	
LED2_SEG6	
LED2_SEG5	
FB_AD26	
FB_AD10	
MEM_ADDR15	
FPGA_UTXD	
FPGA_UDSR	
FPGA_UCLK	
LED2_SEG4	
LED2_SEG3	
FB_TA	
FB_AD22	
XPF_TDO	R3 56 OHM FPGA_TDI
FB_AD8	
FB_AD4	
FB_AD0	
PCI_FRAME	
FPGA_LED1	
FPGA_LED2	
MEM_ADDR17	
MEM_ADDR9	
MEM_ADDR1	
FPGA_TDO	
FB_AD1	
XPF_CF_b	R1 56 OHM FPGA_PROG_b
FB_AD16	
FB_AD12	
FB_AD28	
SLOT_PCI_GNT0	
FB_CLK	
FPGA_LED0	
MEM_DATA27	
MEM_CS_b	
MEM_ADDR13	
MEM_ADDR5	
MEM_ADDR2	

VDD, V1.2, V2.5

Pin	Net
VCCAUX7 F16	
IO_L22P_2 F15	MEM_DATA24
IO_L22N_2 F14	
IO_L21P_2 F13	
IO_L21N_2 F12	
GND31 F11	
VCCO_1 F10	
VCCO_1 F9	
VCCO_0 F8	
VCCO_0 F7	
GND32 F6	
IO_L23P_7 F5	LED1_SEG2
IO_L21N_7 F4	LED1_SEG1
IO_L22P_7 F3	LED1_SEG0
IO_L22N_7 F2	IRQ4
VCCAUX8 F1	
IO13 G16	MEM_DATA28
IO_L24P_2 G15	
IO_L24N_2 G14	
IO_L23P_2 G13	
IO_L23N_2/VREF_2 G12	
VCCO_2 G11	
GND27 G10	
GND28 G9	
GND29 G8	
GND30 G7	
VCCO_7 G6	
IO_L23N_7 G5	LED1_SEG5
IO_L24P_7 G4	LED1_SEG4
IO_L24N_7 G3	LED1_SEG3
IO14 G2	IRQ7
IO_L40P_7 G1	IRQ3
IO_L40P_2/VREF_2 H16	MEM_OE_b
IO_L40N_2 H15	
IO_L39P_2 H14	
IO_L39N_2 H13	
VCCO_2 H12	
VCCO_2 H11	
GND22 H10	
GND23 H9	
GND24 H8	
GND25 H7	
VCCO_7 H6	
VCCO_7 H5	
IO_L39P_7 H4	LED1_SEG7
IO_L39N_7 H3	LED1_SEG6
GND26 H2	
IO_L40N_7/VREF_7 H1	IRQ1
IO_L40N_3/VREF_3 J16	MEM_ADDR3
GND17 J15	
IO_L39N_3 J14	FPGA_URTS
IO_L39P_3 J13	FPGA_UCTS
VCCO_3 J12	
VCCO_3 J11	
GND18 J10	
GND19 J9	
GND20 J8	
GND21 J7	
VCCO_6 J6	
VCCO_6 J5	
IO_L39N_6 J4	LED2_SEG0
IO_L39P_6 J3	FB_BS2
IO_L40N_6 J2	FB_AD14
IO_L40P_6/VREF_6 J1	FB_AD2
IO_L40P_3 K16	MEM_ADDR7
IO11 K15	MEM_ADDR11
IO_L24N_3 K14	FPGA_URXD
IO_L24P_3 K13	FPGA_UDCD
IO_L23N_3 K12	FPGA_URI
VCCO_3 K11	
GND13 K10	
GND14 K9	
GND15 K8	
GND16 K7	
VCCO_6 K6	
IO_L23N_6 K5	LED2_SEG2
IO_L23P_6 K4	LED2_SEG1
IO_L24N_6/VREF_6 K3	FB_CS2
IO_L24P_6 K2	FB_AD18
IO12 K1	FB_AD6
IO_L20P_2 E16	MEM_ADDR18
IO_L20N_2 E15	MEM_DATA20
IO_L19P_2 E14	
IO_L19N_2 E13	
VCCINT5 E12	
IO_L28P_1 E11	PCI_RESET
IO_L30P_1 E10	
VCCO_1 E9	
VCCO_0 E8	
IO_L29N_0 E7	SLOT_PCI_REQ0
IO_L27N_0 E6	FB_OE
VCCINT6 E5	
IO_L21P_7 E4	FB_RWB
IO_L19N_7/VREF_7 E3	FB_CS1
IO_L20P_7 E2	FB_AD29
IO_L20N_7 E1	FB_AD21
IO_L17P_2/VREF_2 D16	MEM_ADDR14
IO_L17N_2 D15	MEM_DATA16
IO_L16P_2 D14	
VCCINT3 D13	
IO/VREF_1 D12	MEM_DATA23
IO_L28N_1 D11	F_PCI_REQ2
IO_L30N_1 D10	F_PCI_REQ3
IO_L32P_1/GCLK4 D9	PCI_IRDY
IO_L31N_0 D8	F_PCI_GNT3
IO_L29P_0 D7	FB_CS0
IO_L27P_0 D6	FB_AD24
IO/VREF_02 D5	
VCCINT4 D4	
IO_L19P_7 D3	FB_BS1
IO_L17P_7 D2	FB_AD17
IO_L17N_7 D1	FB_AD9
IO_L01P_2/VRN_2 C16	MEM_ADDR6
IO_L16N_2 C15	MEM_ADDR10
TCK C14	R4 56 OHM XPF_TCK
TMS C13	R5 56 OHM XPF_TMS
IO_L27P_1 C12	MEM_DATA19
IO_L29P_1 C11	MEM_DATA31
IO10 C10	F_PCI_REQ1
IO_L32N_1/GCLK5 C9	
IO_L31P_0/VREF_0 C8	F_PCI_GNT2
IO_L30N_0 C7	F_PCI_GNT1
IO_L28N_0 C6	FB_BS0
IO_L25N_0 C5	FB_AD20
HSWAP_EN C4	HSWAP_EN
IO_L16P_7/VREF_7 C3	FB_AD25
IO_L16N_7 C2	FB_AD13
IO_L01N_7/VRP_7 C1	FB_AD5

These spare test points should be placed in a row. Preferably 0.1 inch spacing.

TP6 FPGA_SPARE0, TP7 FPGA_SPARE1

SW6 / SW7

SW6 TL3301AF160QG — MEM_DATA28

SW7 TL3301AF160QG

MRAM

U915 — U? mr2a16a — 256k x 16 bit 3.3V

VDD (11, 33)

MEM_ADDR1	MEM_DATA16
MEM_ADDR2	MEM_DATA17
MEM_ADDR3	MEM_DATA18
MEM_ADDR4	MEM_DATA19
MEM_ADDR5	MEM_DATA20
MEM_ADDR6	MEM_DATA21
MEM_ADDR7	MEM_DATA22
MEM_ADDR8	MEM_DATA23
MEM_ADDR9	MEM_DATA24
MEM_ADDR10	MEM_DATA25
MEM_ADDR11	MEM_DATA26
MEM_ADDR12	MEM_DATA27
MEM_ADDR13	MEM_DATA28
MEM_ADDR14	MEM_DATA29
MEM_ADDR15	MEM_DATA30
MEM_ADDR16	MEM_DATA31
MEM_ADDR17	
MEM_ADDR18	
MEM_CS_b	
MEM_OE_b	
MEM_RW	
MEM_BE0_b	
MEM_BE1_b	

FPGA RS-232 Interface

U916 — MAX3243CDB

FPGA_UDTR	DB9_UDTR
FPGA_URTS	DB9_URTS
FPGA_UTXD	DB9_UTXD
DB9_URXD	FPGA_URXD
DB9_UDSR	FPGA_UDSR
DB9_UDCD	FPGA_UDCD
DB9_UCTS	FPGA_UCTS
DB9_URI	FPGA_URI

C883 0.1 UF, C880 0.1 UF, C881 0.1 UF, C884 0.1 UF, C882 0.1 UF

R809 4.7K, R808 4.7K

FORCEON, FORCEOFF, INVALID, VCC, GND

U918 — 18.432MHZ

VDD, R655 10K, FPGA_UCLK

P3 DB9_M Silkscreen

S2, S1

DB9_URI	5
DB9_UDTR	9
DB9_UCTS	4
DB9_UTXD	8
DB9_URTS	3
DB9_URXD	7
DB9_UDSR	2
DB9_UDCD	6
	1

SW5 SW_DIP-4_SM

1	FPGA_CFG0
2	FPGA_CFG1
3	FPGA_CFG2
4	FPGA_CFG3

RP97 (4.7K)

VDD, M66EN

RP93A–RP93D / RP94A–RP94D (470OHM)

LED1_SEG0	LED2_SEG0
LED1_SEG1	LED2_SEG1
LED1_SEG2	LED2_SEG2
LED1_SEG3	LED2_SEG3
LED1_SEG4	LED2_SEG4
LED1_SEG5	LED2_SEG5
LED1_SEG6	LED2_SEG6
LED1_SEG7	LED2_SEG7

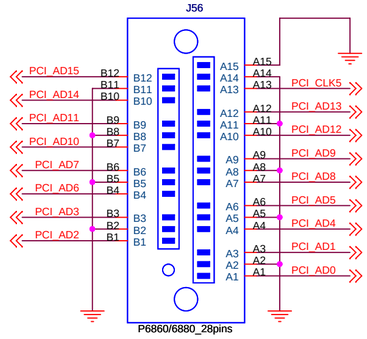
U28 — 30mA — 7-segment Display

COM1_D1, COM_2, A1, A2, B1, B2, C1, C2, D1, D2, E1, E2, F1, F2, G1, G2, DP1, DP2

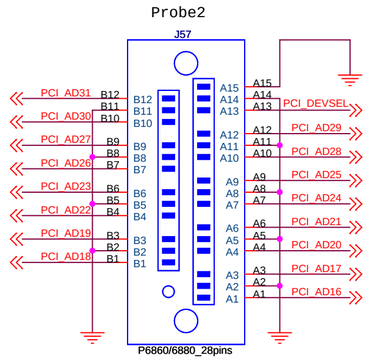
JP906 HDR_1X2_M

VDD, R810 4.7K, TP2

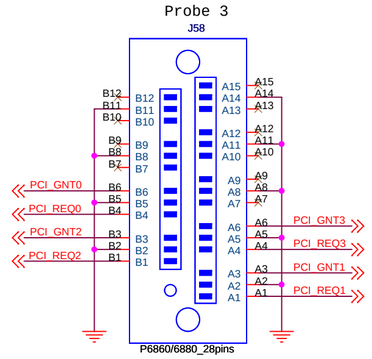
Probe 1



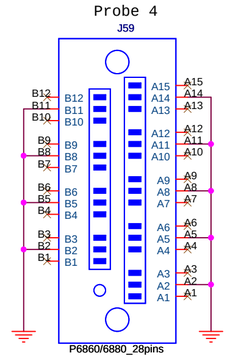
Probe2



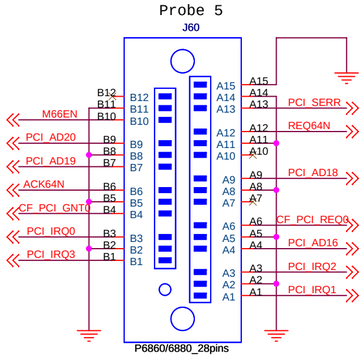
Probe 3



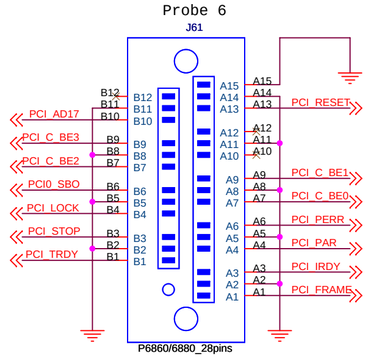
Probe 4



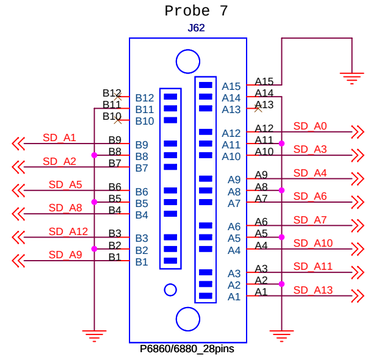
Probe 5



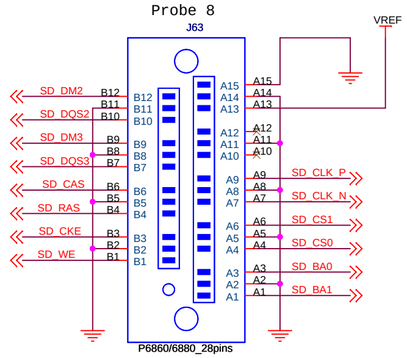
Probe 6



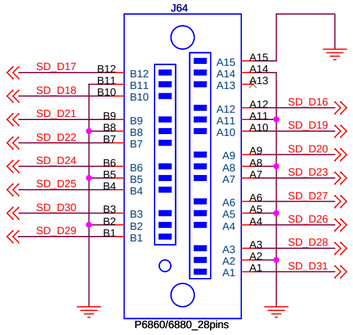
Probe 7



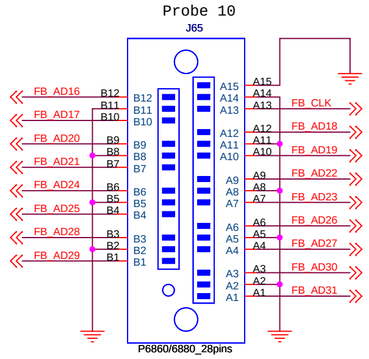
Probe 8



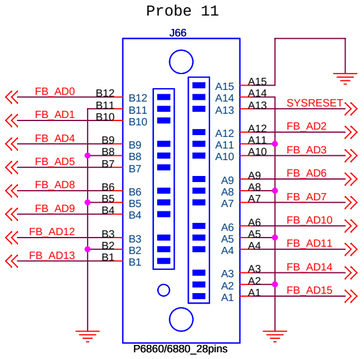
Probe 9



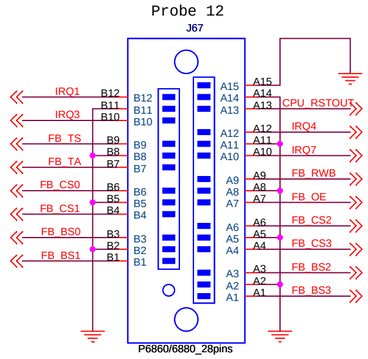
Probe 10



Probe 11



Probe 12



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Drawing Title: **M54455EVB**

Page Title: **PROBES**

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C	870012704-100	C

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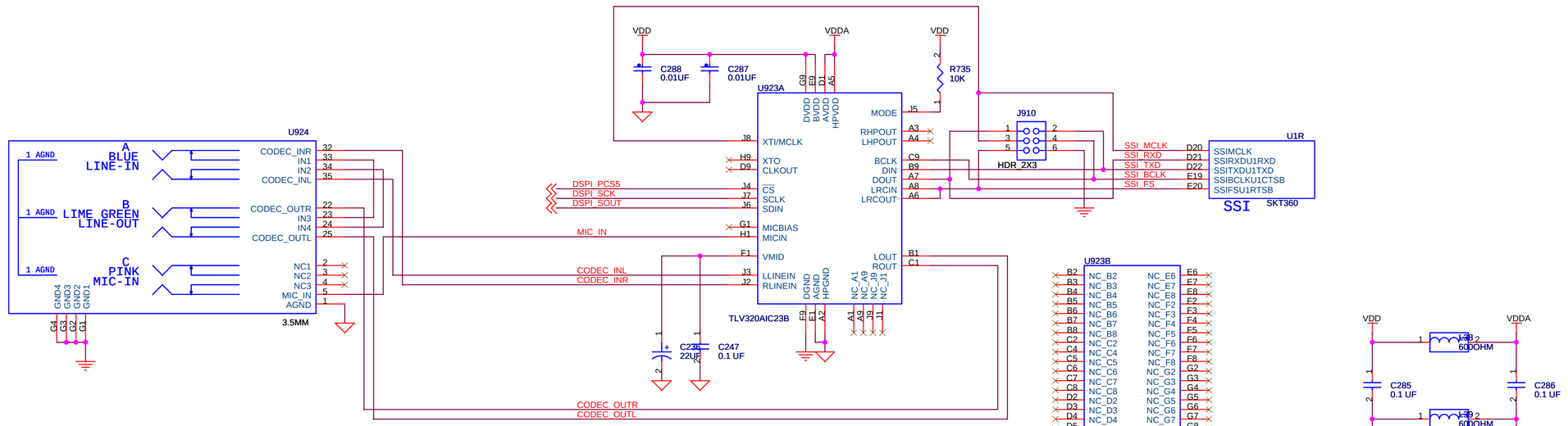
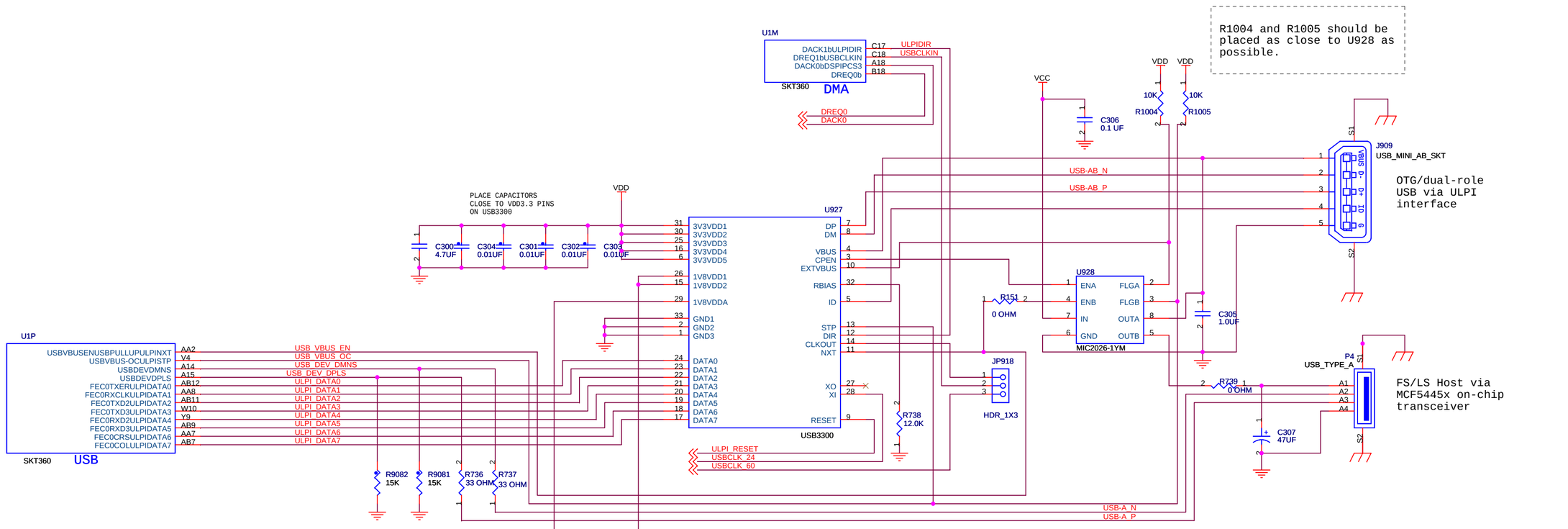


AUDIO



USB

Layout Notes:
* The required 33 ohm series source termination resistors should be placed as closely to the USB_DEV_DMNS and USB_DEV_DPLS outputs as possible.
* Route D- and D+ signals on the top or bottom layer of the board keeping them as short as possible with a minimum amount of vias and corners.
* Use 45deg turns instead of 90deg turns.
* The trace width and spacing of the D- and D+ signals should be such that the differential impedance is 90 Ohms.
* Maintain the parallelism (skew matching) between D- and D+. These traces should be the same overall length.

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Drawing Title: **M54455EVB**

Page Title: **AUDIO AND USB**

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P&E Microcomputer Systems
USB ColdFire Multilink BDM Interface

CF_RESET
BDM_RESET

CF_TEA
FB_TA

CF_DSO
DSO

CF_FREEZE
TCLK_PSTCLK

CF_DSCLK
DSCLK

CF_BKPT
BKPT

PST0
PSTDDATA0

PST1
PSTDDATA1

PST2
PSTDDATA2

PST3
PSTDDATA3

CF_DSI
DSI

EXTERNAL_DSI
EXTERNAL_DSI

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Drawing Title:
P&E CONFIDENTIAL INFORMATION

Page Title:
USB TO BDM COLDFIRE REFERENCE DESIGN

Size	Document Number	Rev
C	PDF: SPF-22131 SOURCE: SCH-22131	C

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