DWG. NO.	SH.	REV
LPCX5411x QFP64	1	B

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	- Chng R19 to 4.12ohm; sht 3. - Chng JS10 to R80 4.12ohm; sht 3. - Add hdr & shunt at JP3; sht 3. - Add JS28, JS29, JS30; sht 2.	04/20/2015	
A1	- Chng C8 to 2.2uF; sht 3.	05/06/2015	
B	- Chng U2 to PESD3V3L5UY; sht 2. - Add C66 - C72 decoupling, sht 1	06/18/2017	

+2.5V_LINK
Fanout_TP Z4
Fanout_TP Z1
GND
R52 12Kohms
R53 12Kohms
R54 12Kohms
nTRST_LINK2
SWDIO_LINK2
SWDCLK_LINK2
R65 2.2Kohms
U12
LPC4322JET100
LPC4322JET100
nTRST
STDI/TDI
TMS/SWDIO
TCK/SWDCLK
TDO/SWO
DBGEN
nRESET
VBAT
VDDREG_1
VDDREG_2
VDDREG_3
VDDIO_1
VDDIO_2
VDDA
XTAL1
XTAL2
RTCX1
RTCX2
RTC_ALARM
WAKEUP0
ADC0
ADC1
ADC2
ADC3
VSSA
VSSIO_1
VSSIO_2
VSSIO_3
VSSIO_4
VSSIO_5
VSSIO_6
ABLS2-12.000MHZ-D4Y-T
Y2
12M
C30 27pF
C31 27pF
R55 100Kohms
Fanout_TP Z7
FB1
3v3_LNK_CORE
C36 4.7uF 10v
C34 0.1uF
C35 0.01uF
C20 0.1uF
C12 0.01uF
C27 0.1uF
C29 0.1uF
SHT 4, 5
BRIDGE_SCL
BRIDGE_SDA-WAKEUP
JS3
JS2
I2C0_SCL
I2C0_SDA
C19 10uF
C28 4.7uF 10v
C26 10uF
C33 0.1uF
C32 0.01uF
U12
LPC4322JET100
LPC4322JET100
CLK0_/EXTBUS_CLK0/CLKOUT
CLK2_/EXTBUS_CLK2/CLKOUT//SDIO_CLK/I2S0_TX_MCLK/I2S1_RX_CLK
USB0_DP
USB0_DM
USB0_VBUS
USB0_ID
USB0_VDDA3V3_DRVR
USB0_VDDA3V3
USB0_RREF
USB0_VSSA_TERM
USB0_VSSA_REF
USB1_DP
USB1_DM
I2C0_SCL
I2C0_SDA
USB_DP_LINK
USB_DM_LINK
USB_VBUS_LINK
USB_ID
R72 0ohms
R58 12Kohms

Power-On LED

VDD_LPC5411x
R75 100ohms
D3
LG L29K-G2J1-24-Z
(Green)

VDD_LPC5411x
C66 0.01uF
C67 0.01uF
C68 0.01uF
C69 0.01uF
C70 0.01uF
C71 0.01uF
C72 0.01uF

Link +2.5V Power

U25
Vin Gnd Ena Vout nc
TLV70225DBVR
300mA
C53 4.7uF 10v
C64 0.1uF
C65 0.1uF
C54 4.7uF 10v
JS23

GND TP

TP1 DNI
HDR-1x02

SHT 3
EXT_VIN_TARGET
D5
D7
PMEG2005EJ

Target +3.3V Power

U24
CE VIN GND VROUT NC
XC6227C331PR-G
C58 4.7uF 10v
C59 0.1uF
C60 0.1uF
C46 4.7uF 10v
JS21
M3
JP9
HDR-1x03
VDD_LPC5411x

Target +1.8V Power

Fanout_TP Z8
U23
VIN GND ENA VOUT NC
LP5951MF-1.8
LP5951MF-1.8
+1.8REG
C55 1uF 10V
C56 0.1uF
C57 0.1uF
C45 10uF
JS20

USB_VBUS_LINK
R74 270ohms
FB3 220ohms
U21
I/O1 I/O2 GND VCC
PRTR5V0U2X
J7
SHLD1 SHLD2 SHLD3 SHLD4 SHLD5 SHLD6
VBUS D- D+ ID GND
ZX62D-B-5P8
USB_DM_LINK
USB_DP_LINK
USB_ID
C44 1uF 10V

USB Device Micro-B

LPC5411x VDD voltage select JP9

VDD = 3.3V;	2 - 3 (default)
VDD = 1.8V;	1 - 2

CONTRACT NO.		LINK2 LPC43xx
APPROVALS	DATE	**NXP** Semiconductors
DRAWN d.consiglio	6/18/2017	411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/
CHECKED		
ISSUED	06/18/17	SIZE D · FSCM NO. · DWG. NO. LPCX5411x QFP64 · REV B
		SCALE · SHEET 1 OF 06

H=8ND; V=4LA

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

U12
LPC4322JET100
LPC4322JET100

P0[0]_/GPIO0[0]/SSP1_MISO/ENET_RXD1/SGPIO0
P0[1]_/GPIO0[1]/SSP1_MOSI/ENET_TXEN/SGPIO1
P1[0]_/GPIO0[4]/CTIN_3/EXTBUS_A5
P1[1]_/GPIO0[8]/CTOUT_7/EXTBUS_A6/SGPIO8
P1[2]_/GPIO0[9]/CTOUT_6/EXTBUS_A7/SGPIO9
P1[3]_/GPIO0[10]/CTOUT_8/SGPIO10/EXTBUS_OE
P1[4]_/GPIO0[11]/CTOUT_9/SGPIO11/EXTBUS_BLS0
P1[5]_/GPIO1[8]/CTOUT_10/NC/EXTBUS_CS0
P1[6]_/GPIO1[9]/CTIN_5/NC/EXTBUS_WE
P1[7]_/GPIO1[0]/U1_DSR/CTOUT_13/EXTBUS_D0
P1[8]_/GPIO1[1]/U1_DTR/CTOUT_12/EXTBUS_D1
P1[9]_/GPIO1[2]/U1_RTS/CTOUT_11/EXTBUS_D2
P1[10]_/GPIO1[3]/U1_RI/CTOUT_14/EXTBUS_D3
P1[11]_/GPIO1[4]/U1_CTS/CTOUT_15/EXTBUS_D4
P1[12]_/GPIO1[5]/U1_DCD/NC/EXTBUS_D5
P1[13]_/GPIO1[6]/U1_TXD/NC/EXTBUS_D6
P1[14]_/GPIO1[7]/U1_RXD/NC/EXTBUS_D7
P1[15]_/GPIO0[2]/U2_TXD/SGPIO2/ENET_RXD0
P1[16]_/GPIO0[3]/U2_RXD/SGPIO3/ENET_RX_DV
P1[17]_/GPIO0[12]/U2_UCLK/NC/ENET_MDIO
P1[18]_/GPIO0[13]/U2_DIR/NC/ENET_TXD0
P1[19]_/ENET_TX_REF_CLK/SSP1_SCK/CLKOUT/I2S1_RX_SCK
P1[20]_/GPIO0[15]/SSP1_SSEL/NC/ENET_TXD1

TRACE_D0 G2
TRACE_D1 G1
SHT 3 CUR_MEAS_SEL H1
BOOT0_LED K2
BOOT1 K1
SHT 3 BRIDGE_L_MISO J1
SHT 3 BRIDGE_L_MOSI J2
TMS_SWDIO_TXEN J4
TMS_SWDIO K4
G4
NC H5
NC J5
SHT 3 BRIDGE_L_INTR-ISP1 H6
NC J7
SHT 3 BRDG_INTR-ISP1_DIR K7
TRACE_CLK H8
NC J8
TDO_SWO K8
TRACE_D2 H9
TRACE_D3 H10
TCK_SWCLK J10
JTAG_TDI K9
SHT 3 BRIDGE_L_SCK K10
SHT 3 BRIDGE_L_SSEL

U12
LPC4322JET100
LPC4322JET100

P2[0]_/SGPIO4/U0_TXD/EXTBUS_A13/USB0_PWR_EN
P2[1]_/SGPIO5/U0_RXD/EXTBUS_A12/USB0_PWR_FAULT
P2[2]_/SGPIO6/U0_UCLK/EXTBUS_A11/USB0_IND1
P2[3]_/SGPIO12/I2C1_SDA/U3_TXD/CTIN_1
P2[4]_/SGPIO13/I2C1_SCL/U3_RXD/CTIN_0
P2[5]_/SGPIO14/CTIN_2/USB1_VBUS/ADCTRIG1
P2[6]_/SGPIO7/U0_DIR/EXTBUS_A10/USB0_IND0
P2[7]_/GPIO0[7]/CTOUT_1/U3_UCLK/EXTBUS_A9
P2[8]_/SGPIO15/CTOUT_0/U3_DIR/EXTBUS_A8/GPIO5[7]
P2[9]_/GPIO1[10]/CTOUT_3/U3_BAUD3/EXTBUS_A0
P2[10]_/GPIO0[14]/CTOUT_2/U2_TXD/EXTBUS_A1
P2[11]_/GPIO1[11]/CTOUT_5/U2_RXD/EXTBUS_A2
P2[12]_/GPIO1[12]/CTOUT_4/NC/EXTBUS_A3
P2[13]_/GPIO1[13]/CTIN_4/NC/EXTBUS_A4
P3[0]_/I2S0_RX_SCK/I2S0_RX_MCLK/I2S0_TX_SCK/I2S0_TX_MCLK
P3[1]_/I2S0_TX_WS/I2S0_RX_WS/CAN0_RD/USB1_IND1/GPIO5[8]
P3[2]_/I2S0_TX_SDA/I2S0_RX_SDA/CAN0_TD/USB1_IND0/GPIO5[9]
P3[3]_/SPI_SCK/SSP0_SCK/SPIFI_SCK
P3[4]_/GPIO1[14]///SPIFI_SIO3
P3[5]_/GPIO1[15]///SPIFI_SIO2
P3[6]_/GPIO0[6]/SPI_MISO/SSP0_SSEL/SPIFI_MISO
P3[7]_//SPI_MOSI/SSP0_MISO/SPIFI_MOSI
P3[8]_/SPI_SSEL/SSP0_MOSI/SPIFI_CS

TARGET_UART_RXD G10
TARGET_UART_TXD G7
TARGET_UART_CTRL F5
NC D8
NC D9
NC D10
JTAG_RESET
JTAG_RESET_TXEN G9
BOOT_FLASH C10
BOOT2 C6
BOOT3 B10
NC E8
ISP_CTRL A9
B9
IF_DETECT R29 NC A10
1.5Kohms
NC A8
NC F7
NC G6
SHT 3 SSP0_SCK_LINK A7
B8
NC B7
NC C7
SHT 3 SSP0_MISO_LINK D7
SHT 3 SSP0_MOSI_LINK E7
SHT 3 SSP0_SSEL_LINK

U12
LPC4322JET100
LPC4322JET100

P6[0]_/I2S0_RX_MCLK///I2S0_RX_SCK
P6[1]_/GPIO3[0]/EXTBUS_nDYCS1/U0_UCLK/I2S0_RX_WS
P6[2]_/GPIO3[1]/EXTBUS_CKEOUT1/U0_DIR/I2S0_RX_SDA
P6[4]_/GPIO3[3]/CTIN_6/U0_TXD/EXTBUS_nCAS
P6[5]_/GPIO3[4]/CTOUT_6/U0_RXD/EXTBUS_nRAS
P6[9]_/GPIO3[5]/NC/NC/EXTBUS_nDYCS0
P6[11]_/GPIO3[7]/NC/NC/EXTBUS_CKEOUT0
PF[4]_/SSP1_SCK/SPIFI_CLKIN/TRACECLK///I2S_TX_MCLK/I2S_RX_MCLK

NC H7
NC G5
J9
F6
NC F9
F8
C9
NC H4

R45 2.2Kohms DNI
R43 2.2Kohms DNI
R44 2.2Kohms DNI
R42 2.2Kohms
GND

+2.5V_LINK
R51 2.2Kohms
R40 2.2Kohms
BOOT0_LED
BOOT1
BOOT2
BOOT3
R50 2.2Kohms
R71 2.2Kohms
R41 2.2Kohms
default = Not shunted M6
JP5 HDR-1x02
BOOT_FLASH
D1 LS Q976-NR-1
Short JP5 to force DFU boot
(when internal flash is programmed)
GND GND GND

Link LPC4322 Boot mode

DFU USB0 = B3:0 = 0101

+2.5V_LINK
U8
SN74AVC2T45DCTR
SN74AVC2T45DCTR
VCCA VCCB
A0 B0
A1 B1
DIR GND
TCK_SWCLK
JTAG_TDI
R47 100Kohms
R32 100ohms
R46 100ohms
VDD_TRGT_SWD
IF_TCK_SWCLK
IF_JTAG_TDI
C13 0.1uF
GND GND

VDD_LPC5411x
M1
JP2 HDR-1x03
NC
Buffer Pwr Select (JP2)
On-board Target 1 - 2 (default)
Off-board Target 2 - 3

VDD_LPC5411x
C3 0.01uF
GND
U4
VDD
R16 100Kohms
IF_TCK_SWCLK
IF_RST
IF_TDO_SWO
1Y0 1Y1 2Y0 2Y1 3Y0 3Y1 4Y0 4Y1 S
1Z NC
2Z TCK-SWDCLK_TRGT-SPIFI_IO1 SHT 4, 6
3Z nRESET_ULP SHT 4, 5, 6
4Z TDO-SWO_TRGT-SPIFI_IO2 SHT 4, 6
GND
NX3DV2567GU,115
JP1 HDR-1x02
default = Not shunted M5

U13
74LVC1T45GW
VCCA VCCB
GND DIR
A B
TDO_SWO
C14 0.1uF
R59 100Kohms
IF_TDO_SWO
GND GND

U14
74LVC1T45GW
TMS_SWDIO
C21 0.1uF
R60 100Kohms
R61 100ohms
IF_TMS_SWDIO-SPIFI_IO0

U1
74LVC1T45GW
TMS_SWDIO_TXEN
R66 2.2Kohms
C2 0.1uF
R10 100Kohms
JTAG_RESET
R11 100ohms
IF_RST
JTAG_RESET_TXEN
R12 2.2Kohms
GND

Target SWD Debug

C6 10uF
P1
FTSH-105-01-L-DV-K
IF_TMS_SWDIO-SPIFI_IO0 SHT 4, 6
IF_TCK_SWCLK
IF_TDO_SWO
IF_JTAG_TDI
IF_RST
IF_DETECT R18 0ohms
GND

U2
PESD3V3L5UY
IF_JTAG_TDI
IF_RST
IF_TDO_SWO
IF_TMS_SWDIO-SPIFI_IO0
IF_TCK_SWCLK
GND

+2.5V_LINK
U3 74LVC1G07GW
VCC
ISP_CTRL
R17 100ohms
IF_ISPEN
GND

JS28 IF_TCK_SWCLK TCK-SWDCLK_TRGT-SPIFI_IO1
JS29 IF_RST nRESET_ULP
JS30 IF_TDO_SWO TDO-SWO_TRGT-SPIFI_IO2

TRACE_CLK R30 DNI 0ohms NC
TRACE_D0 R27 DNI 0ohms NC
TRACE_D1 R26 DNI 0ohms NC
TRACE_D2 R31 DNI 0ohms NC
TRACE_D3 R28 DNI 0ohms NC

LPC-5411x Target
does not have trace.

VDD_LPC5411x
U18
74LVC1G3157GW
TARGET_UART_CTRL
P0_0-ISP_RX_FTDI SHT 5
TARGET_UART_RXD
SEL VDD
Y0 Z
Y1 GND
TO_MUX_P0_0-ISP_RX SHT 4
R67 2.2Kohms
GND

Target to debug location (JP1)
On-board Target - open (default)
Off-board Target - short

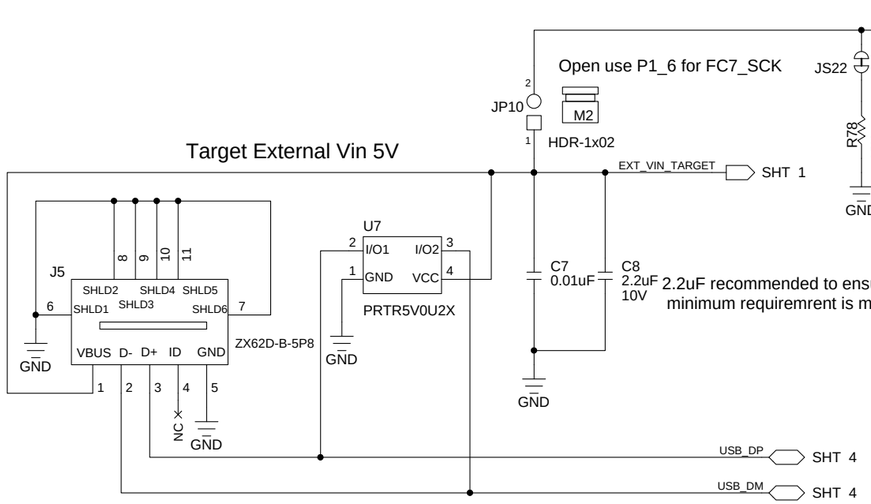
+2.5V_LINK VDD_LPC5411x
U6
74LVC1T45GW
TARGET_UART_TXD
R56 100ohms
VCCA VCCB
GND DIR
A B
C9 0.1uF
P0_1-ISP_TX SHT 4, 5
GND GND
IF_ISPEN
R13 0ohms
P0_31-PDM0_CLK-ISP0_EN SHT 4, 5, 6

CONTRACT NO.		Link2 LPC43xx Peripheral
APPROVALS	DATE	**NXP** Semiconductors
DRAWN d.consiglio	6/18/2017	411 E. Plumeria Dr
CHECKED		San Jose, CA 95134
ISSUED	06/18/17	www.standardics.nxp.com/microcontrollers/
SIZE D	FSCM NO.	DWG. NO. LPCX5411x QFP64 REV B
SCALE		SHEET 2 OF 06

H=8ND; V=4LA

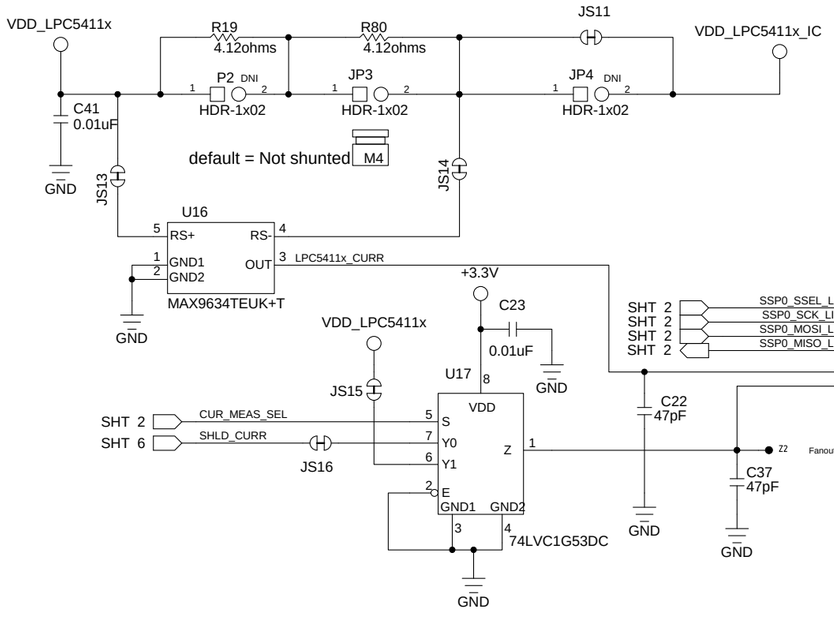
REVISIONS

REV	DESCRIPTION	DATE	APPROVED

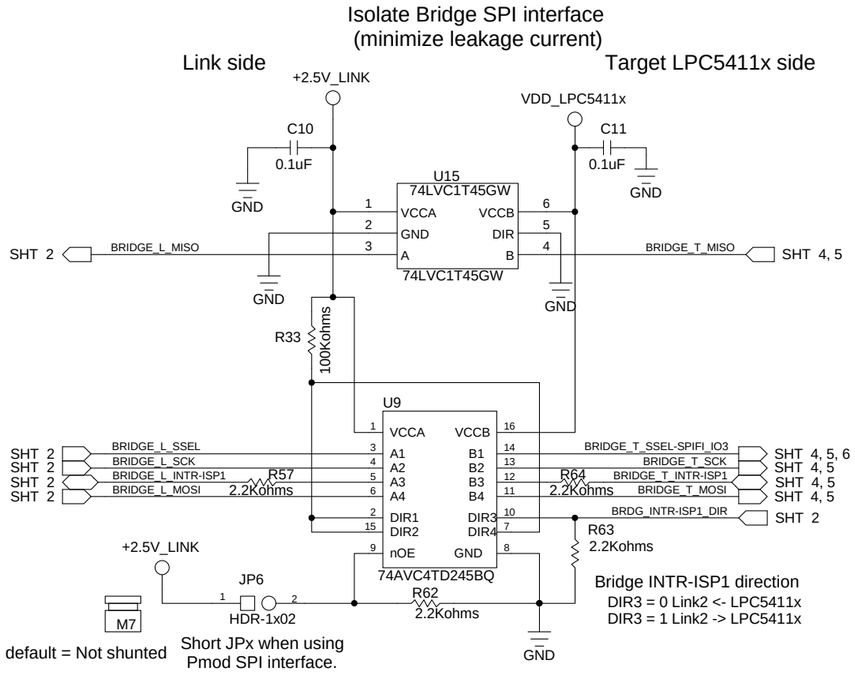


LPC5411x Current measurement				
LPC5411x				ADC111S021 12bit ADC
Vsense (1) voltage 1-lsb	JP3 open LPC5411x Current 1-lsb	JP3 shunted LPC5411x Current 1-lsb	maximum current	ADC input 1- lsb
32uV	3.88uA	7.77uA	16mA	800uV

(1) Vsense voltage is between U16 RS+ to RS-. Total Rvsense = R19 + (JS10 || JP3).



JP3 Setting		
VDD LPC5411x (volts)	JP3	Total Rvsense (ohms)
3.3V	open	8.24
1.8V	shunted	4.12



CONTRACT NO.	LPC5411x current measurement; Link2 SPI isolation transceiver
APPROVALS / DATE	**NXP** Semiconductors
DRAWN d.consiglio 6/18/2017	411 E. Plumeria Dr
CHECKED	San Jose, CA 95134
ISSUED 06/18/17	www.standardics.nxp.com/microcontrollers/
SIZE D / FSCM NO. / DWG. NO. LPCX5411x QFP64 / REV B	
SCALE	SHEET 3 OF 06

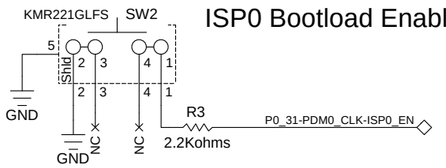
H=8ND, V=4LA

DWG. NO.	SH	REV
LPCX5411x QFP64	4	B

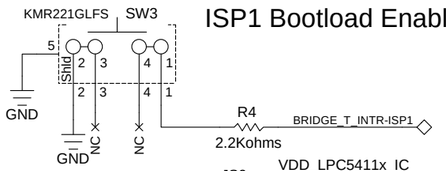
REVISIONS

REV	DESCRIPTION	DATE	APPROVED

ISP0 Bootload Enable

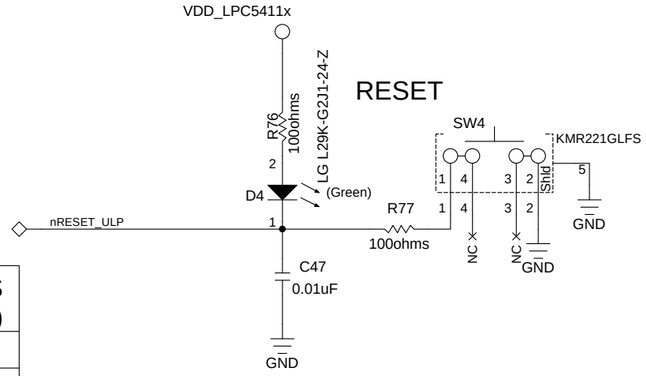


ISP1 Bootload Enable

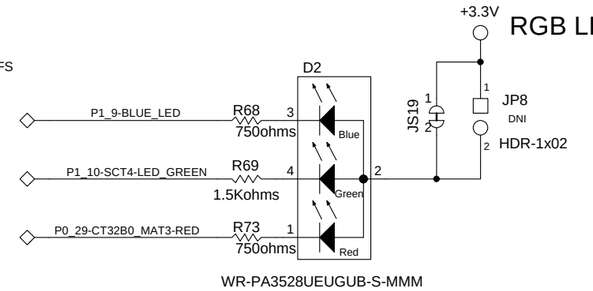


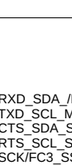
Boot Modes	ISP0 (P0.31)	ISP1 (P0.4)	VBUS (P1.6)
I2C/SPI boot	0	0	X
UART boot	0	1	0
USB MSC boot	0	1	1
FLASH boot	1	X	X

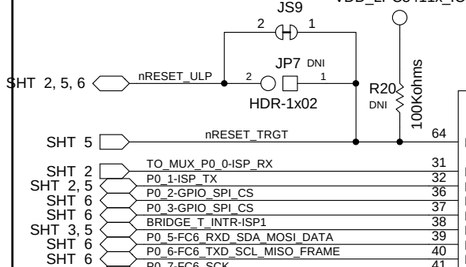
RESET



RGB LED



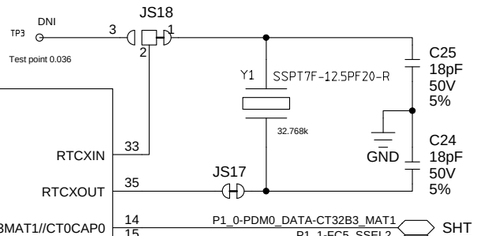




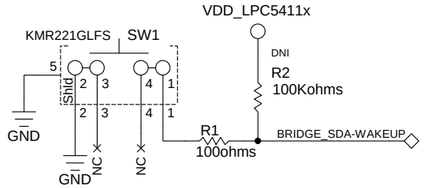
SHT 2	TO_MUX_P0_0-ISP_RX	31	
SHT 2, 5	P0_1-ISP_TX	32	
SHT 6	P0_2-GPIO_SPI_CS	36	
SHT 6	P0_3-GPIO_SPI_CS	37	
SHT 3, 5	BRIDGE_T_INTR-ISP1	38	
SHT 6	P0_5-FC6_RXD_SDA_MOSI_DATA	39	
SHT 6	P0_6-FC6_TXD_SCL_MISO_FRAME	40	
SHT 6	P0_7-FC6_SCK	41	
SHT 6	P0_8-FC2_RXD_SDA_MOSI	43	
SHT 6	P0_9-FC2_TXD_SCL_MISO	44	
SHT 6	P0_10-FC2_SCK-CT32B3_MAT0	45	
SHT 6	BRIDGE_T_SCK	46	
SHT 3, 5	BRIDGE_T_MOSI	47	
SHT 3, 5	BRIDGE_T_MISO	48	
SHT 3, 5	BRIDGE_T_SSEL-SPIFI_IO3	49	
SHT 3, 5, 6	TDO-SWO_TRGT-SPIFI_IO2	50	
SHT 2, 6	TCK-SWDCLK_TRGT-SPIFI_IO1	52	
SHT 2, 6	IF_TMS_SWDIO-SPIFI_IO0	53	
SHT 2, 6	P0_18-FC5_TXD_SCL_MISO	58	
SHT 5, 6	P0_19-FC5_SCK-SPIFI_CSn	59	
SHT 5, 6	P0_20-FC5_RXD_SDA_MOSI	60	
SHT 5, 6	P0_21-CLKOUT-SPIFI_CLK	61	
SHT 6	P0_22-BRIDGE_GPIO	63	
SHT 5	BRIDGE_SCL	1	
SHT 1, 5	BRIDGE_SDA-WAKEUP	2	
SHT 1, 5	P0_25-FC4_SCLX	3	
SHT 5, 6	P0_26-FC4_SDAX	4	
SHT 5, 6	USB_DP	5	
SHT 3	USB_DM	6	
SHT 3	P0_29-CT32B0_MAT3-RED	11	
SHT 6	P0_30-ADC1	12	
SHT 6	P0_31-PDM0_CLK-ISP0_EN	13	

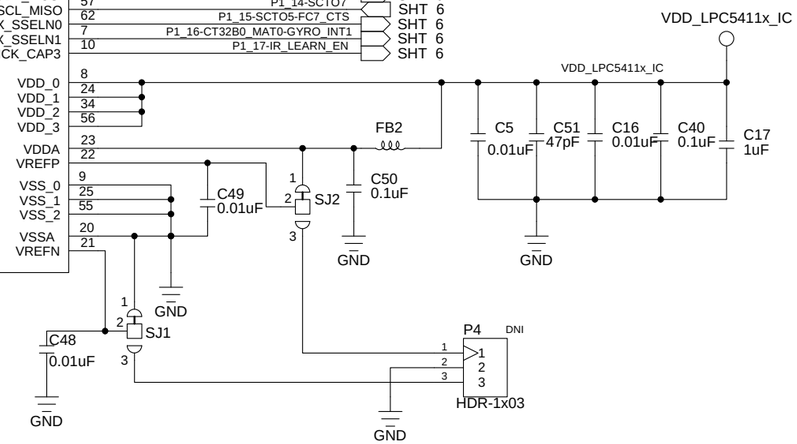
R49 33ohms
R35 33ohms

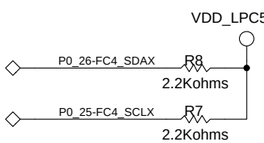
P1_0-PDM0_DATA-CT32B3_MAT1	14	SHT 6
P1_1-FC5_SSEL2	15	SHT 6
P1_2-FC5_SSEL3	16	SHT 5, 6
P1_3-FC7_SSEL2-CT32B0_CAP1	17	SHT 6
P1_4-ADC7-PDM1_CLK-FC7_RTS-FC3_TXD	18	SHT 6
P1_5-ADC8-PDM1_DAT-FC7_CTS	19	SHT 6
P1_6-FC7_SCK-USB_VBUS	26	SHT 6
P1_7-FC7_RXD_SDA_MOSI_DATA	27	SHT 3, 6
P1_8-ADC11-FC7_TXD_SCL_MISO_FRAME	28	SHT 6
P1_9-BLUE_LED	29	SHT 6
P1_10-SCT4-LED_GREEN	30	SHT 6
P1_11-FC6_RTS_SSEL1-MAG_DRDY	42	SHT 6
P1_12-CT32B1_MAT0-ACCI_INT1	51	SHT 6
P1_13-CT32B1_MAT1	54	SHT 6
P1_14-SCTO7	57	SHT 6
P1_15-SCTO5-FC7_CTS	62	SHT 6
P1_16-CT32B0_MAT0-GYRO_INT1	7	SHT 6
P1_17-IR_LEARN_EN	10	SHT 6



WAKEUP





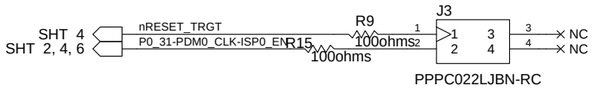


CONTRACT NO.		Target LPC5411x LQFP64	
APPROVALS	DATE	**NXP** Semiconductors	
DRAWN d.consiglio	6/18/2017	411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
CHECKED			
ISSUED	06/18/17	SIZE D / FSCM NO. / DWG. NO. LPCX5411x QFP64 / REV B	
		SCALE / SHEET 4 OF 06	

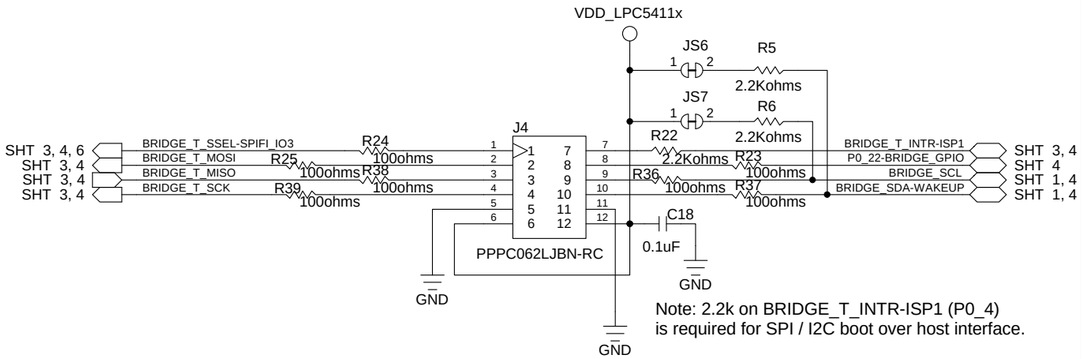
H=8N0; V=4LA

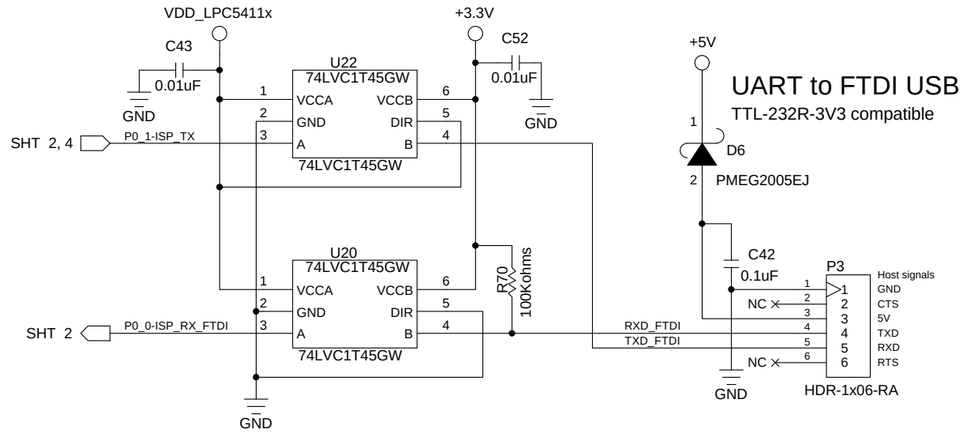
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

LPC5411x AP control port
(AP must drive open-drain)



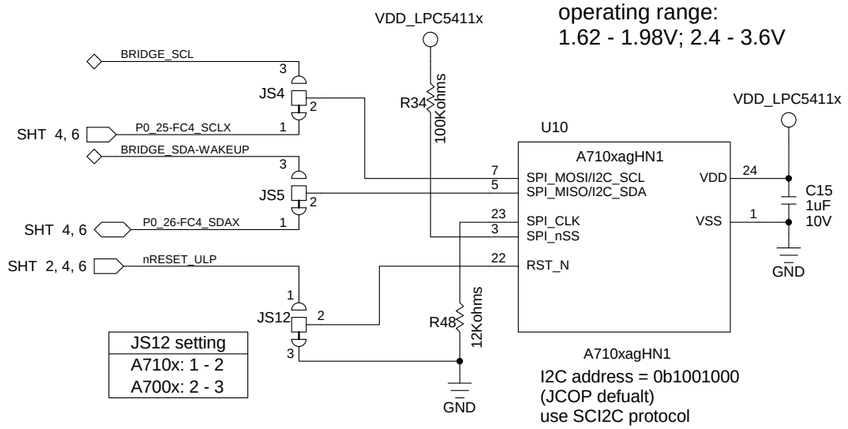
SPI / I2C bridge header (Pmod compatible)





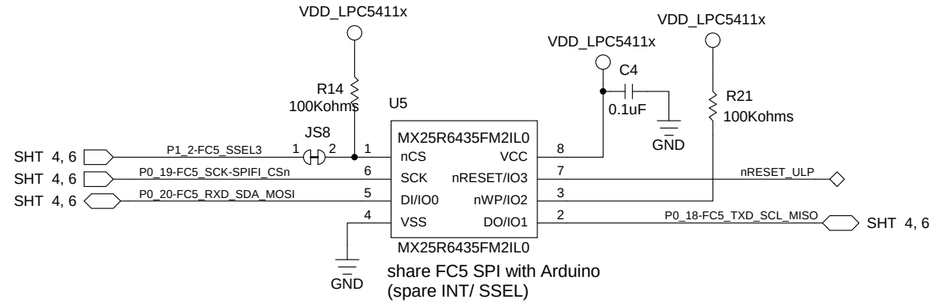
NXP A700x / A71x secure MCU

operating range:
1.62 - 1.98V; 2.4 - 3.6V



JS12 setting
A710x: 1 - 2
A700x: 2 - 3

I2C address = 0b1001000
(JCOP defualt)
use SCI2C protocol

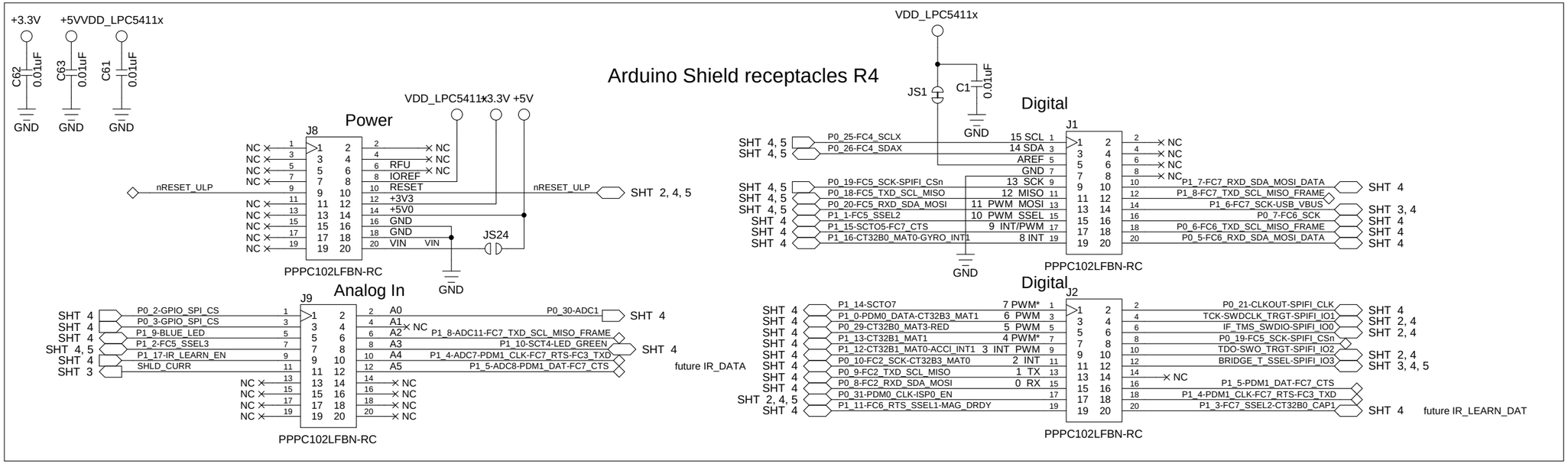


CONTRACT NO.		Pmod / FTDI / SecElem / SPI Flash	
APPROVALS	DATE	**NXP** Semiconductors 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
DRAWN d.consiglio	6/18/2017		
CHECKED			
ISSUED	06/18/17	SIZE D / FSCM NO. / DWG. NO. LPCX5411x QFP64 / REV B	
		SCALE	SHEET 5 OF 06

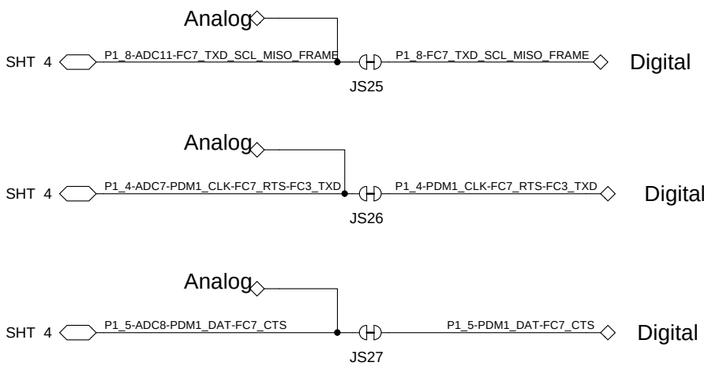
REVISIONS

REV	DESCRIPTION	DATE	APPROVED

Arduino Shield receptacles R4



Board solder jumpers
Digital function by default



CONTRACT NO.		Arduino Interface
APPROVALS	DATE	**NXP** Semiconductors
DRAWN d.consiglio	6/18/2017	411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/
CHECKED		
ISSUED	06/18/17	SIZE D | FSCM NO. | DWG. NO. LPCX5411x QFP64 | REV B
		SCALE | SHEET 6 OF 06