T2080PCIe

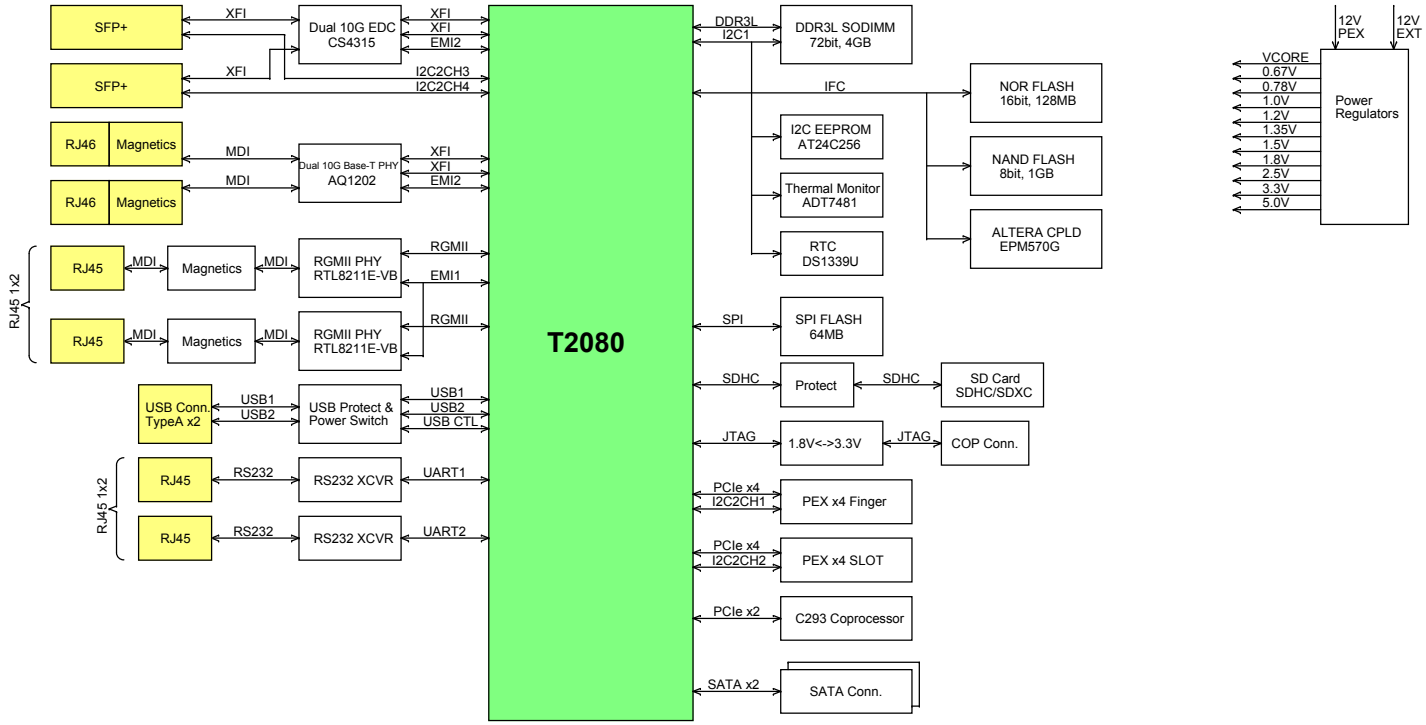
Page	Description
1	SCHEMATIC PAGE LISTING
2	SYSTEM BLOCK DIAGRAM
3	T2080 DDR3L MEMORY INTERFACE
4	T2080 IFC INTERFACE
5	T2080 NOR and NAND FLASH INTERFACE
6	T2080 SPI FLASH and SDHC INTERFACE
7	T2080 SYSTEM LOGIC INTERFACE
8	T2080 ETHERNET and SERDES INTERFACE
9	T2080 USB INTERFACE
10	T2080 DUART and I2C DEVICE INTERFACE
11	T2080 POWER SUPPLY
12	T2080 POWER SUPPLY (cont.)
13	T2080 GROUND
14	RGMII ETHERNET PORT 1
15	RGMII ETHERNET PORT 2
16	10G EDC PHY CS4315
17	SFP+ CONNECTORs
18	10G BASE-T PHY AQ1202
19	10G BASE-T PHY AQ1202 POWER SUPPLY
20	10G BASE-T RJ46 CONNECTORs
21	PCIe X4 FINGER, PCIe X4 SLOT and SATA CONNECTORs
22	C293 COPROCESSOR (part 1 of 3)
23	C293 COPROCESSOR (part 2 of 3)
24	C293 COPROCESSOR (part 3 of 3)
25	CPLD
26	SYSTEM CLOCK GENERATORs
27	SYSTEM CLOCK GENERATORs (cont.)
28	T2080 CORE POWER CONVERTOR
29	SYSTEM POWER CONVERTORs
30	SYSTEM POWER CONVERTORs (cont.)
31	SYSTEM POWER INPUT
32	MECHANICALs
33	CHANGE LIST

Version Control

Version	Date	Modifications
V0.1	2013/06	First release of Schematics
V1.0	2013/12	Released to Manufacturing
V2.0	2014/03	Change TF card socket with CD pin and move close to T2080 Add power-on 2 pin remote connector Add AQ1202 heatsink mounting hole and fan connector
V3.0	2014/04	Swap PCIe finger and PCIe slot SerDes lanes Add clock buffer for PCIe SerDes clock

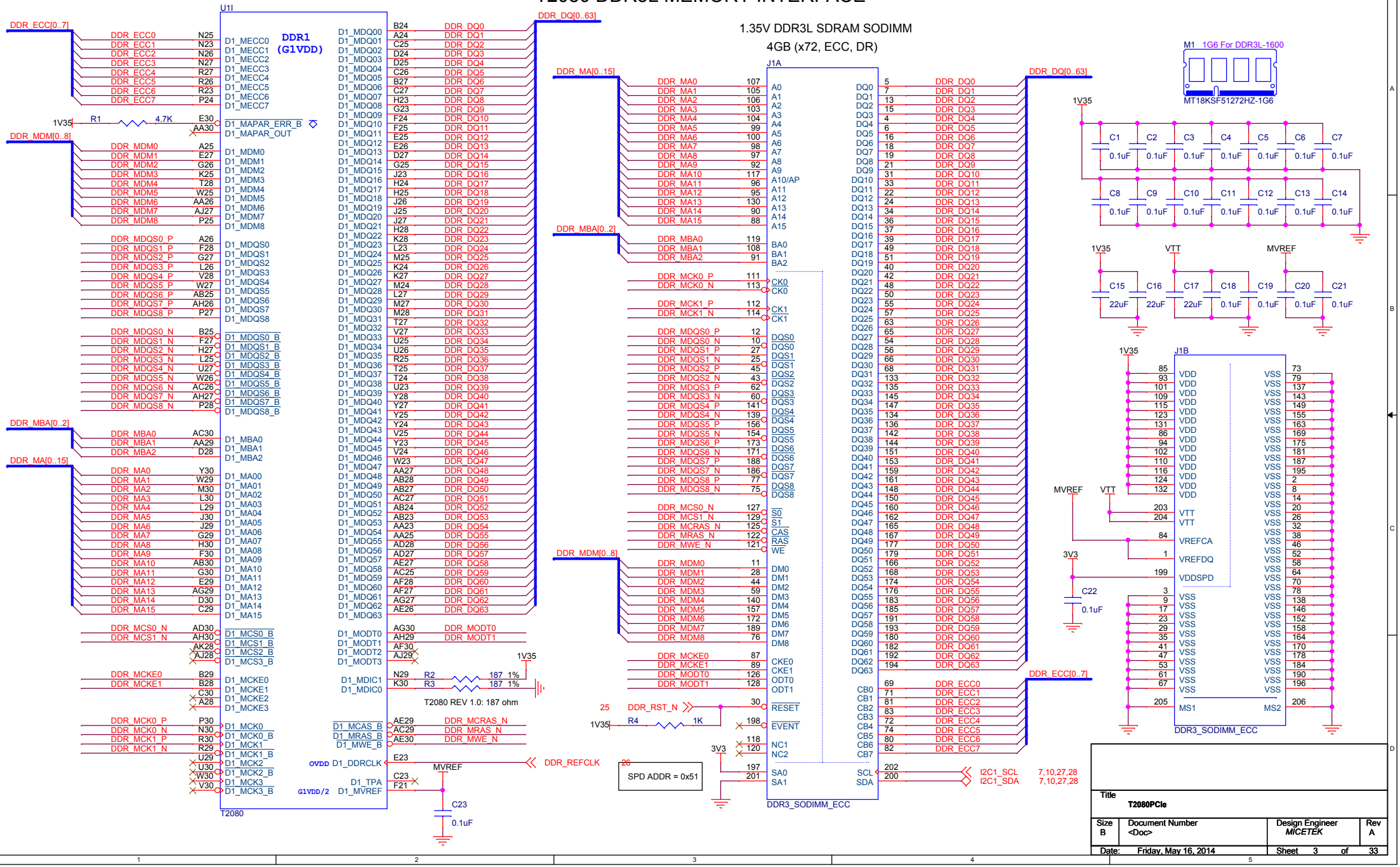
Title: T2080PCIe			
Size: B	Document Number: <Doc>	Design Engineer: *MICETEK*	Rev: A
Date: Friday, May 16, 2014		Sheet 1 of 33	

SYSTEM BLOCK DIAGRAM



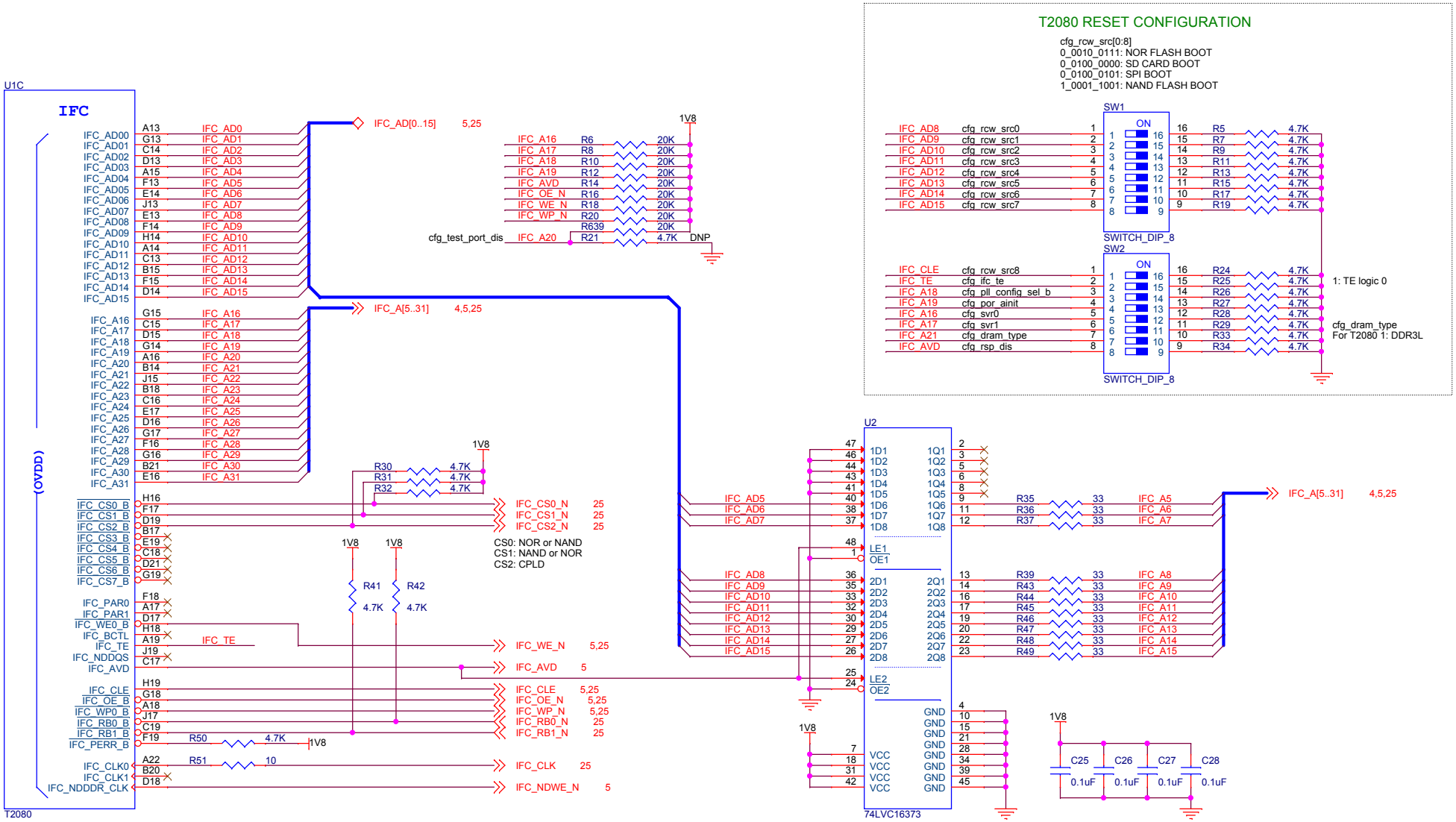
Title: T2080PCIe			
Size: B	Document Number: <Doc>	Design Engineer: *MICETEK*	Rev: A
Date: Friday, May 16, 2014		Sheet 2 of 33	

T2080 DDR3L MEMORY INTERFACE



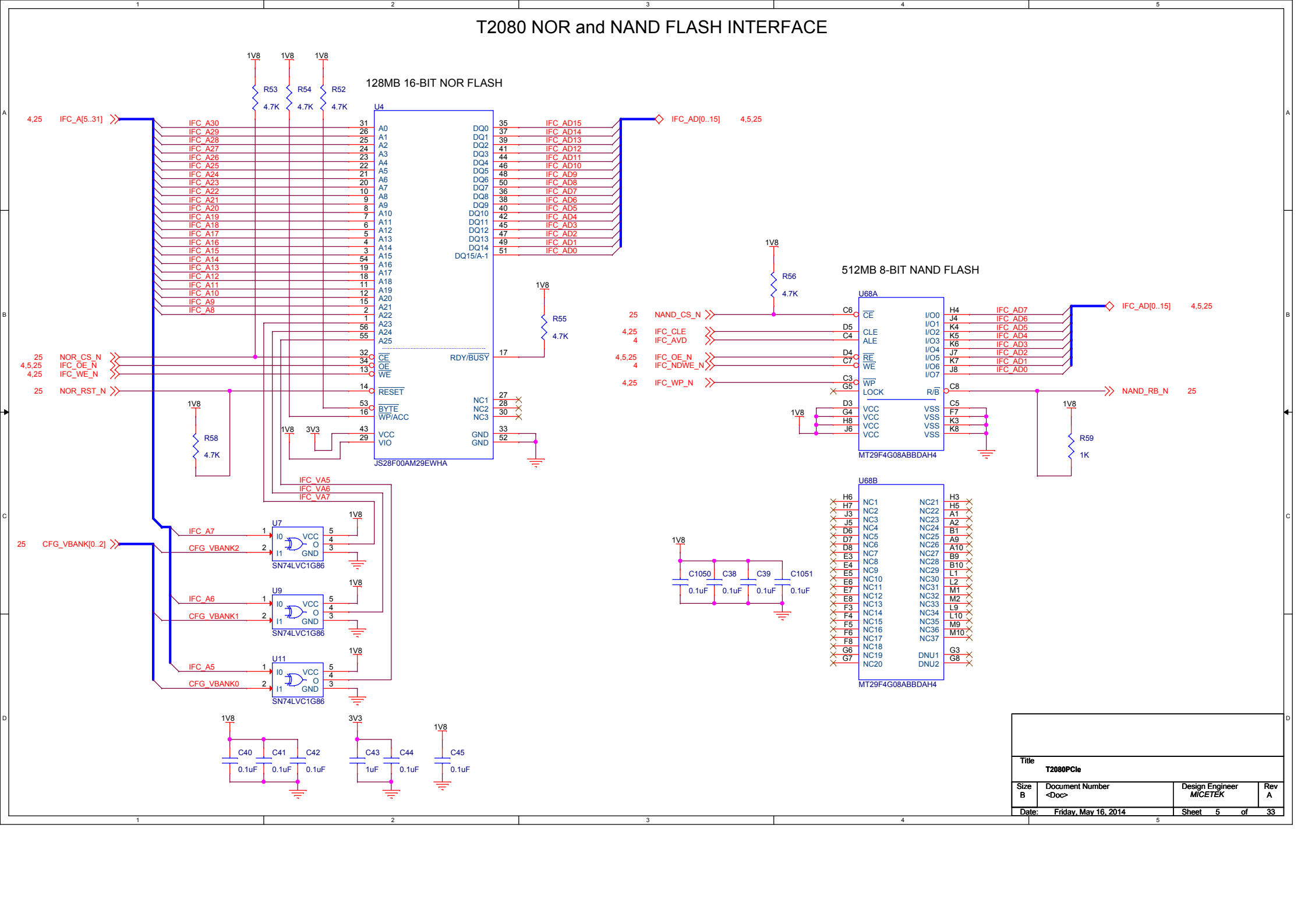
Title: T2080PCIe			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: A
Date: Friday, May 16, 2014		Sheet 3 of 33	

T2080 IFC INTERFACE



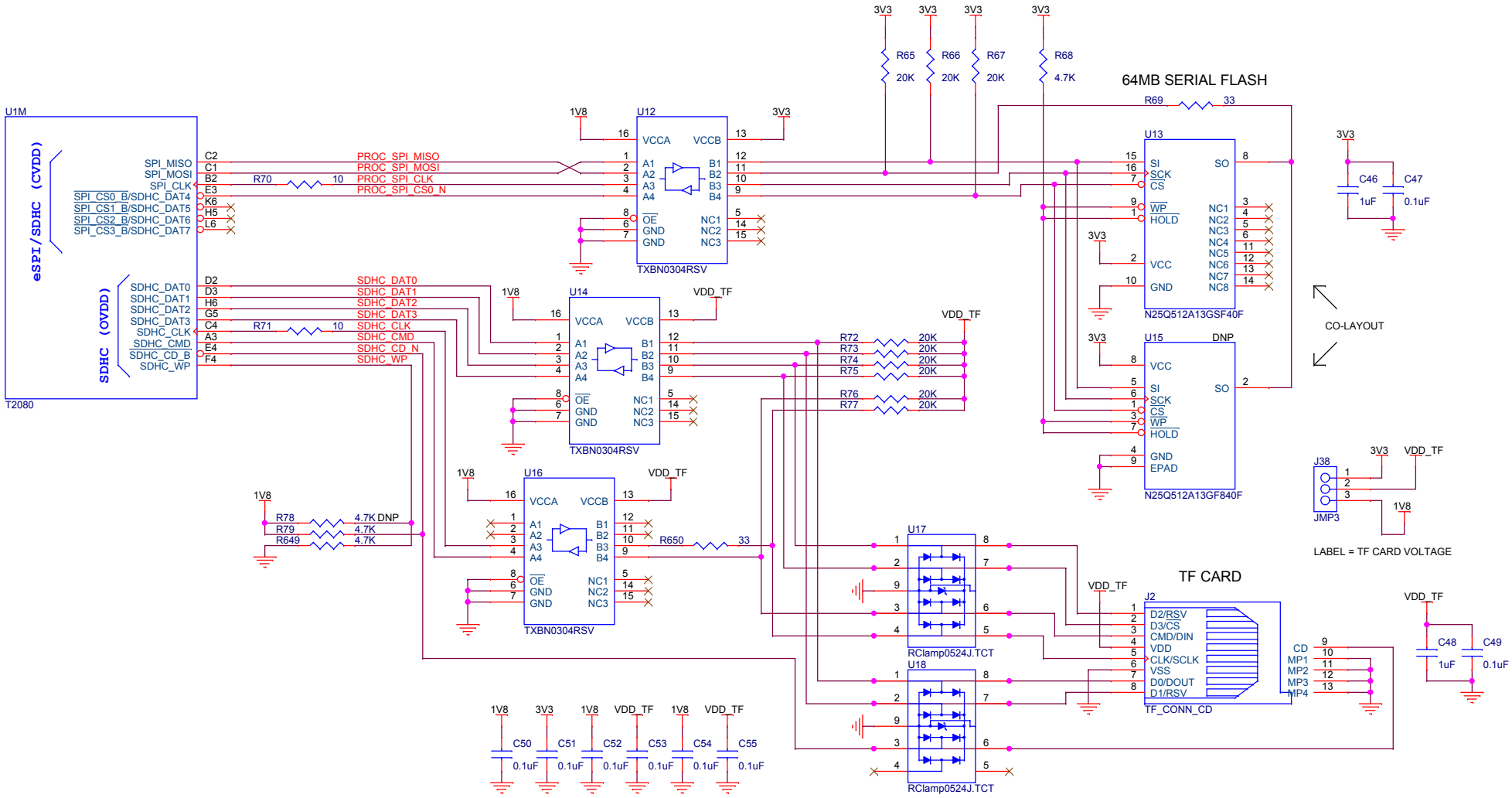
Title: T2080PCIe			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: A
Date: Friday, May 16, 2014		Sheet 4 of 33	

T2080 NOR and NAND FLASH INTERFACE



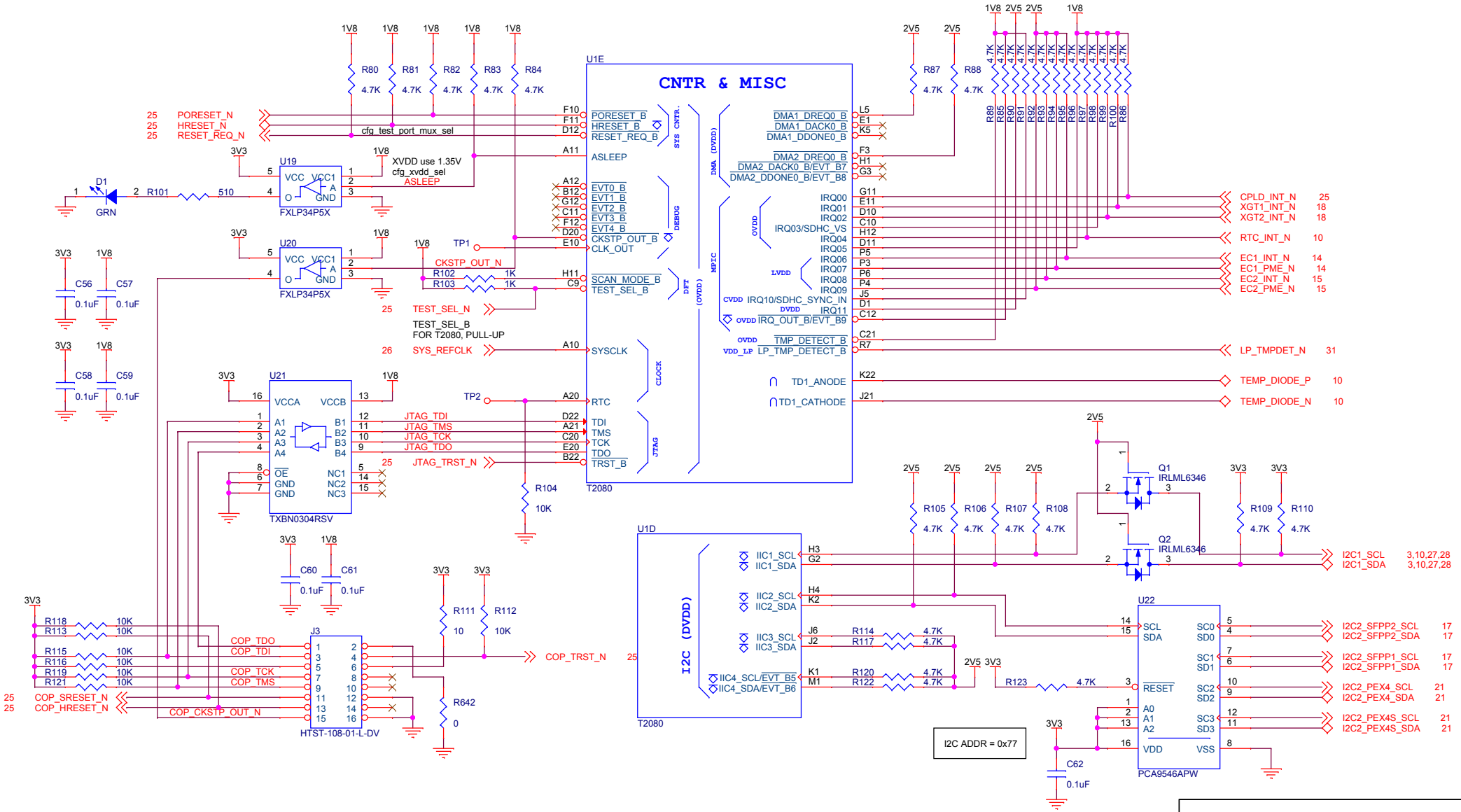
Title: T2080PCIe			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: A
Date: Friday, May 16, 2014		Sheet 5 of 33	

T2080 SPI FLASH and SDHC INTERFACE

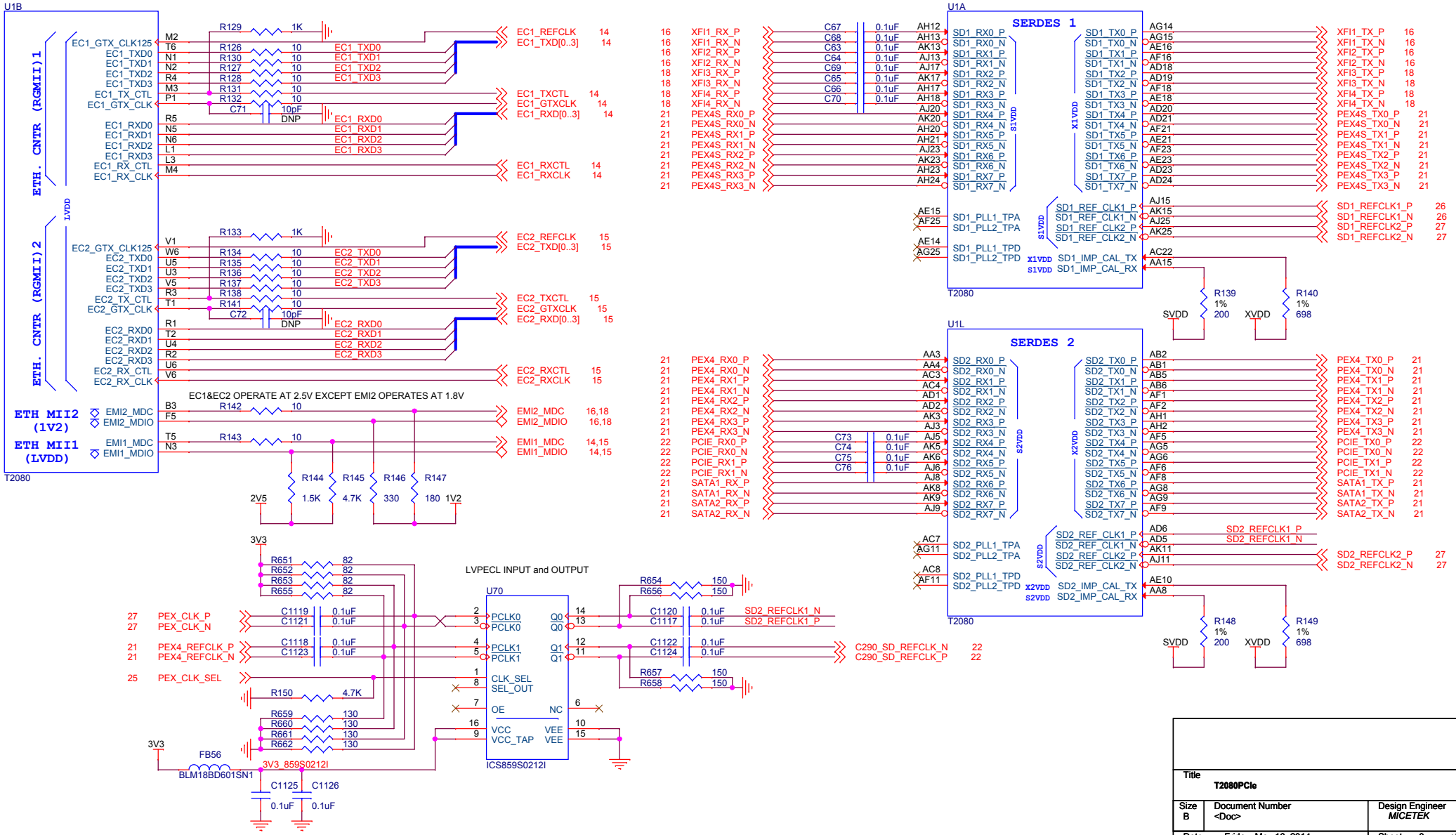


Title: T2080PCIe			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: A
Date: Friday, May 16, 2014		Sheet 6 of 33	

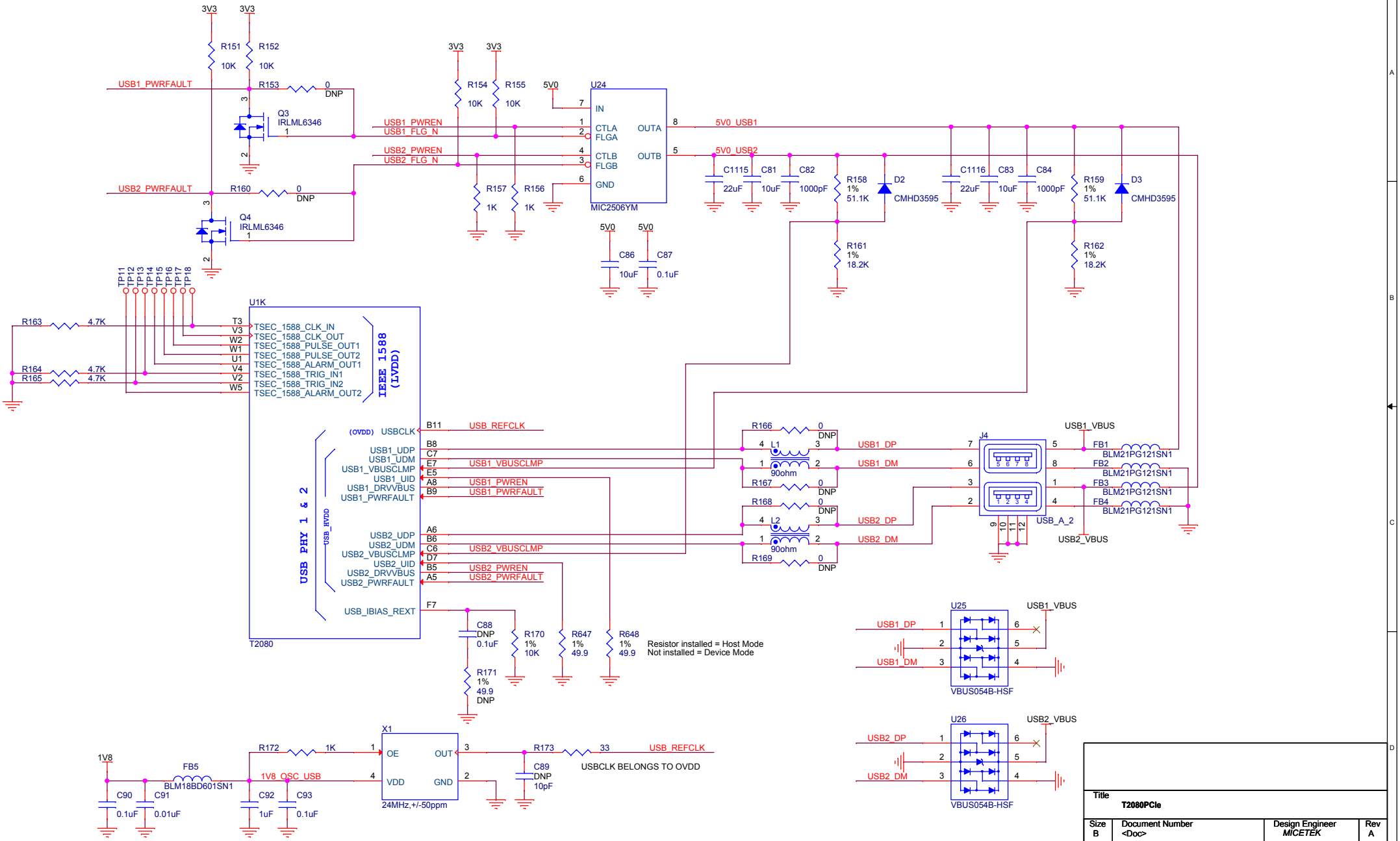
T2080 SYSTEM LOGIC INTERFACE



T2080 ETHERNET and SERDES INTERFACE

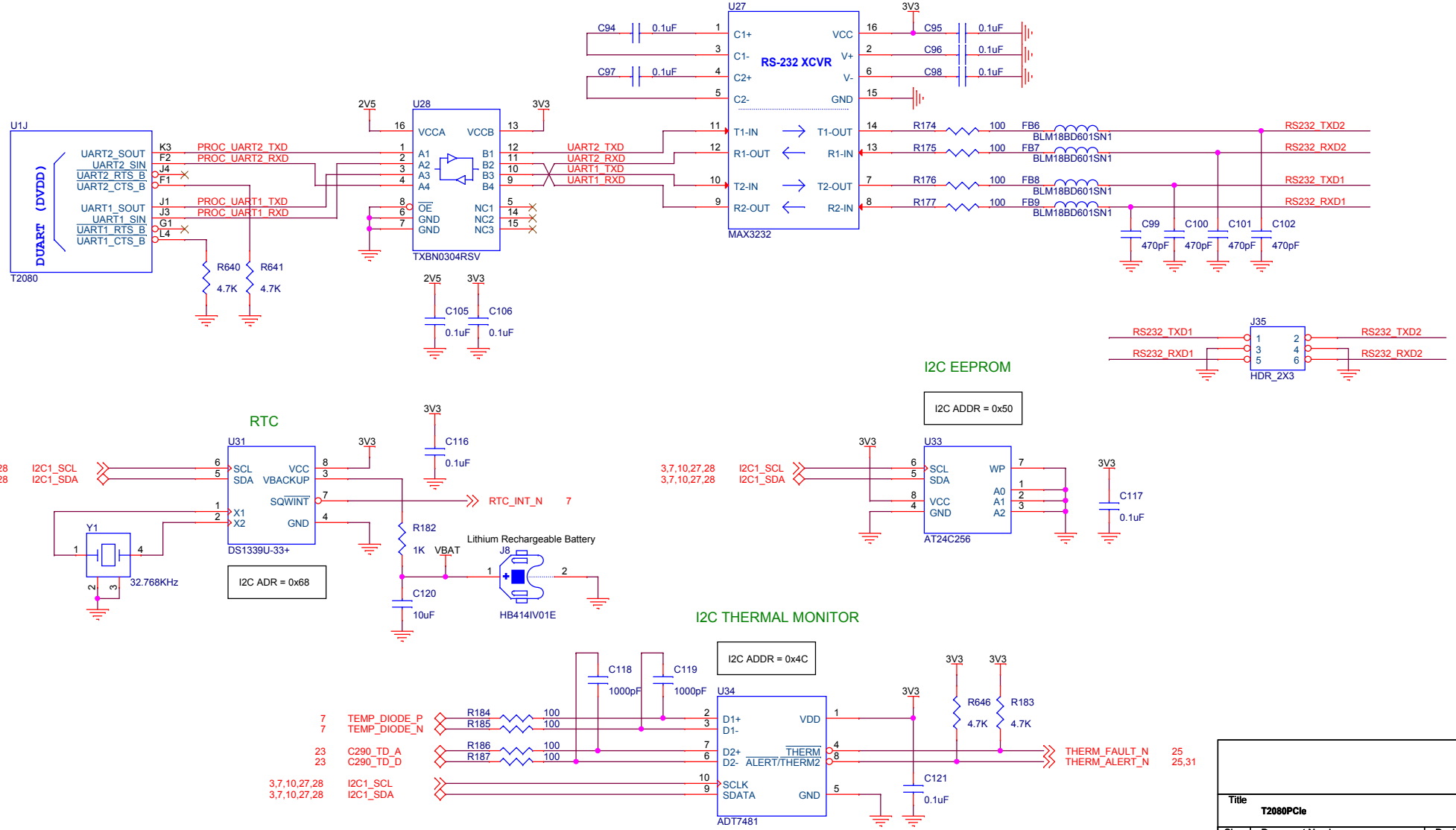


T2080 USB INTERFACE



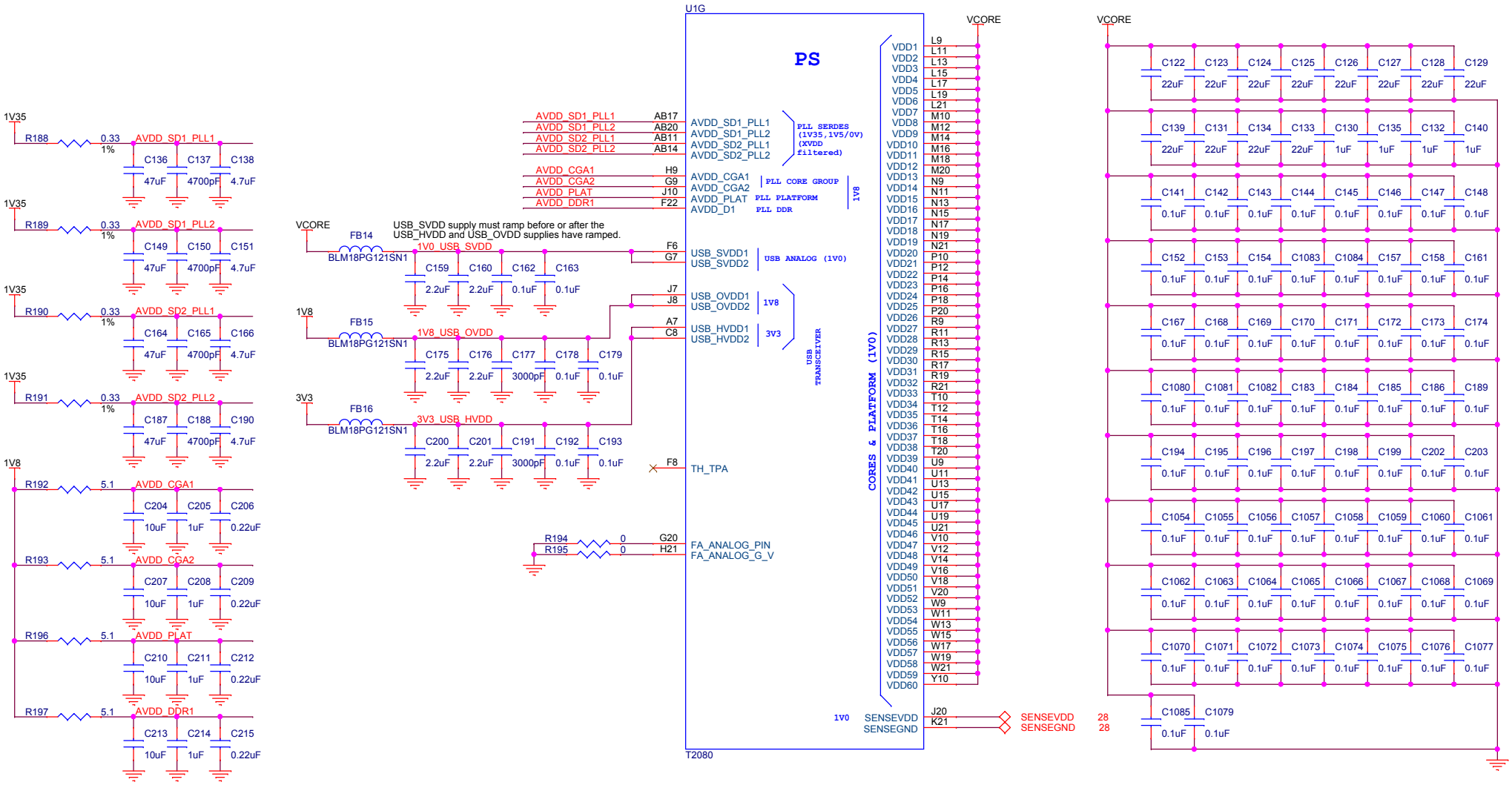
Title: T2080PCIe			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: A
Date: Friday, May 16, 2014		Sheet 9 of 33	

T2080 DUART and I2C DEVICE INTERFACE



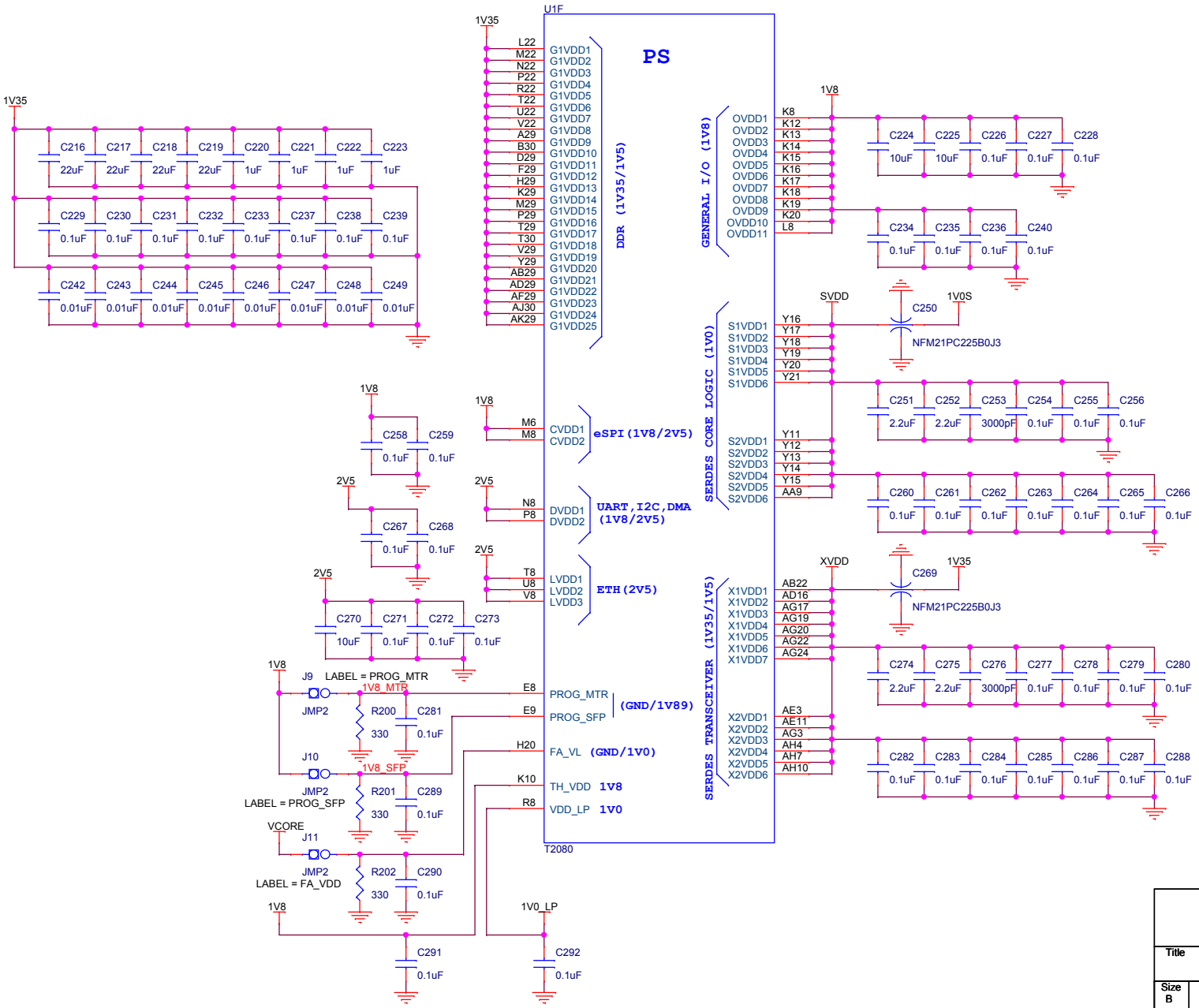
Title: T2080PCIe			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: A
Date: Friday, May 16, 2014		Sheet 10 of 33	

T2080 POWER SUPPLY



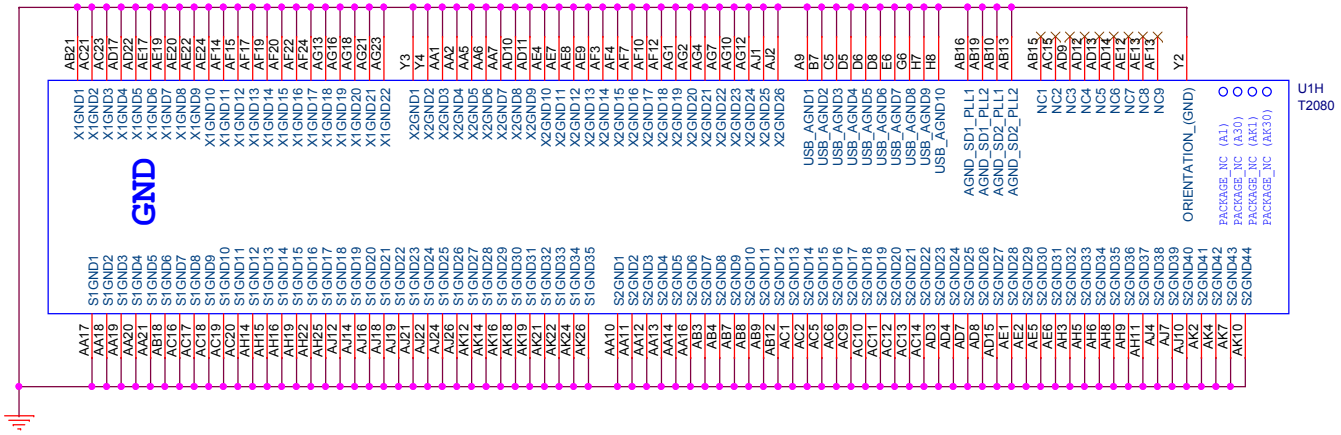
Title: T2080PCIe			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: A
Date: Friday, May 16, 2014		Sheet 11 of 33	

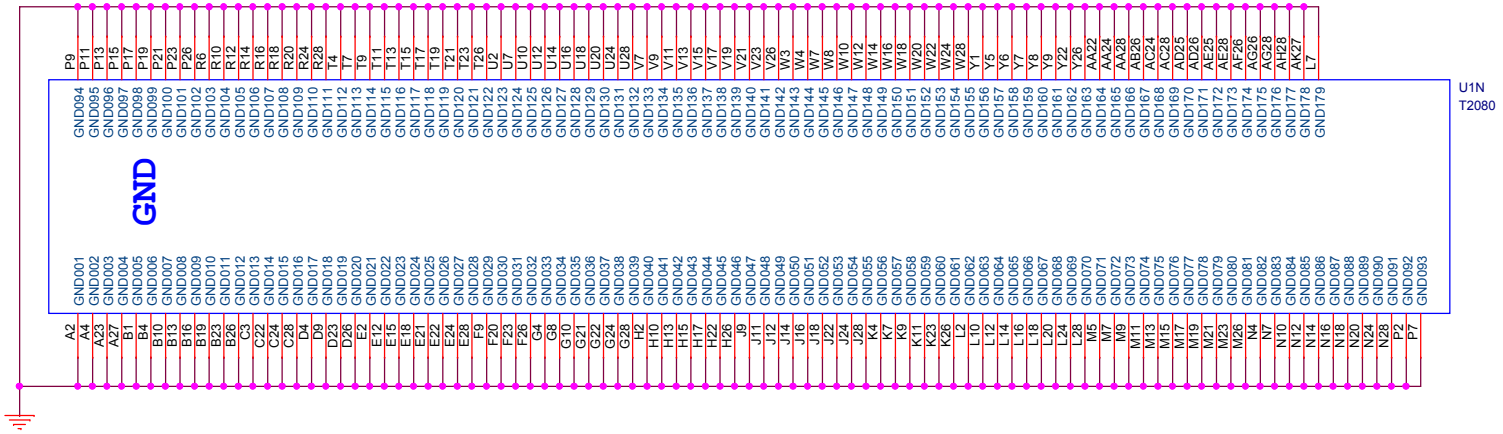
T2080 POWER SUPPLY (cont.)



Title: T2080PCIe			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: A
Date: Friday, May 16, 2014		Sheet 12 of 33	

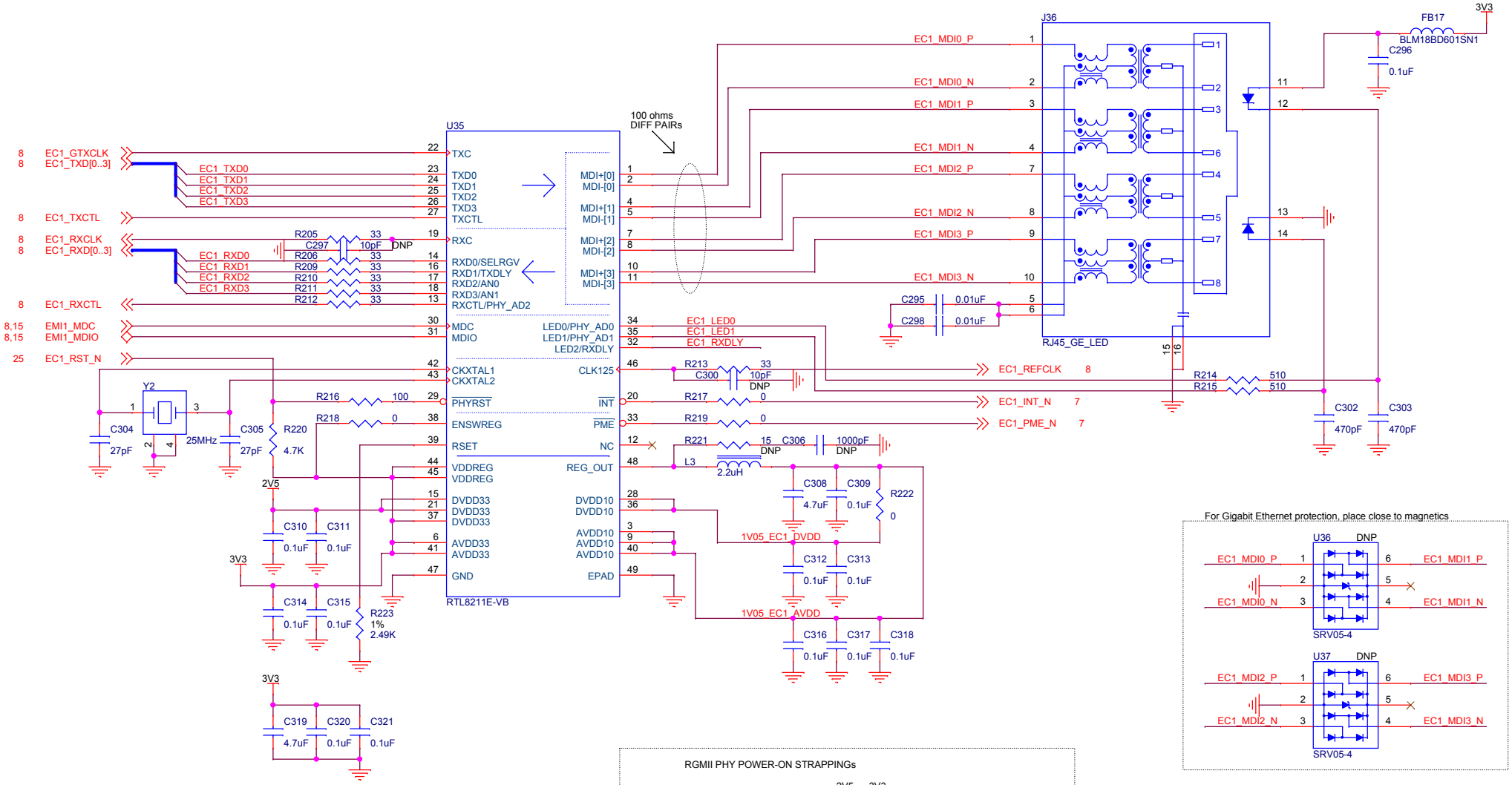
T2080 GROUND





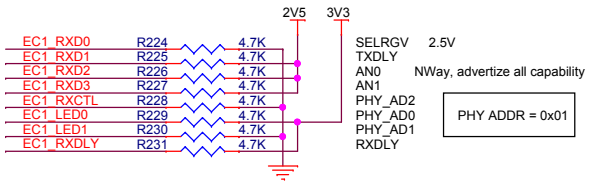
Title: T2080PCIe			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: A
Date: Friday, May 16, 2014		Sheet 13 of 33	

RGMII ETHERNET PORT 1



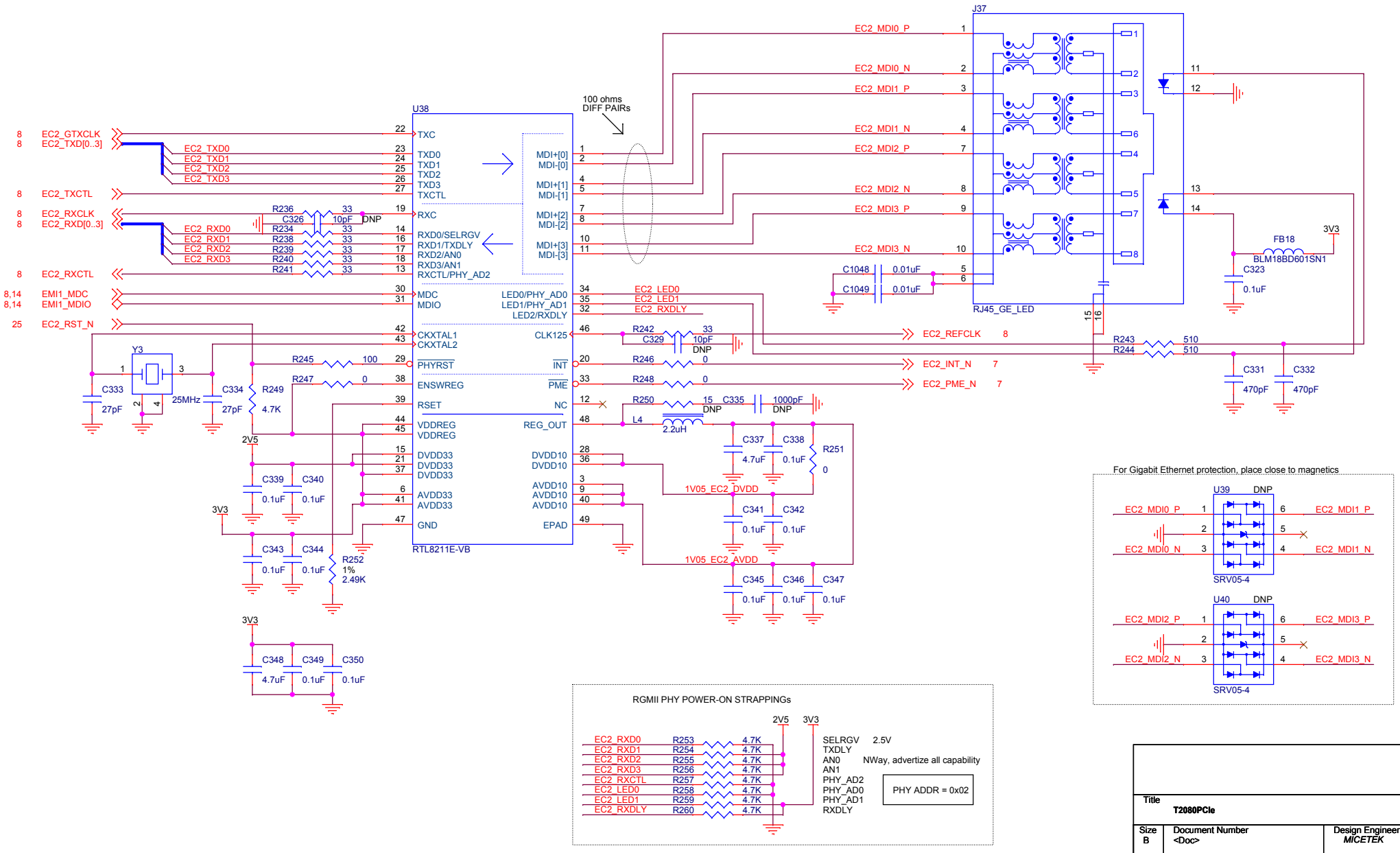
For Gigabit Ethernet protection, place close to magnetics

RGMII PHY POWER-ON STRAPPINGs



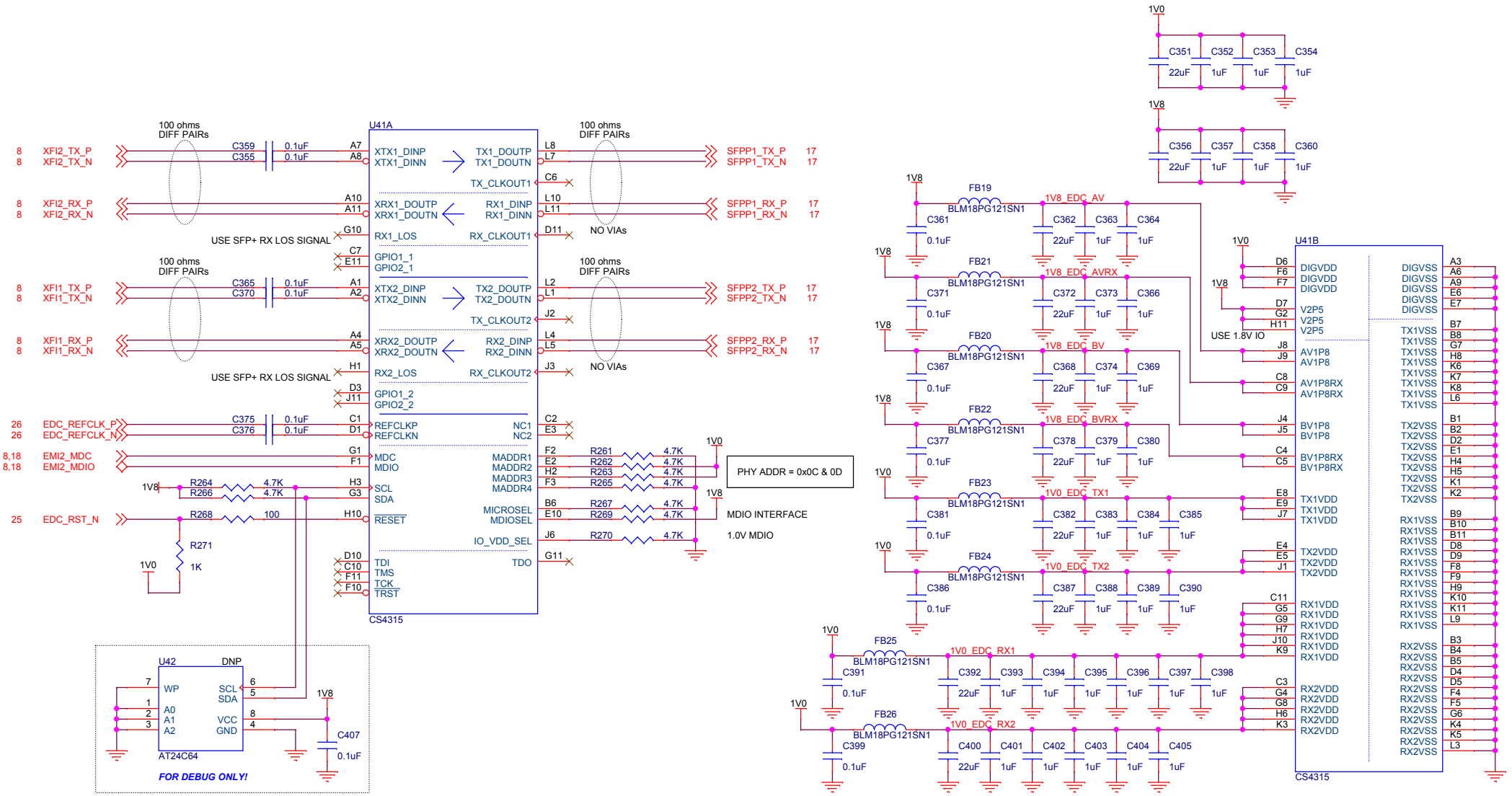
Title: T2080PCIe			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: A
Date: Friday, May 16, 2014		Sheet 14 of 33	

RGMII ETHERNET PORT 2



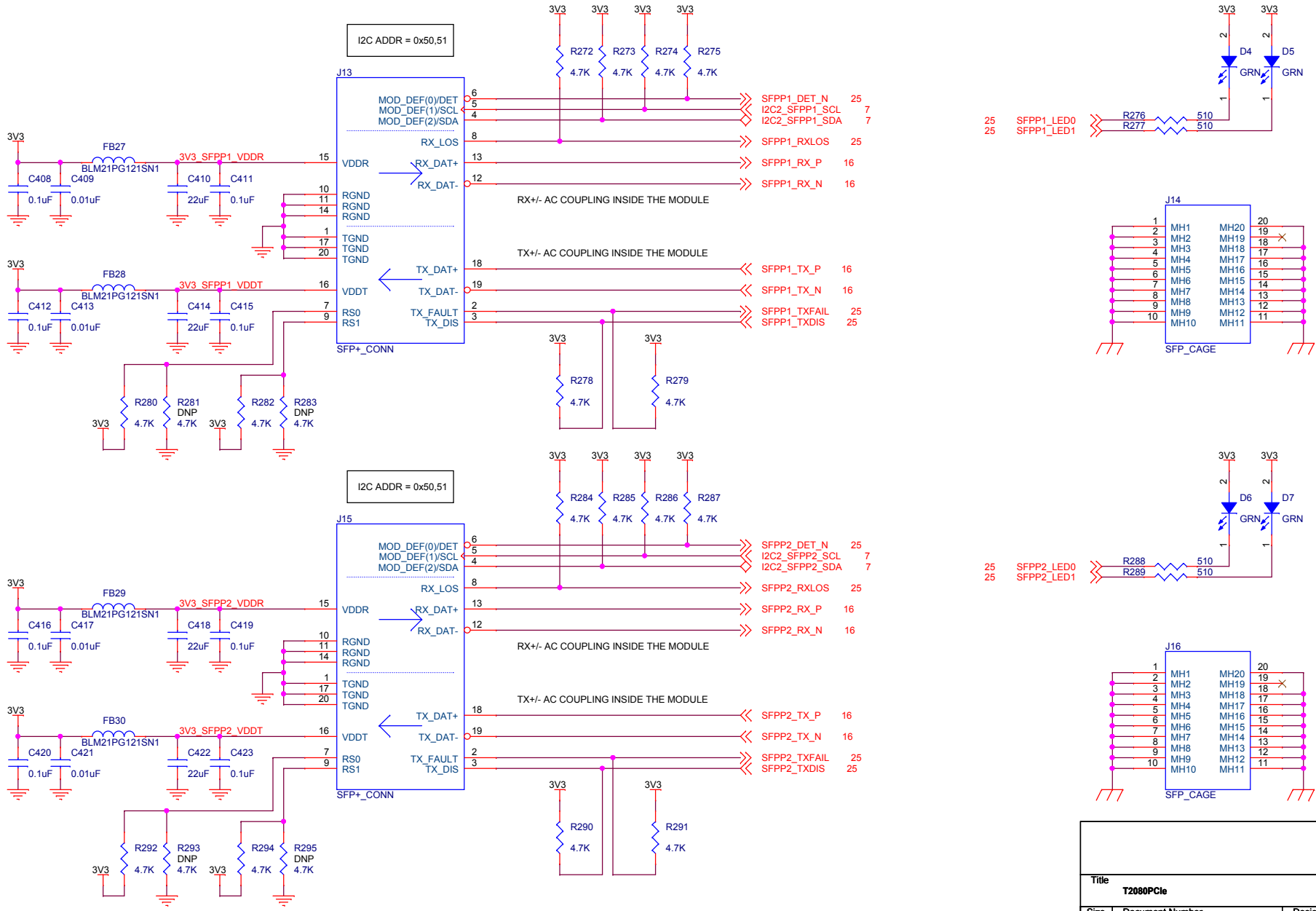
Title: T2080PCIe			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: A
Date: Friday, May 16, 2014		Sheet 15 of 33	

10G EDC PHY CS4315



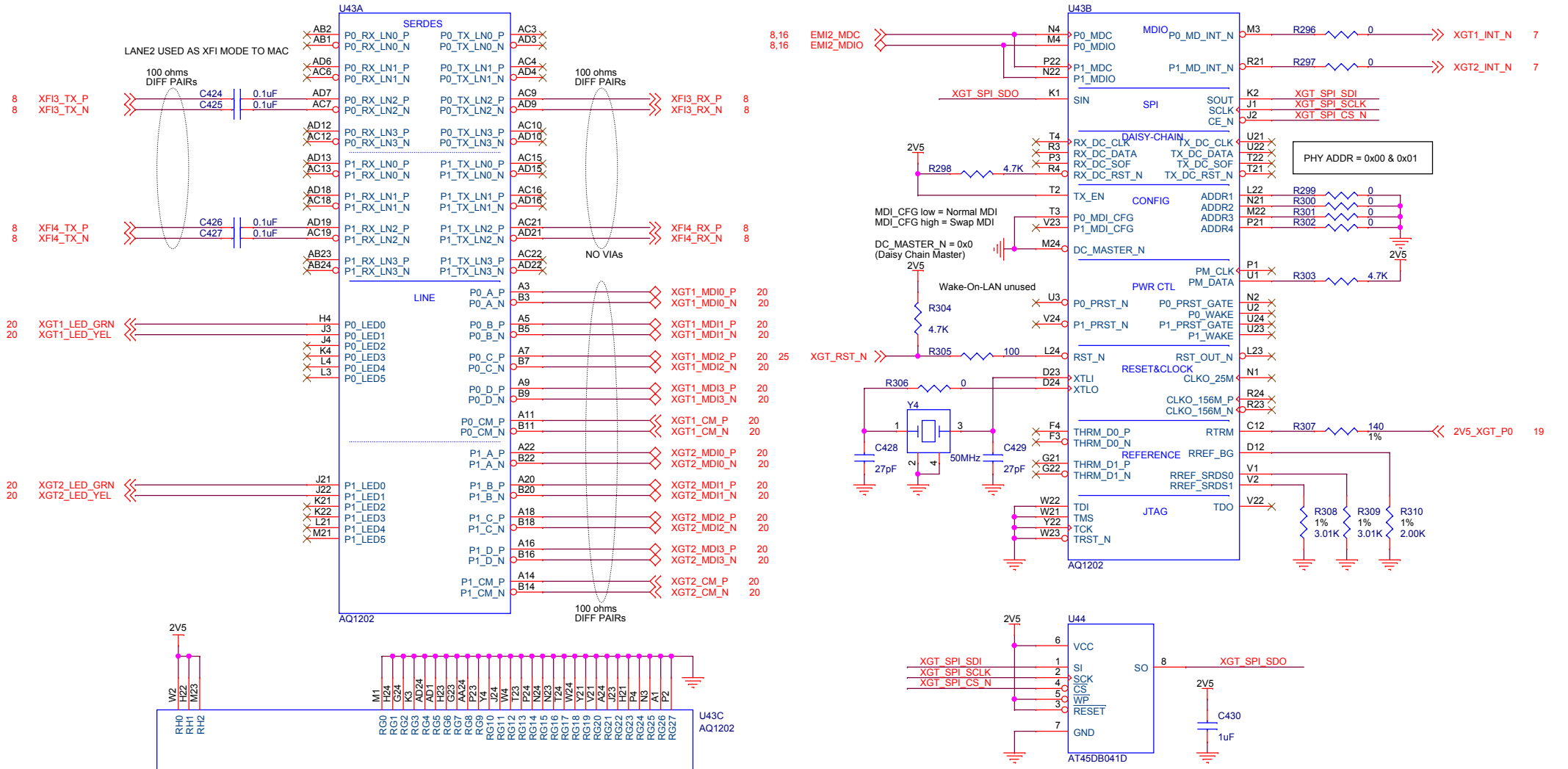
Title	T2080PCIe		
Size B	Document Number <Doc>	Design Engineer MICETEK	Rev A
Date: Friday, May 16, 2014		Sheet 16 of 33	

SFP+ CONNECTORs



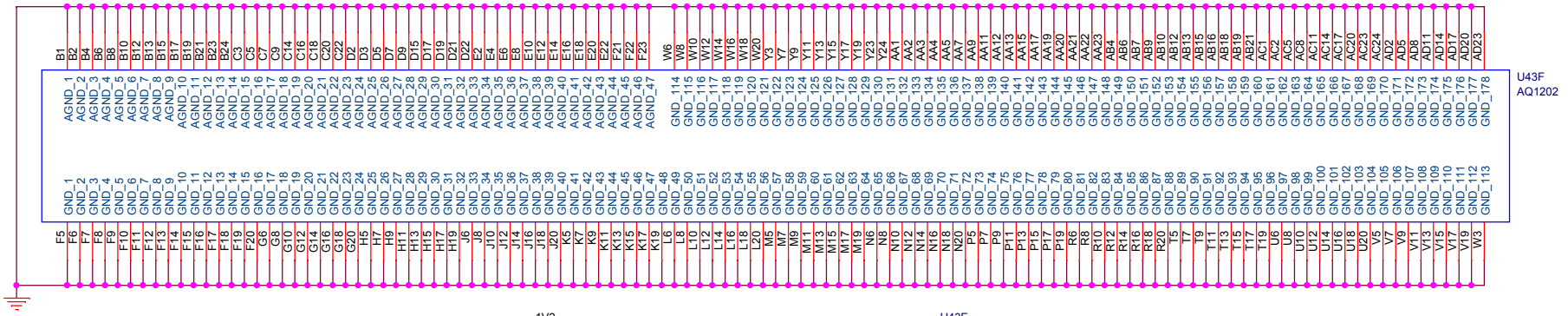
Title: T2080PCIe			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: A
Date: Friday, May 16, 2014		Sheet 17 of 33	

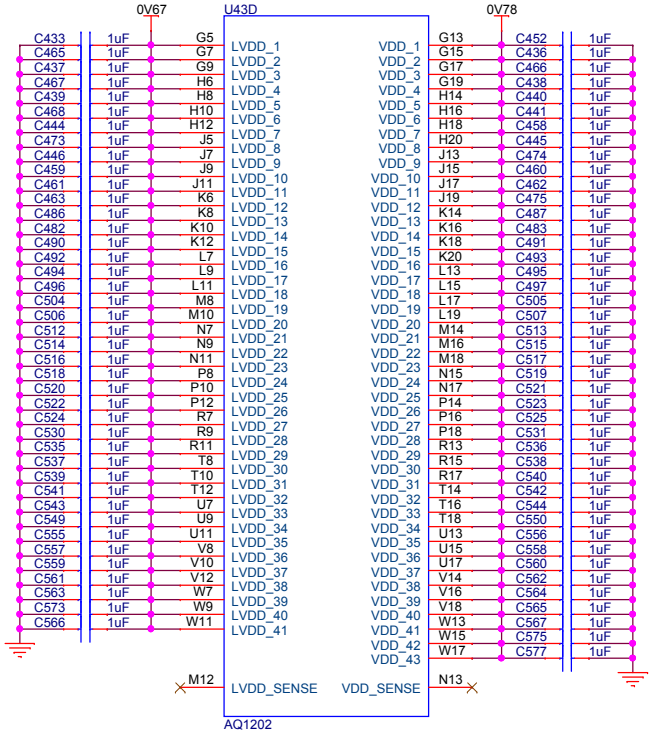
10G BASE-T PHY AQ1202

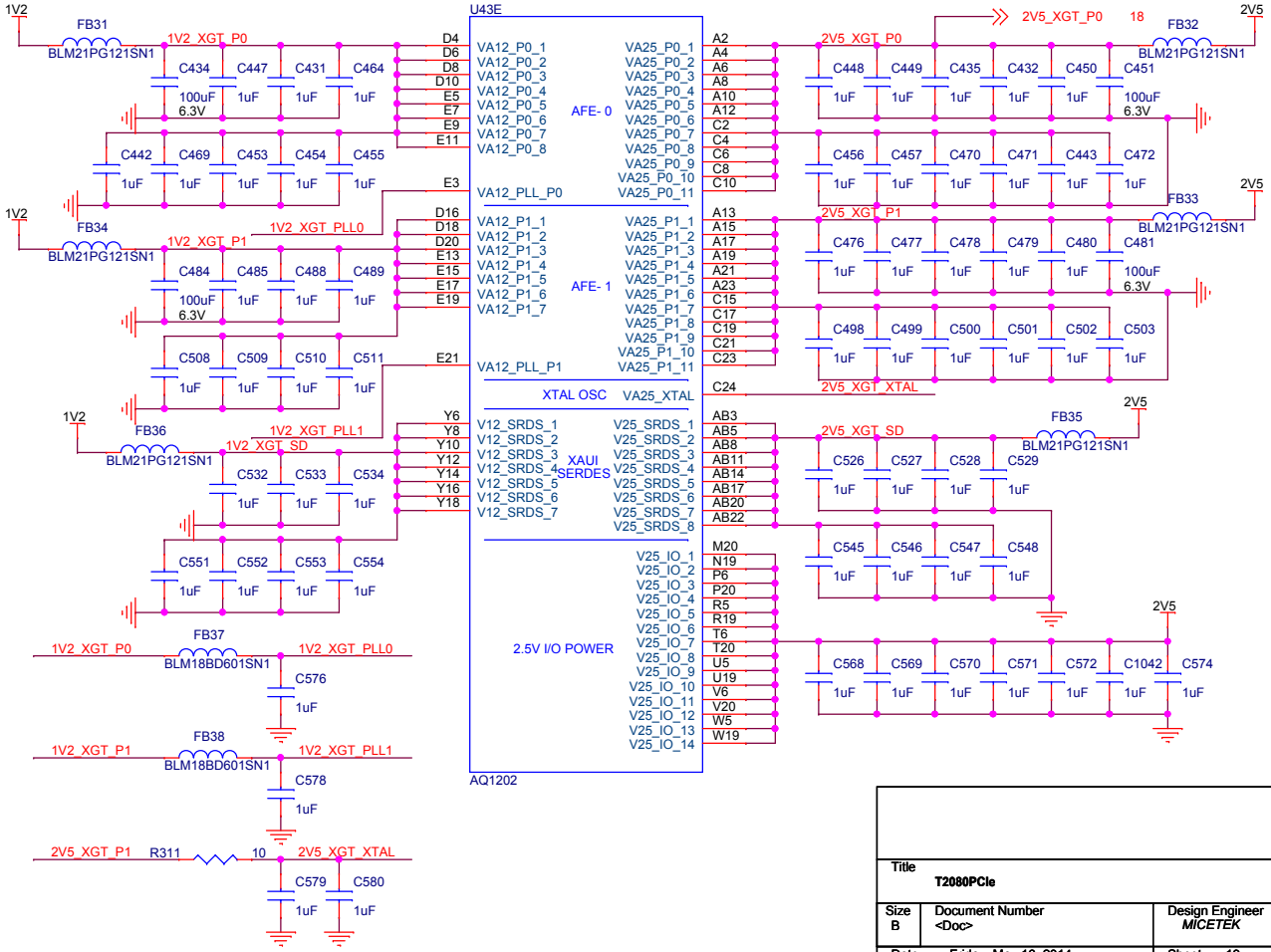


Title	T2080PCIe		
Size B	Document Number <Doc>	Design Engineer *MICETEK*	Rev A
Date: Friday, May 16, 2014		Sheet 18 of 33	

10G BASE-T PHY AQ1202 POWER SUPPLY

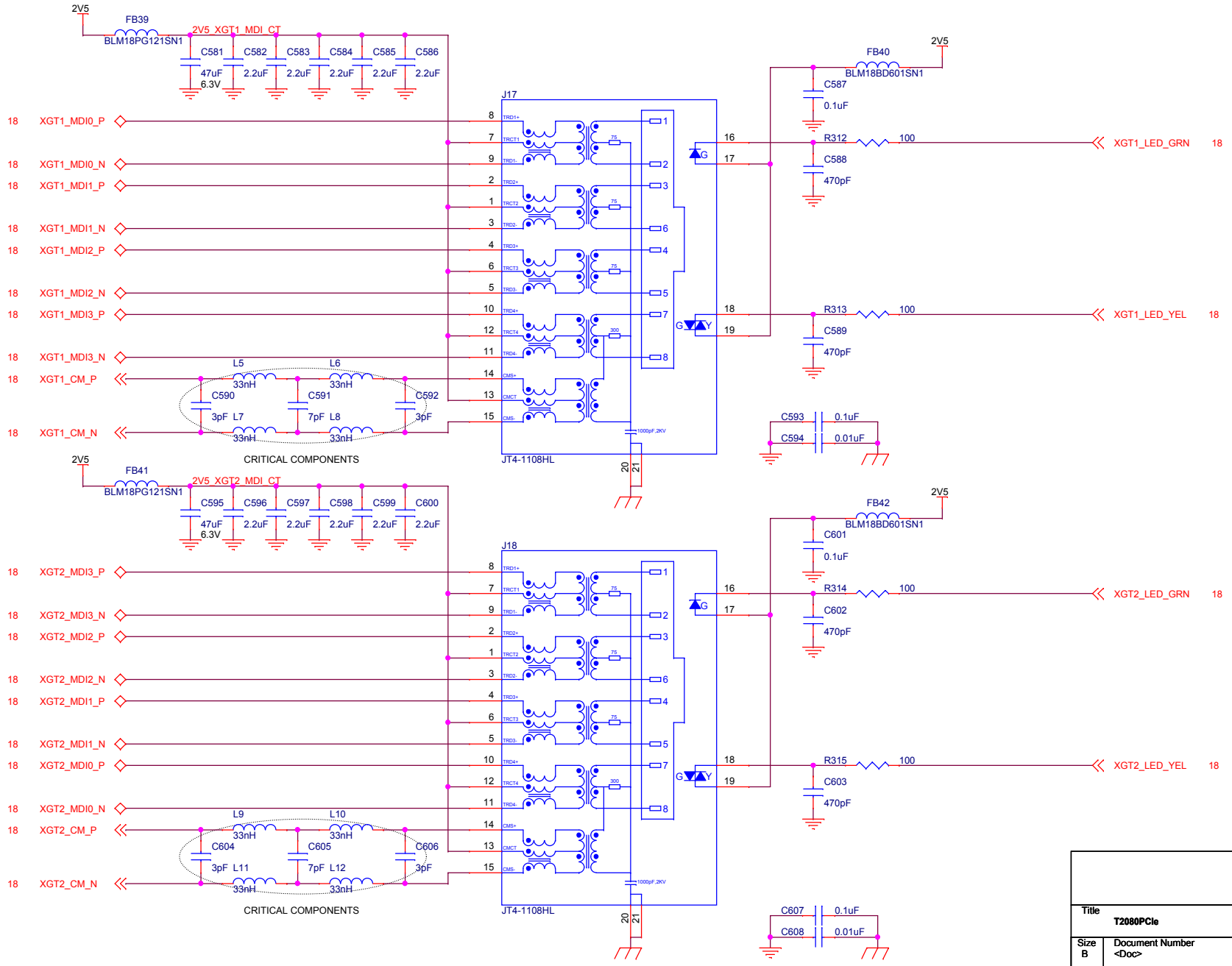






Title	T2080PCIe		
Size B	Document Number <Doc>	Design Engineer *MICETEK*	Rev A
Date: Friday, May 16, 2014		Sheet 19 of 33	

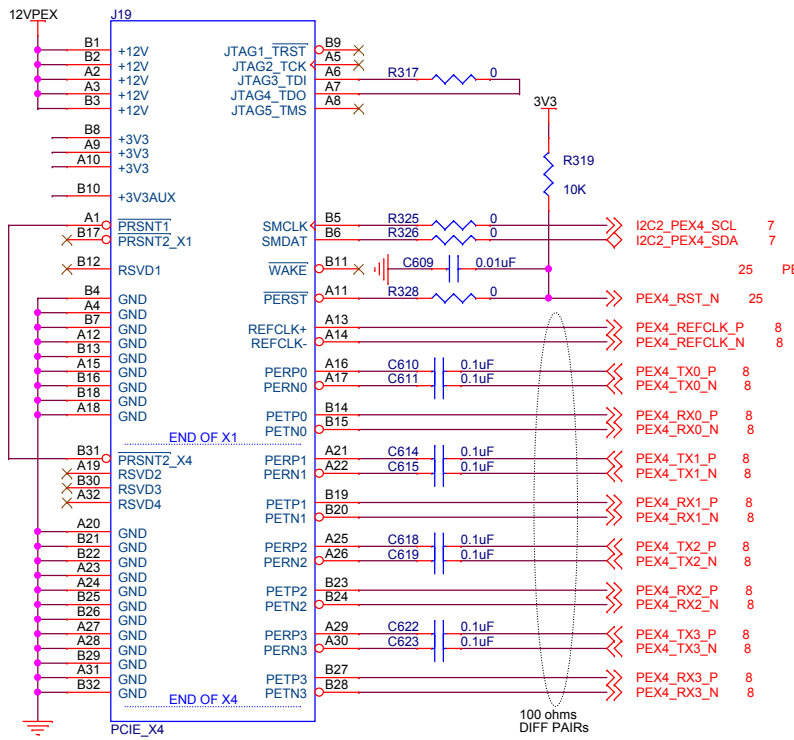
10G BASE-T RJ46 CONNECTORs

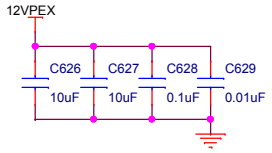


Title: T2080PCIe			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: A
Date: Friday, May 16, 2014		Sheet 20 of 33	

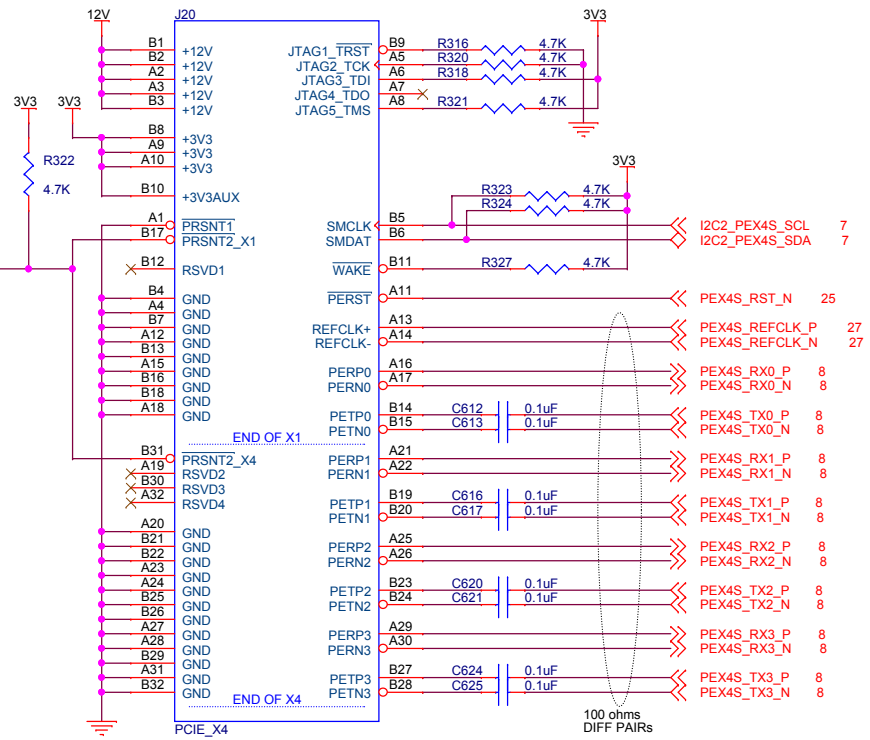
PCIe X4 FINGER, PCIe X4 SLOT and SATA CONNECTORs

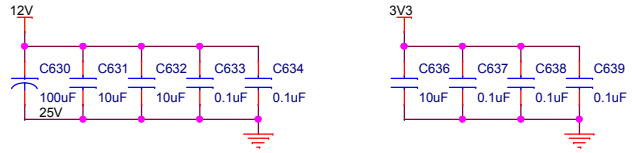
PCIe x4 FINGER



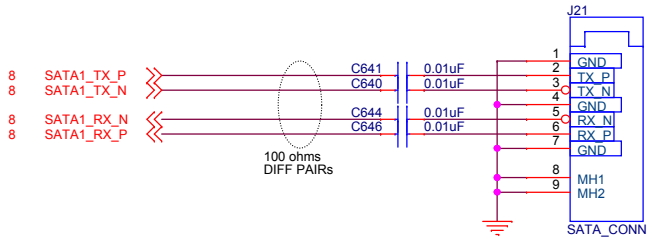


PCIe x4 SLOT

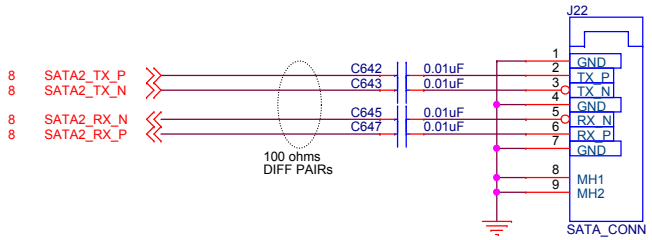




ON-BOARD SATA CONNECTOR

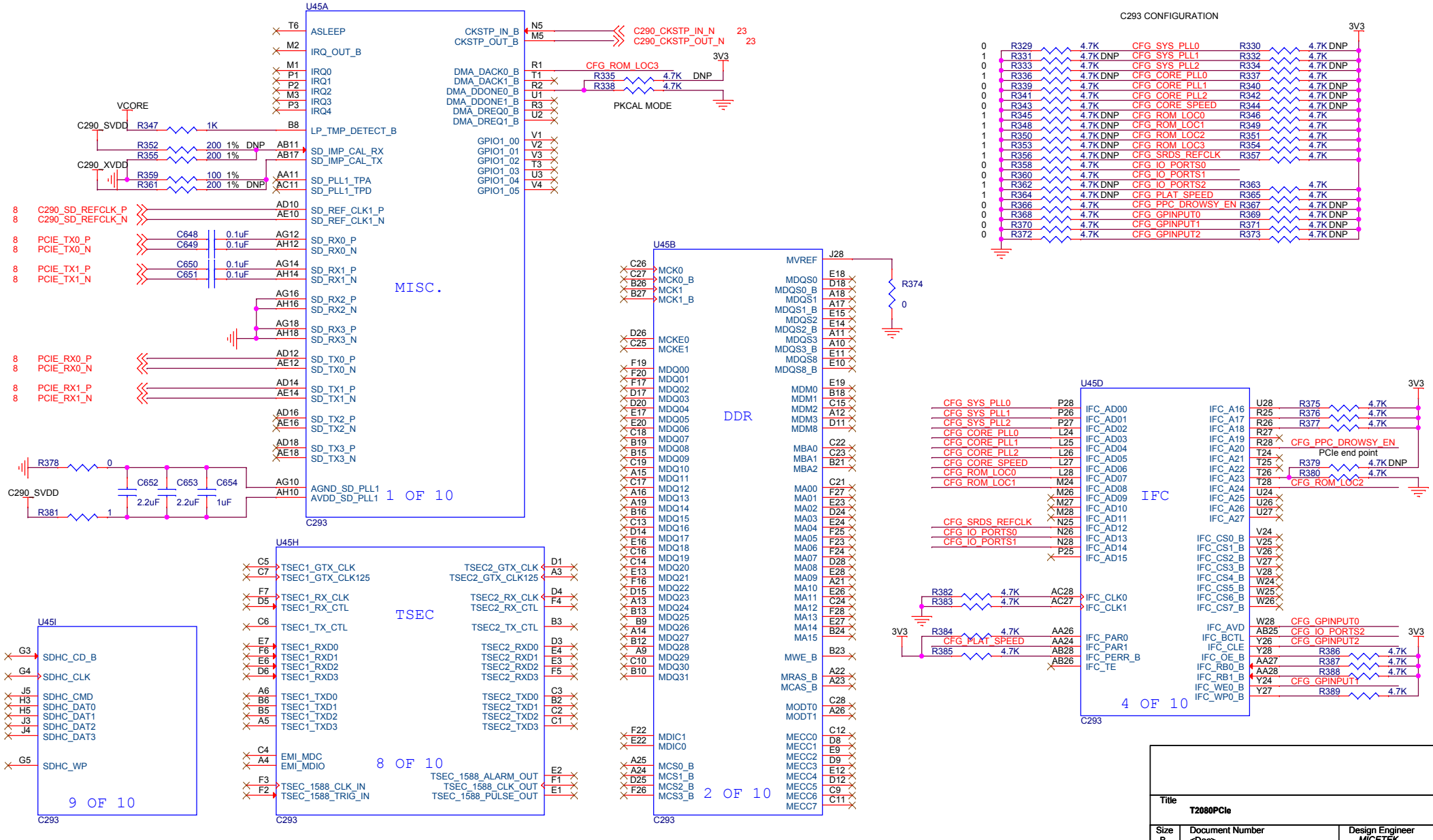


ON-BOARD SATA CONNECTOR



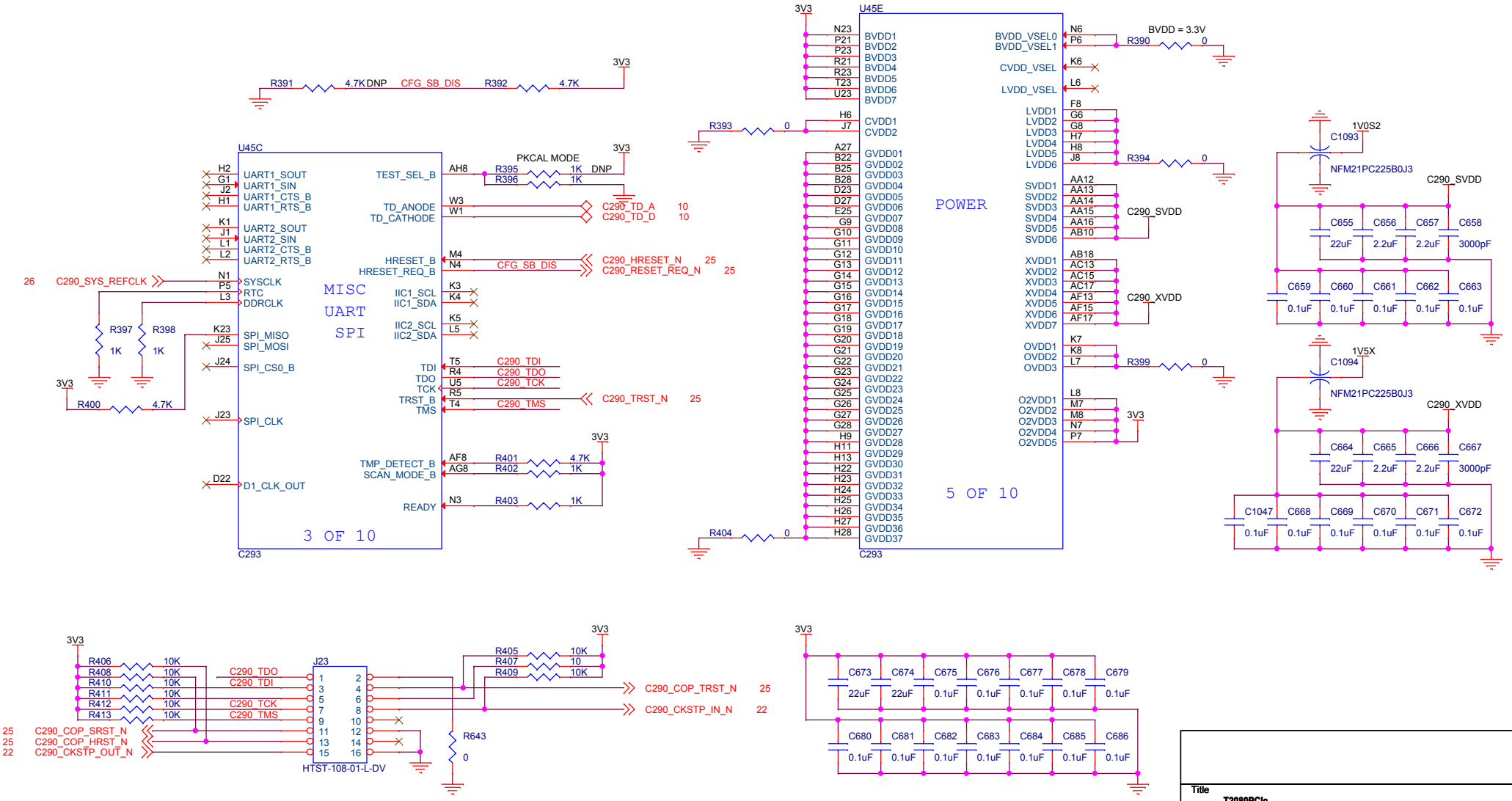
Title: T2080PCIe			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: A
Date: Friday, May 16, 2014		Sheet 21 of 33	

C293 COPROCESSOR (part 1 of 3)



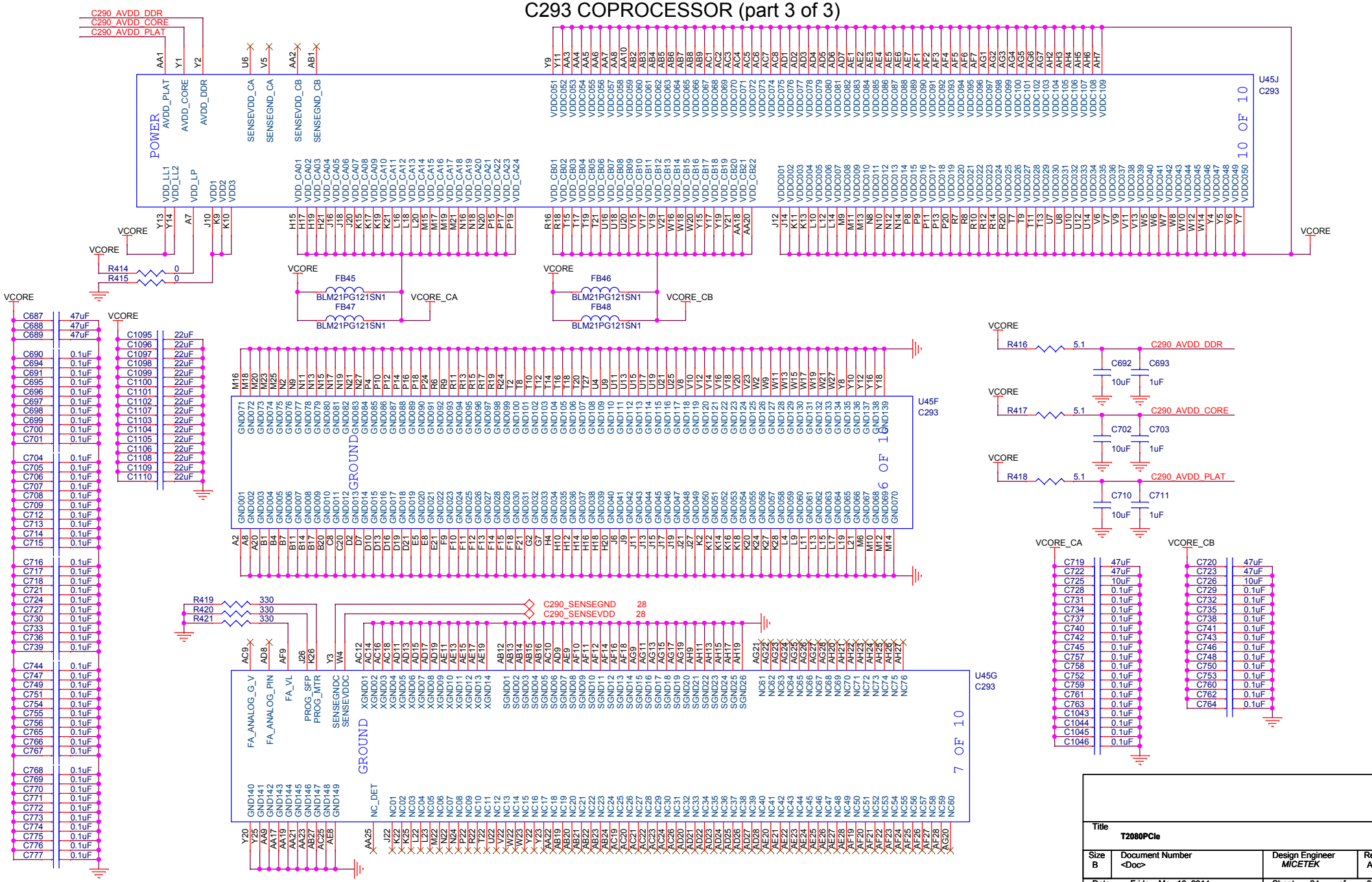
Title	T2080PCIe	
Size B	Document Number <Doc>	Design Engineer MICETEK / Rev A
Date: Friday, May 16, 2014	Sheet 22 of 33	

C293 COPROCESSOR (part 2 of 3)



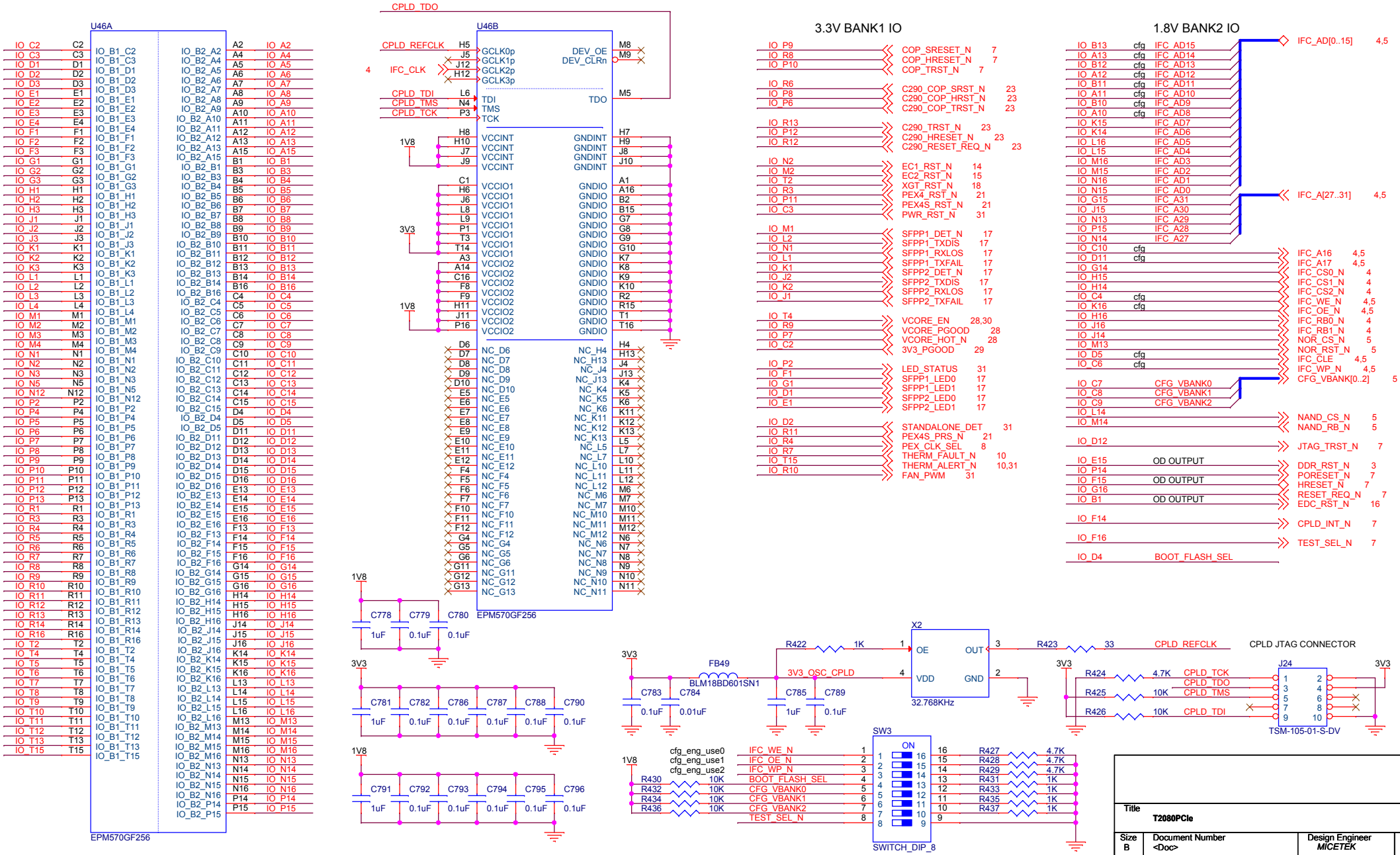
Title: T2080PCIe			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: A
Date: Friday, May 16, 2014		Sheet 23 of 33	

C293 COPROCESSOR (part 3 of 3)

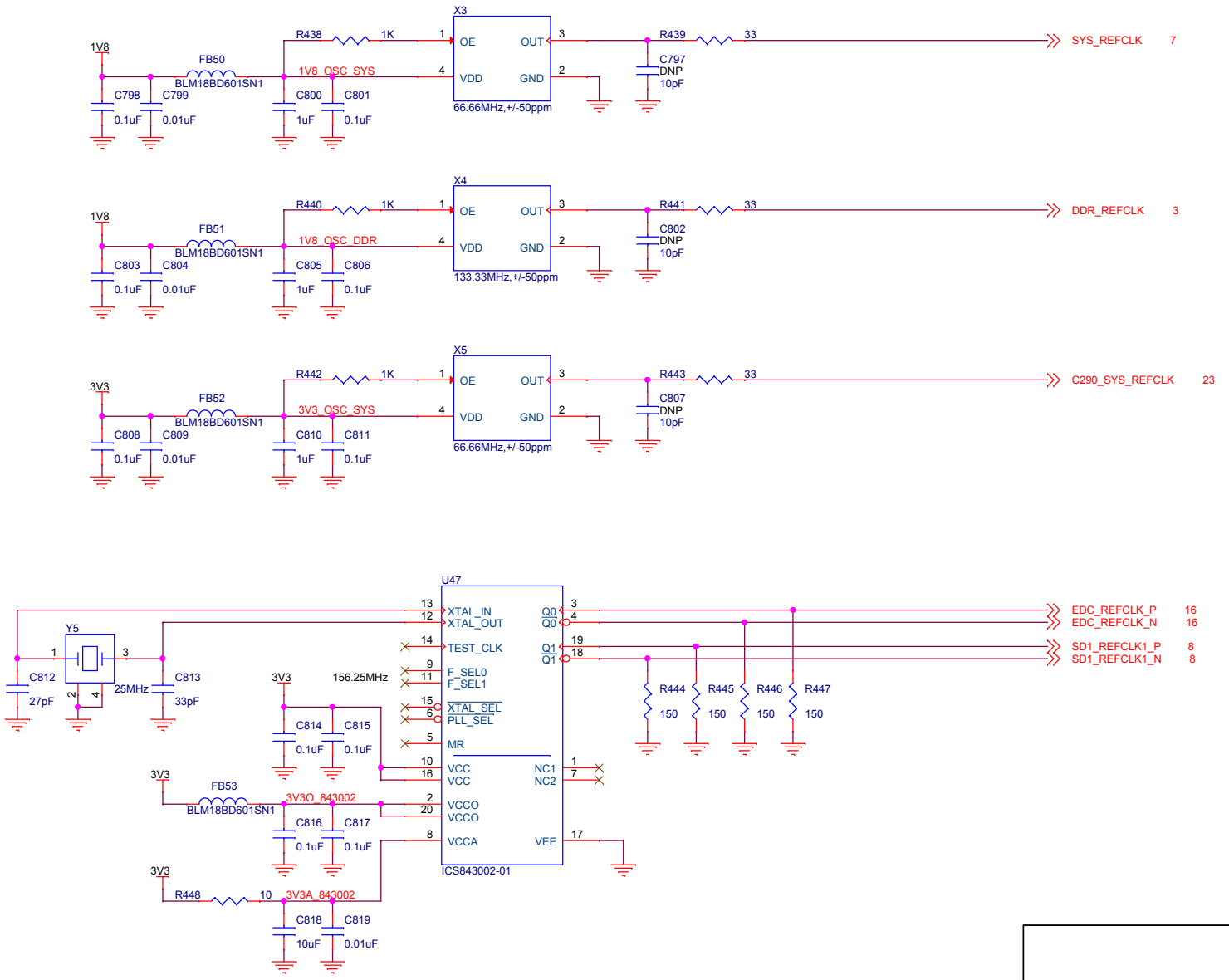


Title: T2080PCIe			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: A
Date: Friday, May 16, 2014		Sheet 24 of 33	

CPLD

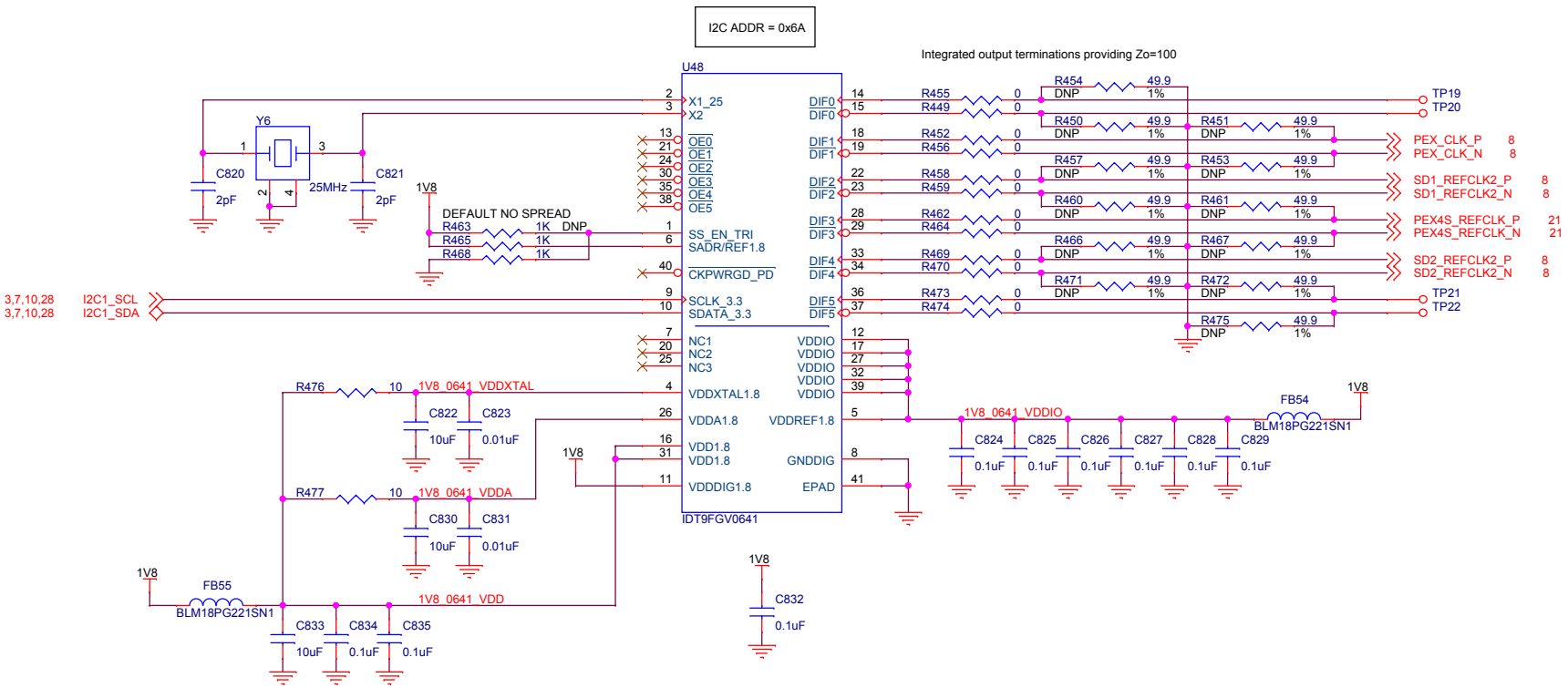

U46A
EPM570GF256
U46B
EPM570GF256
CPLD_TDO
CPLD_REFCLK
IFC_CLK
CPLD_TDI
CPLD_TMS
CPLD_TCK
3.3V BANK1 IO
1.8V BANK2 IO
IFC_AD[0..15]
IFC_A[27..31]
CFG_VBANK[0..2]
CPLD JTAG CONNECTOR
X2
32.768KHz
FB49
BLM18BD601SN1
SW3
SWITCH_DIP_8
TSM-105-01-S-DV
Title
T2080PCIe
Size B
Document Number <Doc>
Design Engineer MICETEK
Rev A
Date: Friday, May 16, 2014
Sheet 25 of 33

SYSTEM CLOCK GENERATORs



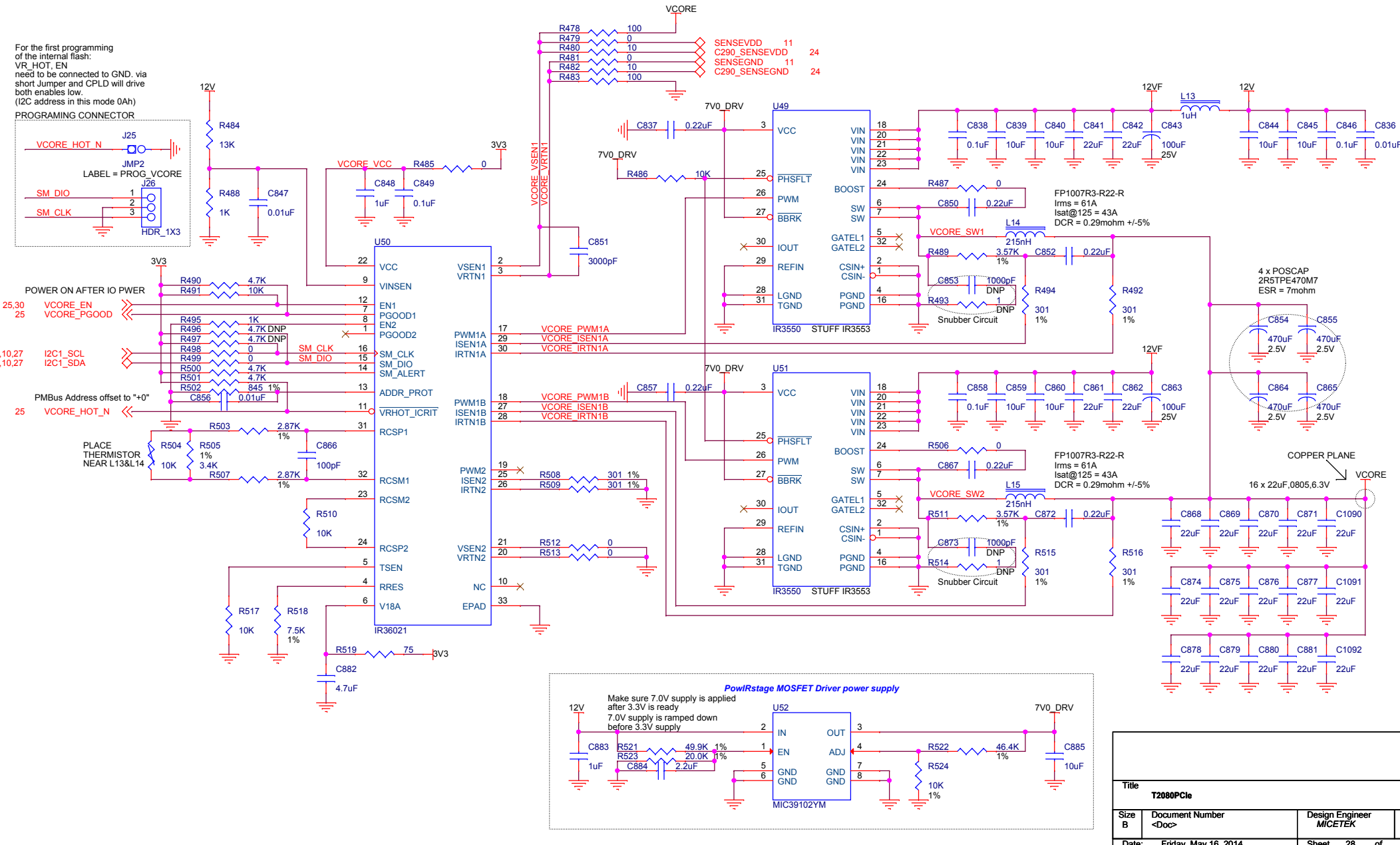
Title: T2080PCIe			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: A
Date: Friday, May 16, 2014		Sheet 26 of 33	

SYSTEM CLOCK GENERATORs (cont.)



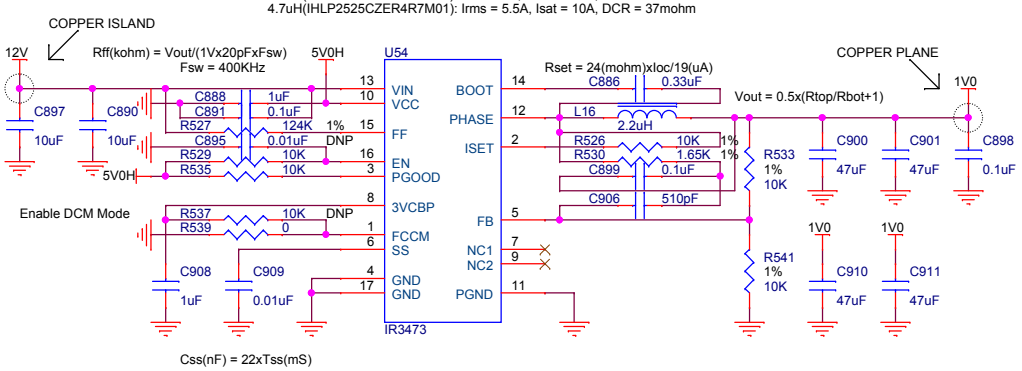
Title: T2080PCIe			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: A
Date: Friday, May 16, 2014		Sheet 27 of 33	

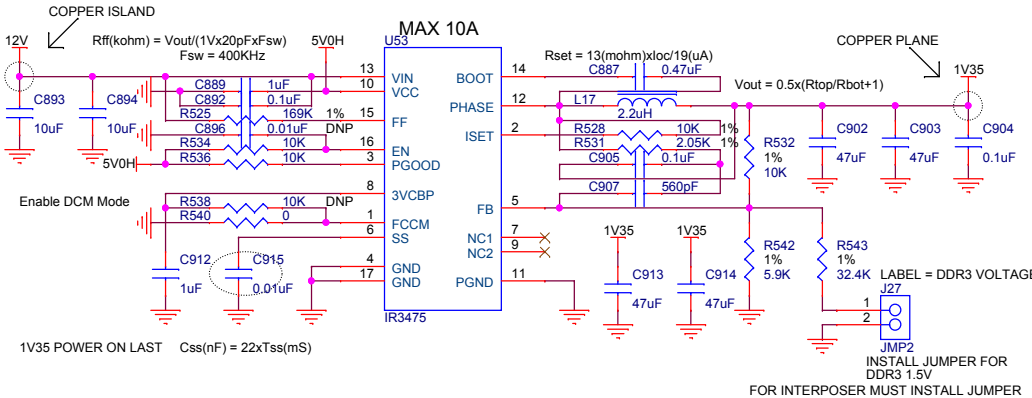
T2080 CORE POWER CONVERTOR

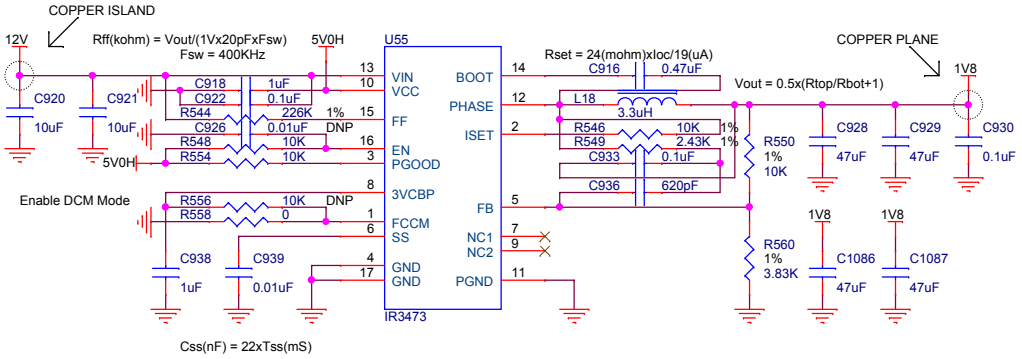


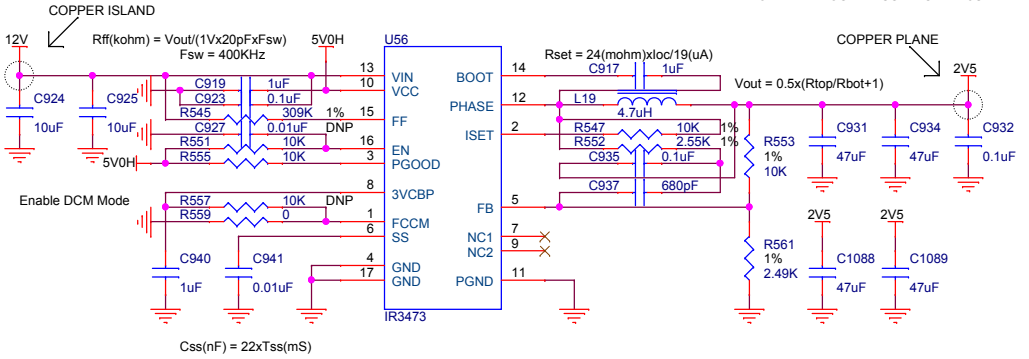
SYSTEM POWER CONVERTORs

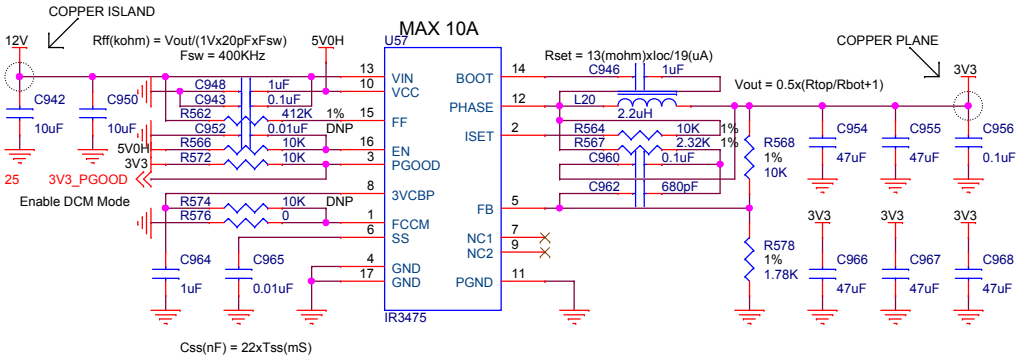
2.2uH(IHLP2525CZER2R2M01): Irms = 8A, Isat = 14A, DCR = 18mohm
3.3uH(IHLP2525CZER3R3M01): Irms = 6A, Isat = 13.5A, DCR = 28mohm
4.7uH(IHLP2525CZER4R7M01): Irms = 5.5A, Isat = 10A, DCR = 37mohm

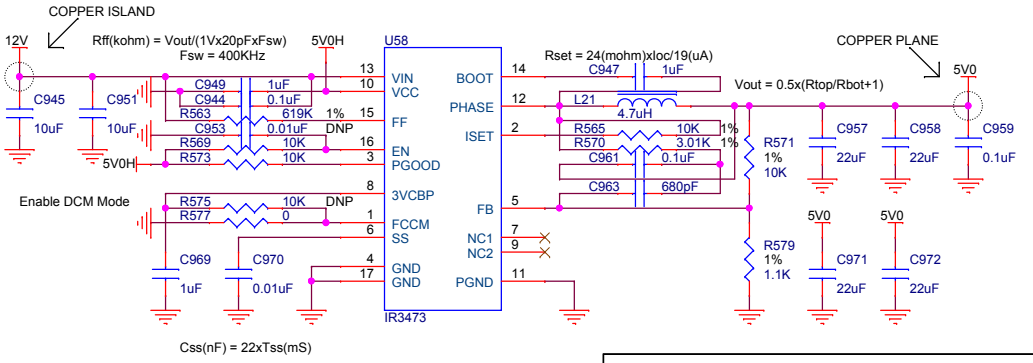








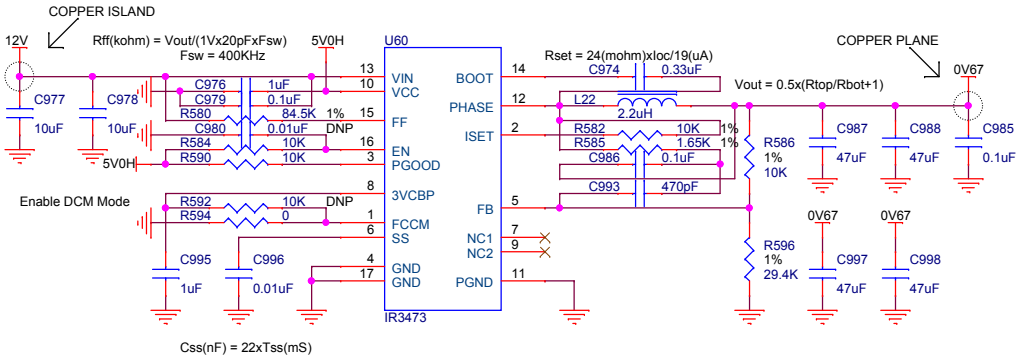


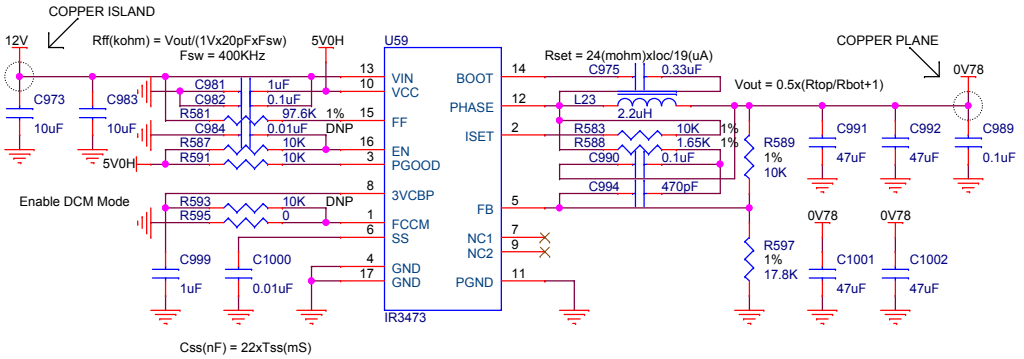


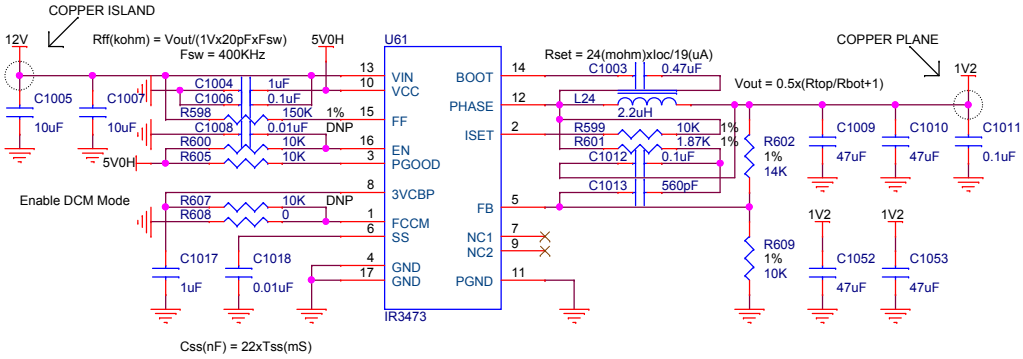
Caution: separate analog and power ground and make connection at GND plane

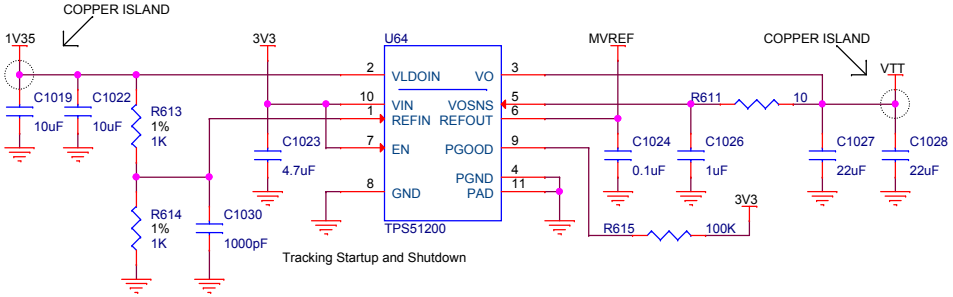
Title: T2080PCIe			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: A
Date: Friday, May 16, 2014		Sheet 29 of 33	

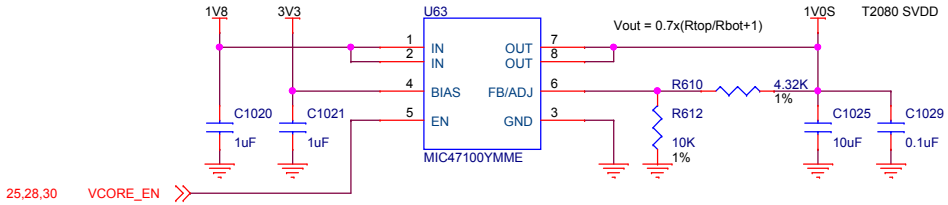
SYSTEM POWER CONVERTORs (cont.)

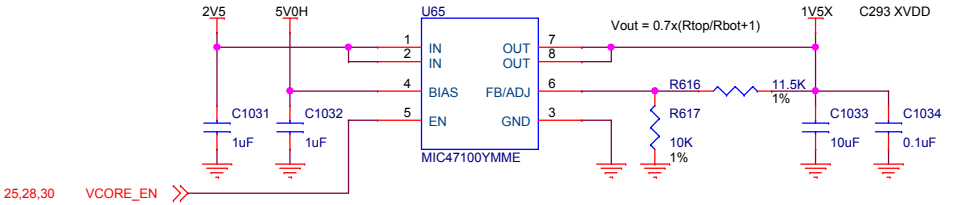


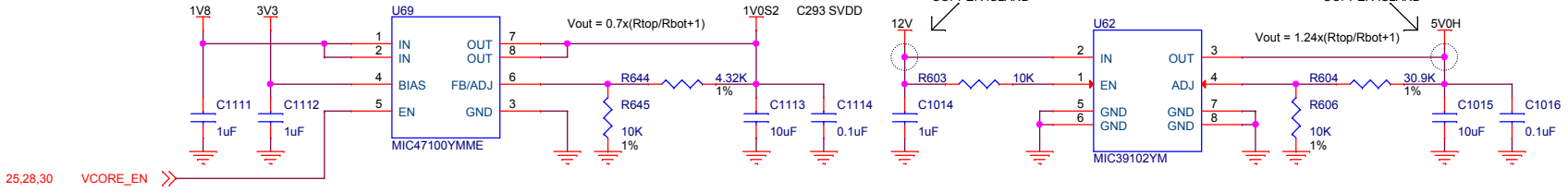






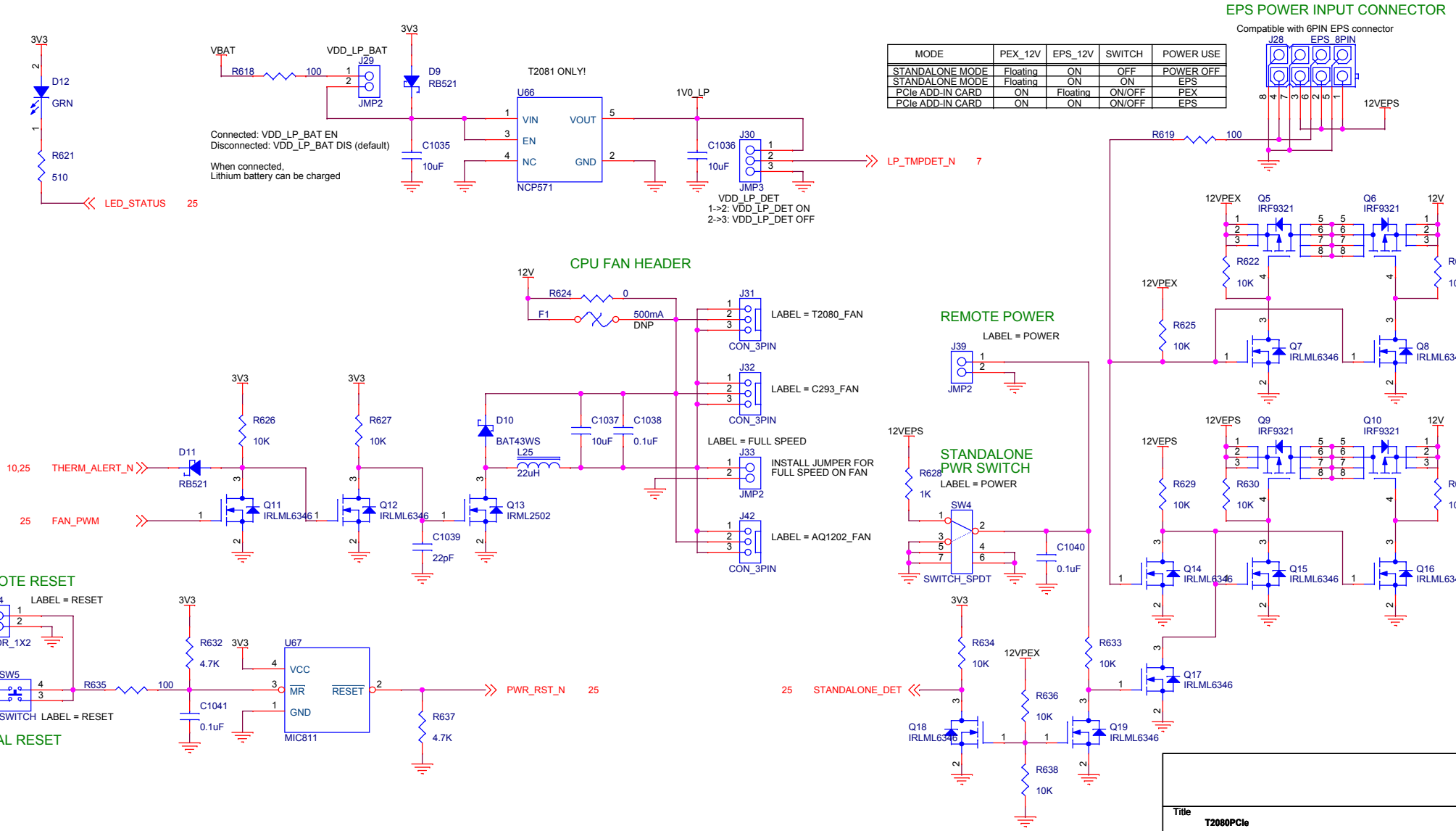






Title: T2080PCIe			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: A
Date: Friday, May 16, 2014		Sheet 30 of 33	

SYSTEM POWER INPUT

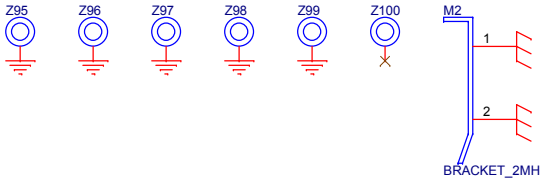


Title	T2080PCIe
Size B / Document Number	<Doc>
Design Engineer	MICETEK
Rev	A
Date:	Friday, May 16, 2014
Sheet	31 of 33

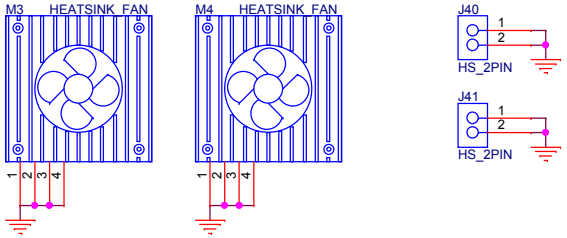
MECHANICALs

Fiducial Marks

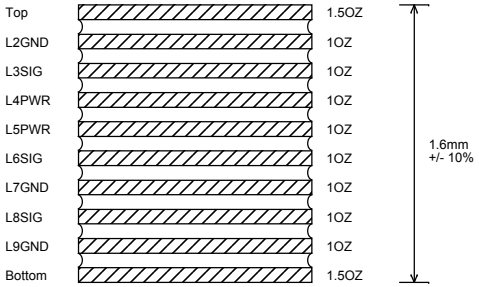
Mouting Holes



Heatsink Fan



Layer Detail



Title: T2080PCIe			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: A
Date: Friday, May 16, 2014		Sheet 32 of 33	

CHANGE LIST

2013/7/19
1. Add 20K pull-up to IFC_A[16-19],AVD,OE,WE,WP
2. Add IFC_LATCH_N to IFC voltage level translators
3. Change NAND RB pull-up to 1K
4. Change SD card ESD chip to Rclamp0524J
5. Change NOR MPN to S29GL01GP11TFIV10
6. Add 1.0V LDO for S1VDD, use NFM55PC155F1H4B instead of BLM18 bead for SVDD and XVDD
7. Add 0.22uF to AVDD_CGA, PLAT and D1 voltages
8. Add a 0.1uF debounce cap to power on switch
9. Update IR power regulators refer to IR's comments
10. Change SD card insert and protect signal pull-up to 1.8V and connect to T2080 derectly

2013/7/24
1. Change I2C MUX address to 0x77
2. Add test point for CLK_OUT and RTC, change RTC pull-down to 10K
3. Add test point for 1588 signals
4. Change USB protect chip from SRV05-4 to VBUS054B-HSF
5. Change LED drive resistor from 330ohm to 510ohm
6. Add test points for SD_PLL_TPA and SD_PLL_TPD
7. Add optional filtering for USB_BIAS
10. Connect RGMII PHY tap pins together, change crystal caps from 20pF to 27pF,
remove bead, add 0 ohm to ENSWREG, change RST to pull-up

2013/8/27
1. Update IR3473/IR3475 circuit, following T1040/T1042RDB
2. Change SVDD and XVDD filter cap from NFM55PC155 to NFM21PC225
3. Swap AQ1202 P1 MDI order
4. Change NAND Flash from TSOP48 to BGA, so can delete 1.8V to 3.3V voltage translator
5. Change SD card to TF card for space saving, like T4240PCIe board
6. Change battery socket to lithium rechargeable battery for space saving
7. Update C293 part circuit in PKCAL mode
8. Change ADT7461 to ADT7481 for sense T2080 and C293
9. Add FAN header for C293
10. Change EMI2 voltage from 1.8V to 1.2V, change CS4315 IO_VDD_SEL pull-down to select MDIO operates at 1.0V
11. Add 1uH inductor for VCORE 12V filter
12. Change mini PCIe to PCIe x4 slot

2013/9/1
1. Add P2041 interposer support
2. Change NAND Flash from BGA to TSOP48
3. Change SFP+ RS0/1 signal to CPLD, add pull-up/down resistor
4. Change 100M diff clock chip to IDT9FGV0641
5. Add C293 VDD sense to IR36021

2013/9/5
1. Change PCIe slot footprint from DIP to SMT

2013/9/12
1. Add notes at page 1

2013/10/15
1. Remove interposer support
2. Change UART RJ45 connector to 2x3pin header
3. Change RGMII PHY RJ45 to with magnetic module

2013/11/26
1. Change IR36021 address offset to +0

2013/12/1
1. Add 1.0V LDO for C293 SVDD
2. Add 0ohm to COP PIN2

Title: T1040RDB			
Size: B	Document Number: <Doc>	Design Engineer: *MICETEK*	Rev: A
Date: Friday, May 16, 2014		Sheet 33 of 33	