MCIMX93-9x9 package Quick Start Board

MCIMX93-QSB

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Revision History

Rev. Code	Date	By	Description
A	2022-05-06	nxa13729	Initial version
A1	2022-09-01	nxa13729	DNP R1767, chang to 1.8V PU due to USB ID power domain is 1.8V Add R823 as USB TCPC shared interrupt to support level trigger mode Change R812 connected with HP_DET which used as audio jack detection Add R845 connected with AUD_nINT to maintain the SW compatible Add R1822, DNP R1203 as audio jack detection to GPIO IRQ path Add R956,R957 for M.2 compatible design Add U1004,D1011,D1012,R1072,R1073-R1085,C1021-C1024,BT1001,TP1015-TP1021 RTC module circuits Change L503,L504 to 0 OHM R530,R531 Add R958,R959 to use RTC_CLKO Add R1823 Add R745,R748, J1710,J1711，used for Audio Hat Board Remove TP1954, TP1955, TP1956,TP1958 Add R850,R851,R852,R853,R854 for backup DNP R1433,R1434,R1435 Add TEMP Sensor U915，R860,R861,R862,R863,C955,C956 PMIC PN Change from PCA9451 to PCA9451A, delete VLDO3_1V8 DNP C728 ADD R870, R871 for validation Add U908 level shift LSF0102 to replace the level shifter inside PMIC ADD TP218, TP219,TP220,TP221 for validation
A2	2023-06-25	nxa13729	Update U101 symbol for USB ID power domain Change VDD_SOC_0V8 to VDD_SOC_0V85，Remove R870, Add R111,Install C728 Change ADC power rail with more CAP+FB, install C720, change L102 to 1K OHM FB Add R211 to support LPDDR4/X w/ 2CS Add R102 to support 100-ball LPDDR4/X Default use PMIC internal Level shift for I2C1. Take U908 NTS0104GU12 as backup. Install R717,R719, R713,R712 Remove TP1959, Add R858, for GPIO EXP3V3_EN Add C931,C932,C933 for better performance Remove R314, C308. Delect the net of USB_GND_CHASSIS Remove the net name of HPL_ZOBEL Add C1230, C1231 for the power of WM8962. Install R1203 to keep WM8962B GPIO5 PU Change the symbol of GND Testloop: TP1901, TP1905,TP1906 Update J1101, J1708 USB Type C connector to longer pin length (footprint compatible) to improve the reliability of soldering Change R745 to 33ohm for better audio performance Remove J1711 and R748, Add R855 and R856
A3	2023-11-10	nxa13729	Using GPIO(U801.P0_2) to control power EXP_5V to fix LCD fliker issue Change R1420 to 1K (DNP default) due to mid-voltage caused by LSM6DSOXTR internal PD Remove TP1906 Update U101 symbol for pinname change （E10） Change the value of resistors R855 and R856 to 0R Add R360, D302 (DNP default) for USB PWR detection backup Update U502, U503 due to ESD EOL
A4	2024-06-27	-	change C102 from 0.22uF to 1.0uF change U201 DDR from MT53E1G16D1FW-046 AAT:A to MT53E1G16D1ZW-046 AAT:C due to EoF change U404 from SGM8709YN5G to MCP6546T-E/OT due to leakage all changes do not impact layout, this schematic version is paired with layout LAY-54852_A3

Preliminary - Subject to Change without Notice!

This board was designed for maximum flexibility in software development and demonstrates multiple functions possible with i.MX processors. Although best design practices have been applied, some areas may not be suitable for a mass-production design.

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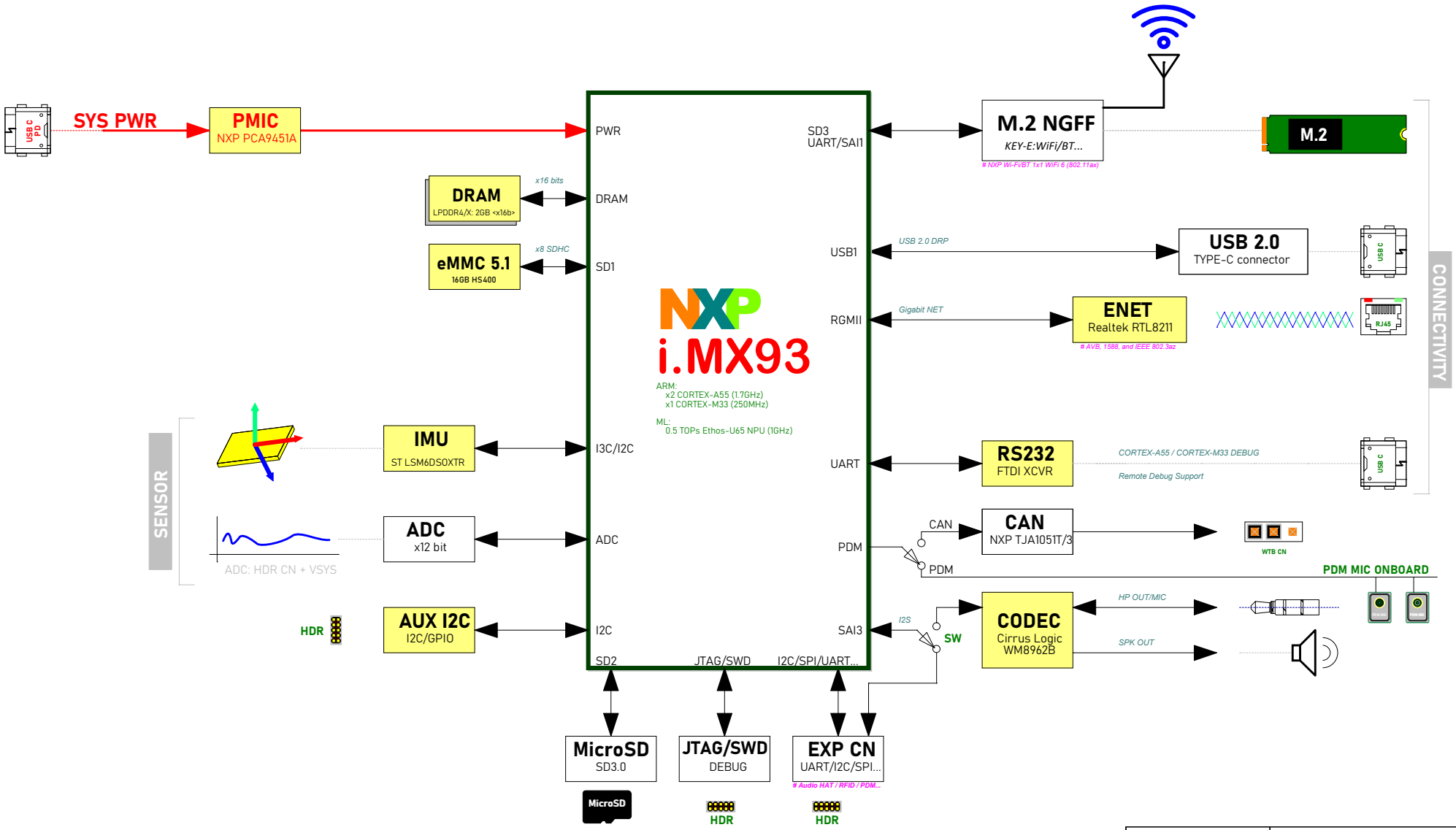
BLOCK DIAGRAM



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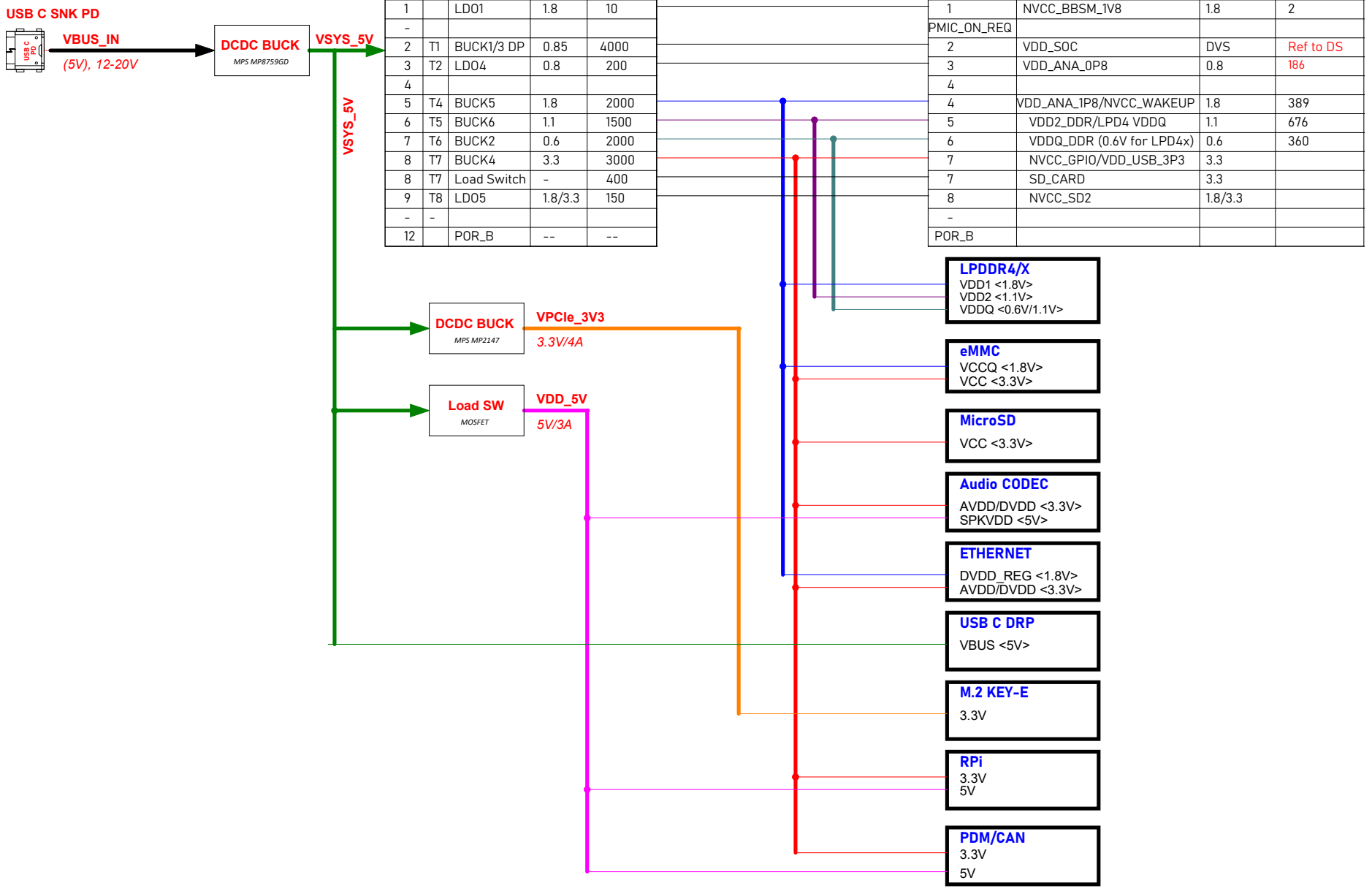
i.MX93 EVK PWR TREE



PMIC: PCA9451AHN

SEQ		REGULATOR	VOL (V)	MAX I (mA)
1		LDO1	1.8	10
-				
2	T1	BUCK1/3 DP	0.85	4000
3	T2	LDO4	0.8	200
4				
5	T4	BUCK5	1.8	2000
6	T5	BUCK6	1.1	1500
7	T6	BUCK2	0.6	2000
8	T7	BUCK4	3.3	3000
8	T7	Load Switch	-	400
9	T8	LDO5	1.8/3.3	150
-	-			
12		POR_B	--	--

SoC: i.MX93

ITEM	PWR RAIL	TYP VOL(V)	REQ I (mA)
1	NVCC_BBSM_1V8	1.8	2
PMIC_ON_REQ			
2	VDD_SOC	DVS	Ref to DS
3	VDD_ANA_0P8	0.8	186
4			
4	VDD_ANA_1P8/NVCC_WAKEUP	1.8	389
5	VDD2_DDR/LPD4 VDDQ	1.1	676
6	VDDQ_DDR (0.6V for LPD4x)	0.6	360
7	NVCC_GPIO/VDD_USB_3P3	3.3	
7	SD_CARD	3.3	
8	NVCC_SD2	1.8/3.3	
-			
POR_B			

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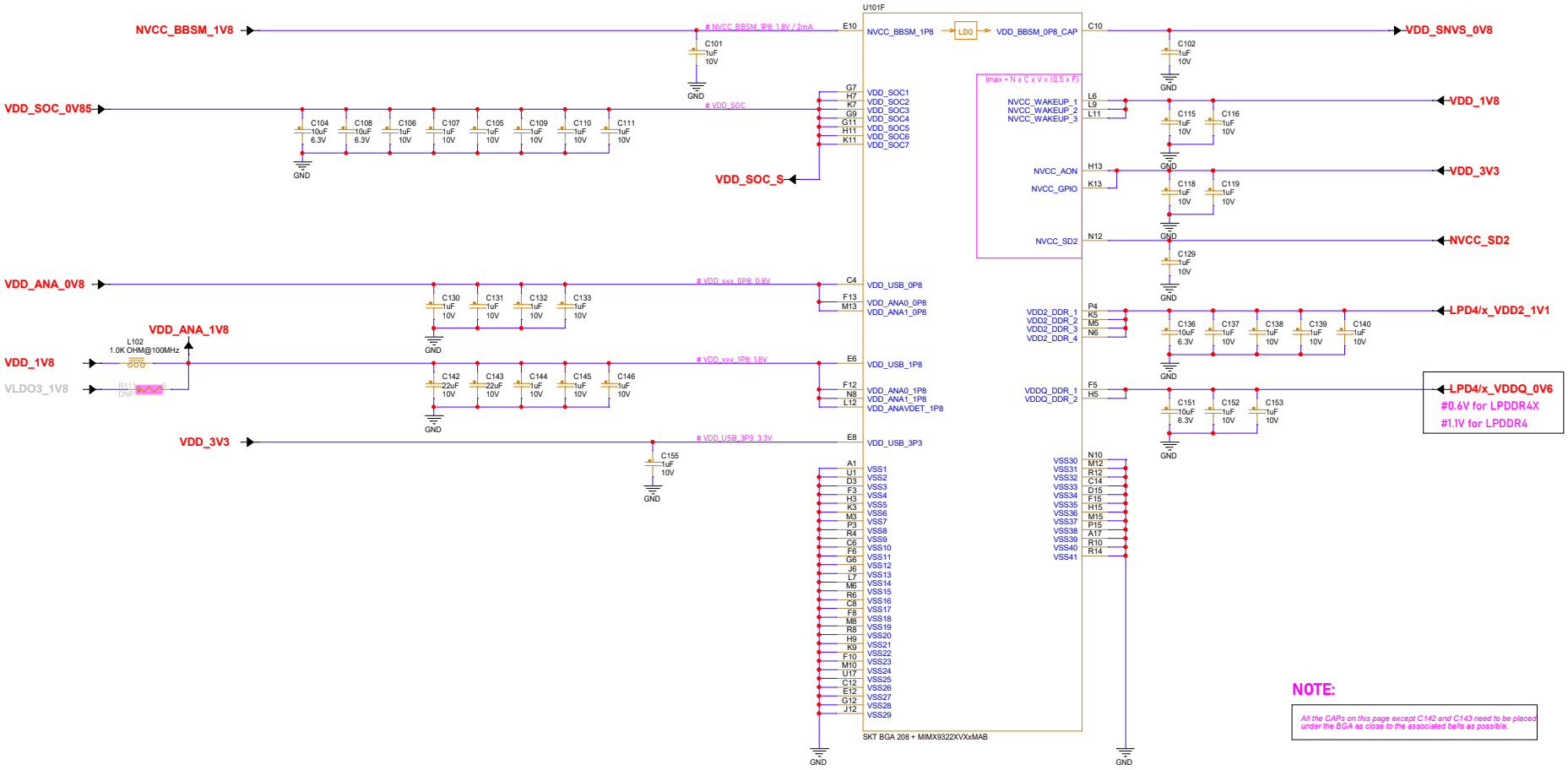
i.MX93 PWR



NOTE:

All the CAPs on this page except C142 and C143 need to be placed under the BGA as close to the associated balls as possible.

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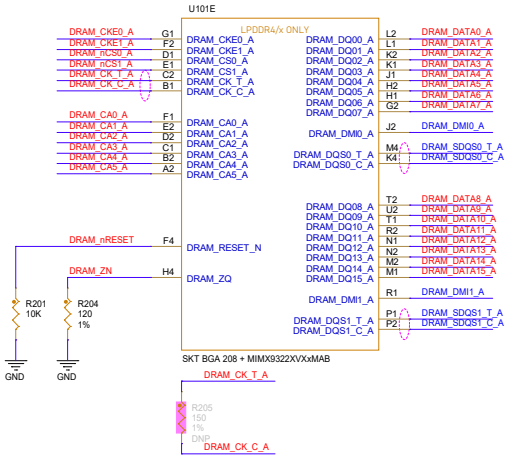
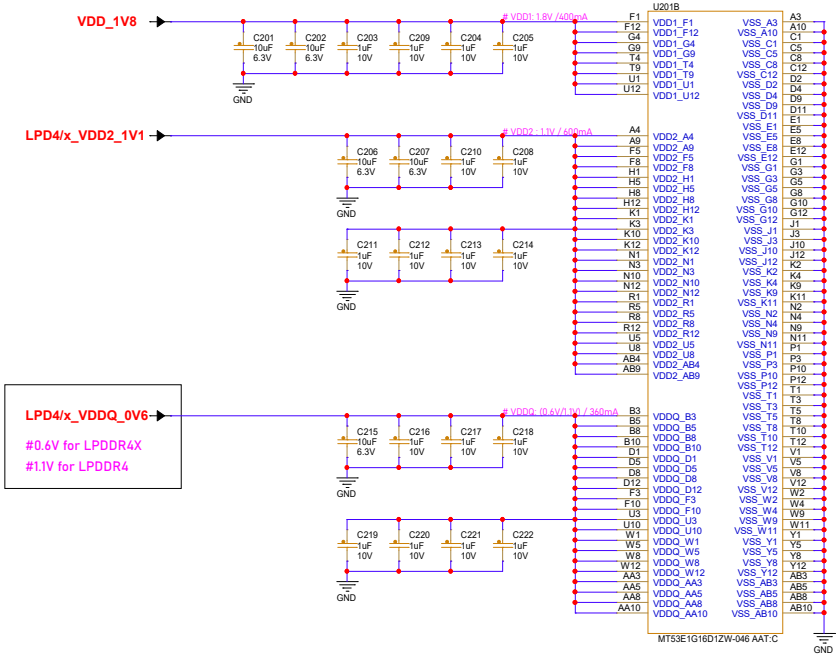
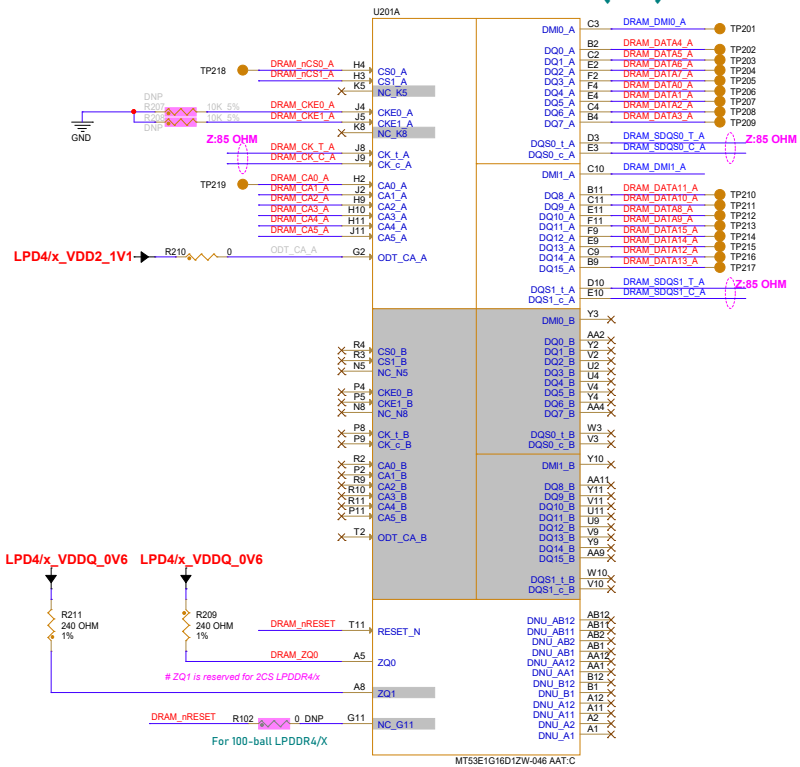
LPDDR4/X





LPDDR4X: 2GB (x16)



 # Power Supply Voltage Sequence:

RESET_n is held LOW.
VDD1 >= VDD2
VDD2 >= VDDQ-200mV

Power ramp duration tINIT0 (Tb-Ta) must not exceed 20ms.

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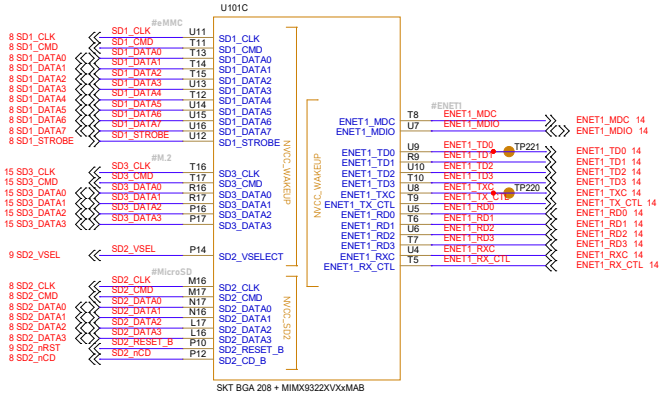
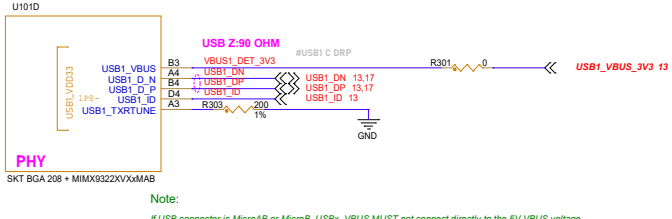
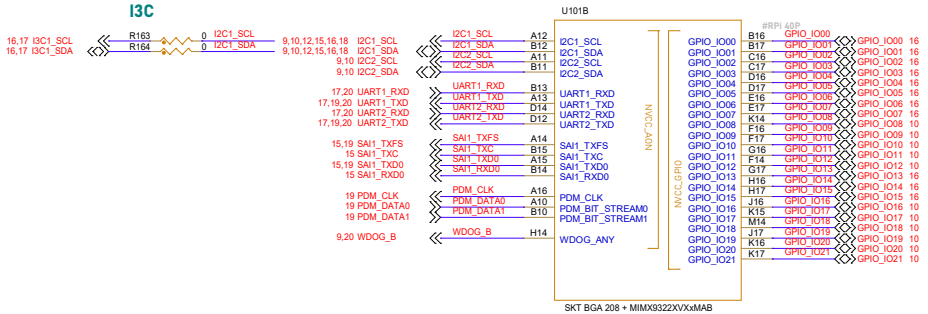
i.MX9D IO/PHY

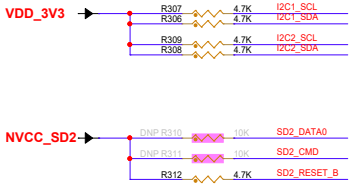




Note:

If USB connector is MicroAB or MicroB, USBx_VBUS MUST not connect directly to the 5V VBUS voltage of connector. Instead, this pin must be isloated with an external 30K 1% resistor.





External PU is necessary for SD2_RESET_B to enable SD card power as default!

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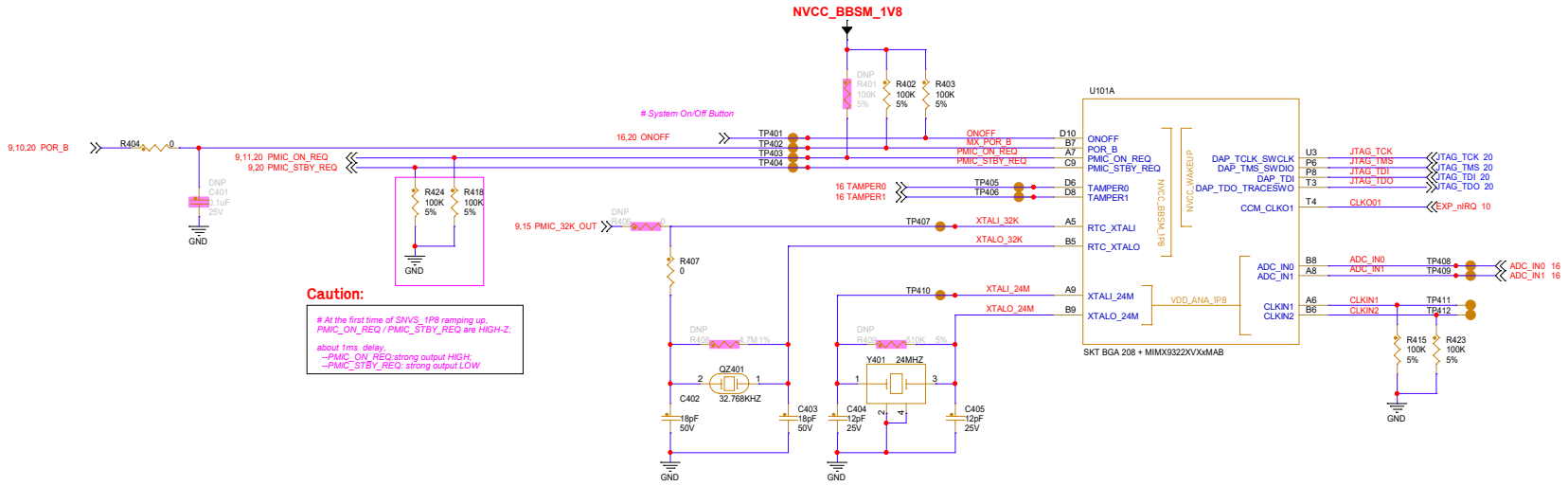
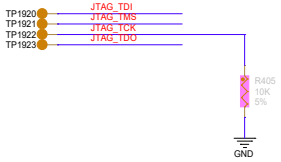
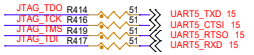
i.MX9D MISC



JTAG/SWD



M.2 UART



Debug through JTAG interface must remove card inserted in M.2 U1707

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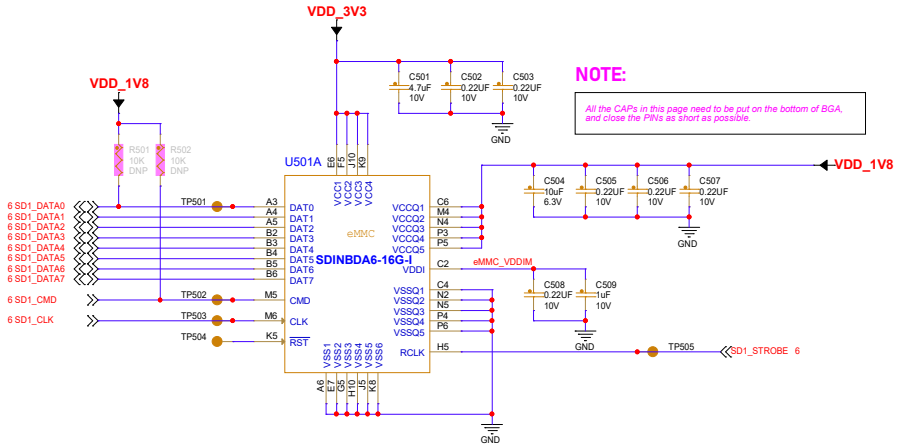
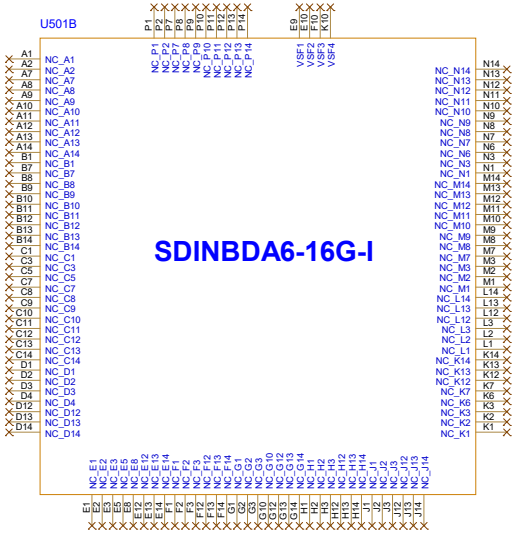
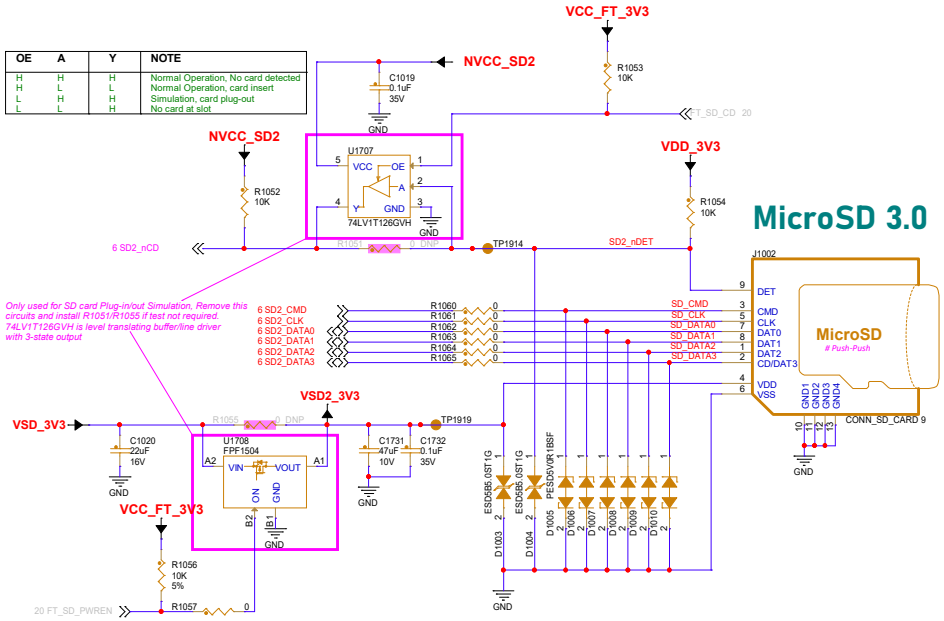
FLASH: eMMC <5.1>

16GB <2D MLC eMMC>





OE	A	Y	NOTE
H	H	H	Normal Operation, No card detected
H	L	L	Normal Operation, card insert
L	H	H	Simulation, card plug-out
L	L	H	No card at slot



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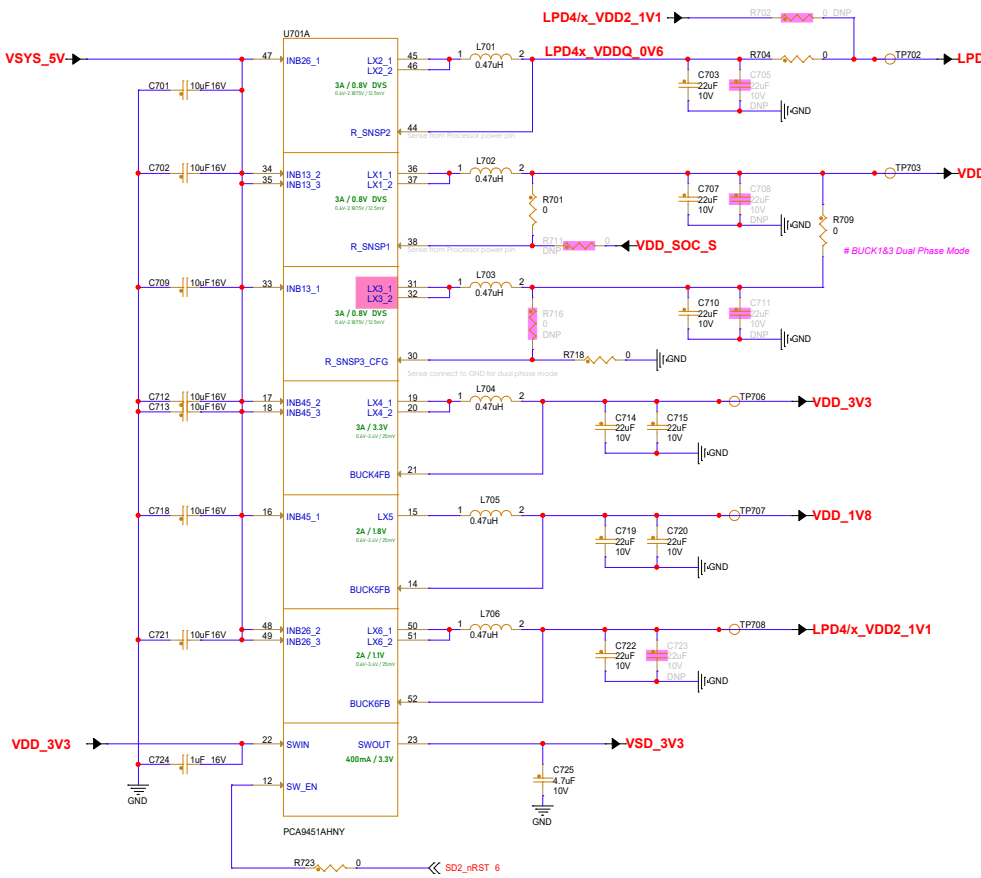
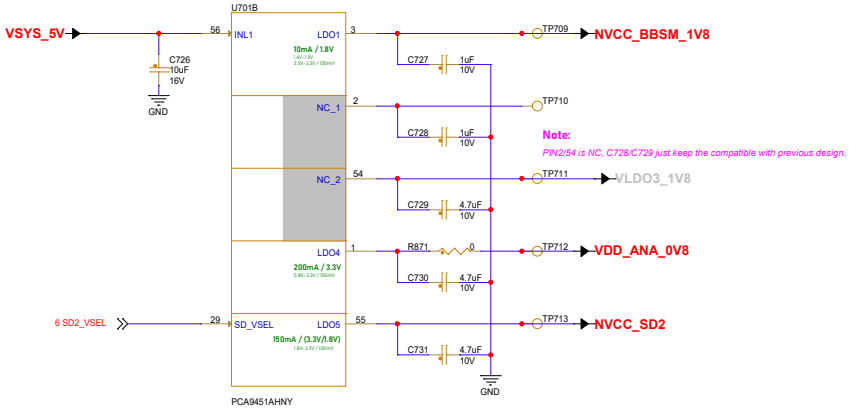
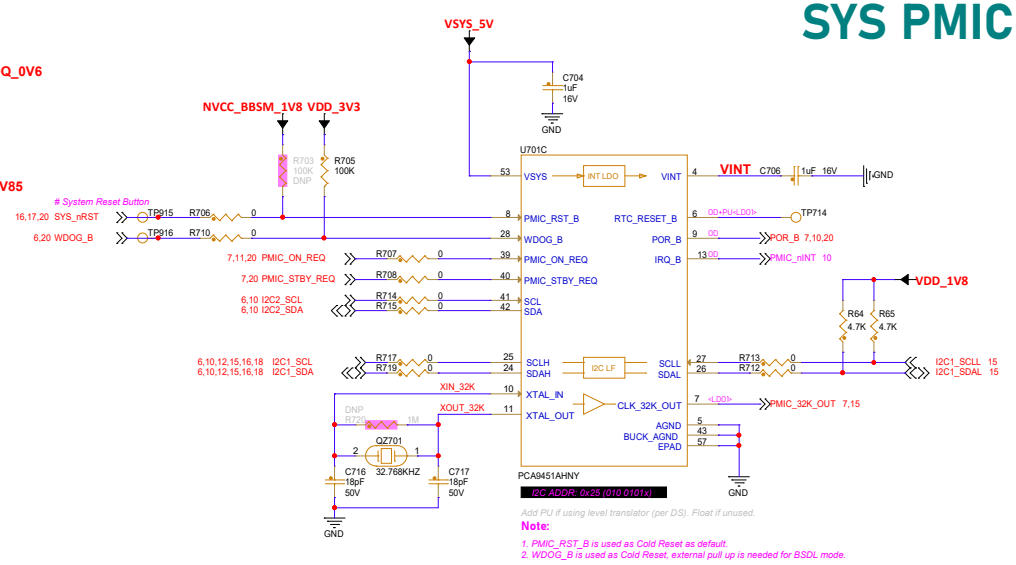
SYS PMIC







PMIC: PCA9451AHN CFG

SEQ	tstep=2ms	REGULATOR	VOL (V)	MAX I (mA)	PWR RAIL	TYP VOL(V)	REQ I (mA)
1		LDO1	1.8	10	NVCC_BBSM_1V8	1.8	2
-							
-					PMIC_ON_REQ		
2	T1	BUCK1/3 DP	0.85	4000	VDD_SOC	DVS	Ref to DS
3	T2	LDO4	0.8	200	VDD_ANA_0P8 VDD_MIPI_0P8 VDD_USB_0P8	0.8	186
4							
5	T4	BUCK5	1.8	2000	VDD_ANAx_1P8 VDD_LVDS_1P8 VDD_MIPI_1P8 VDD_USB_1P8 NVCC_GPIO	1.8	1040 PERI INCLUDE
6	T5	BUCK6	1.1	1500	VDD2_DDR VDDQ_DDR (1.1V for LPD4)	1.1	676
7	T6	BUCK2	0.6	2000	VDDQ_DDR (0.6V for LPD4x)	0.6	360
8	T7	BUCK4	3.3	3000	NVCC_GPIO VDD_USB_3P3	3.3	2870 PERI INCLUDE
8	T7	Load Switch	-	400	SD_CARD (from BUCK4)	3.3	
9	T8	LDO5	1.8/3.3	150	NVCC_SD2	1.8/3.3	
-	-						
12		POR_B	--	--	POR_B		

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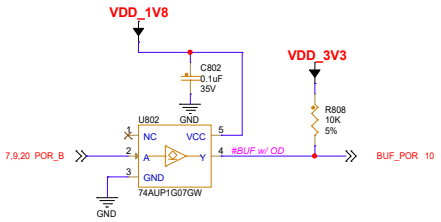
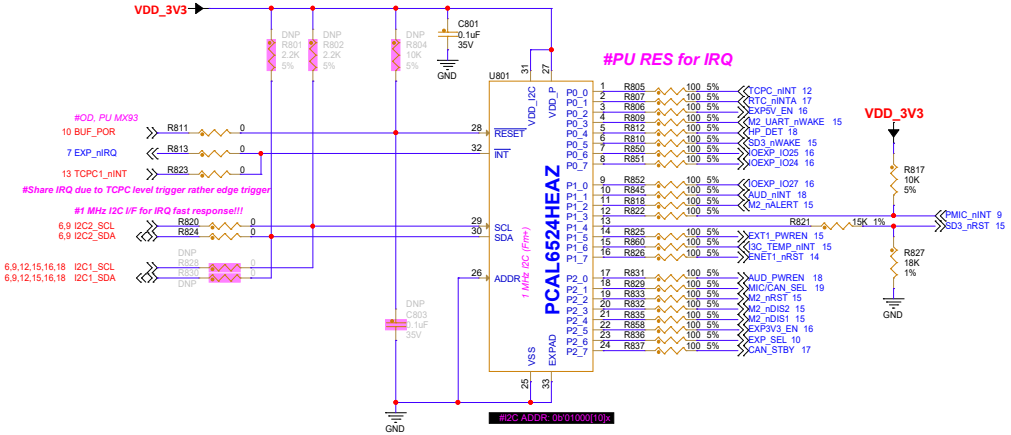
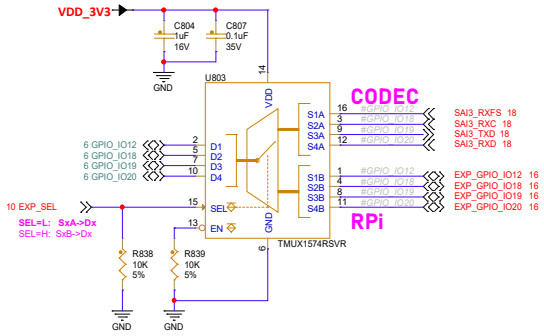
IO MUX / EXP

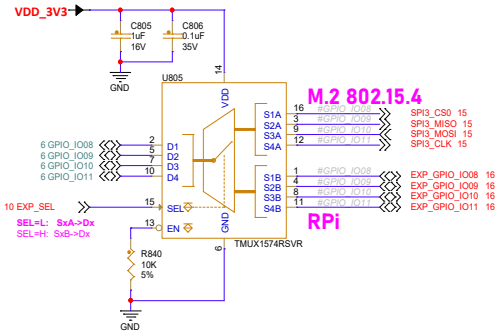


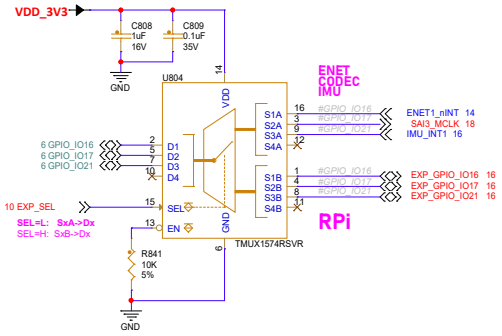
I2C IO EXP



SHARED GPIO MUX







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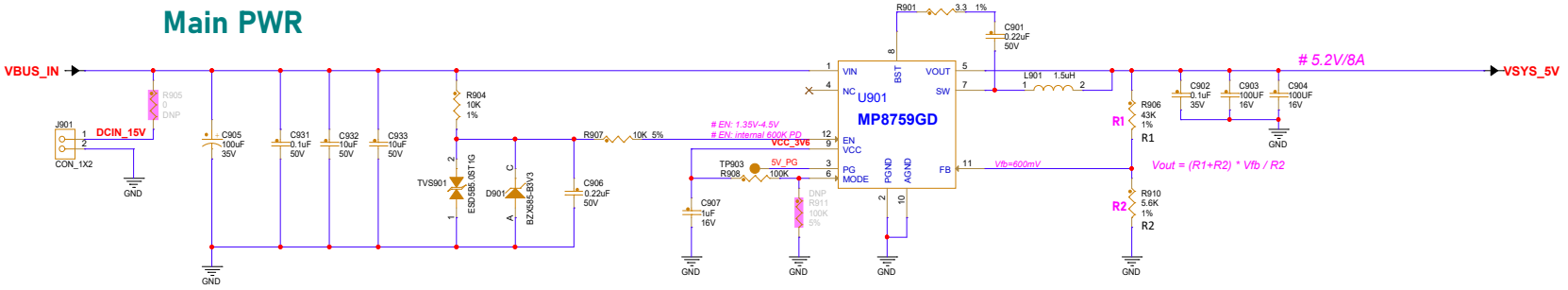
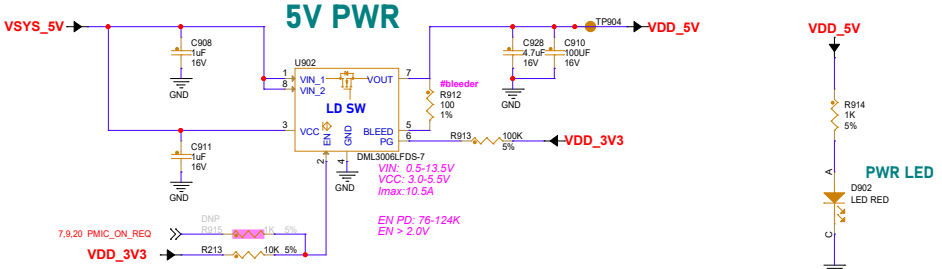
SYSTEM POWER

When PERI 12V is required, VBUS_IN must be at least 12V!!!

Main PWR



5V PWR



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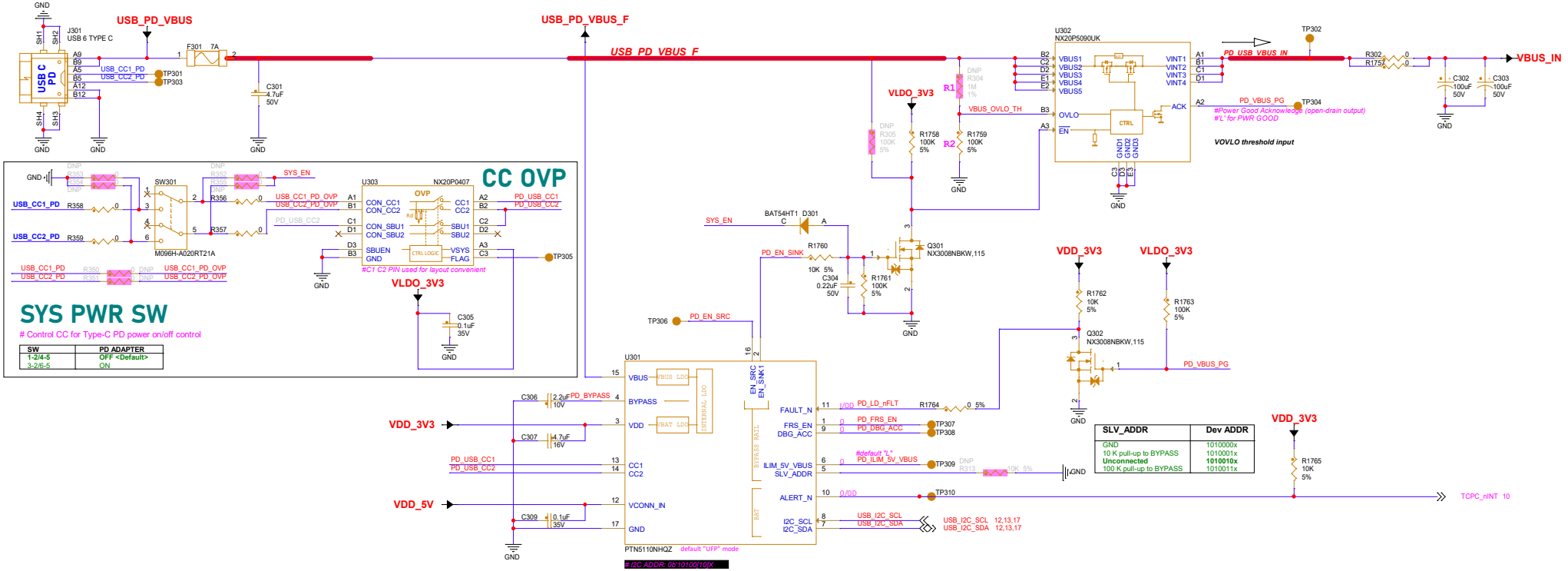
USB TYPE-C PD



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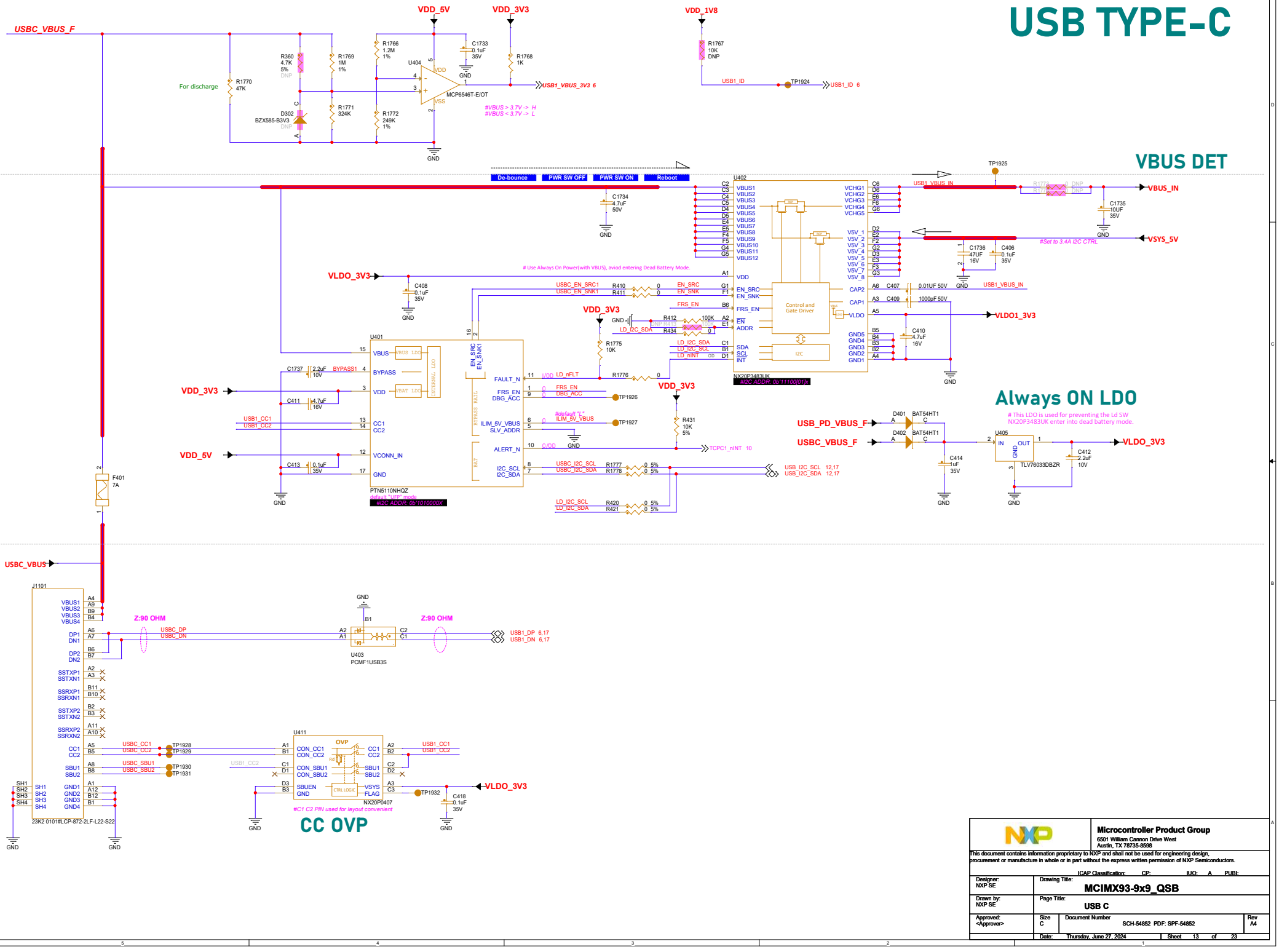
Drawn by: NXP SE	Page Title: USB PD		
Approved: <Approver>	Size C	Document Number SCH-54852 PDF: SPF-54852	Rev A4
	Date: Thursday, June 27, 2024	Sheet 12 of 23	

USB TYPE-C



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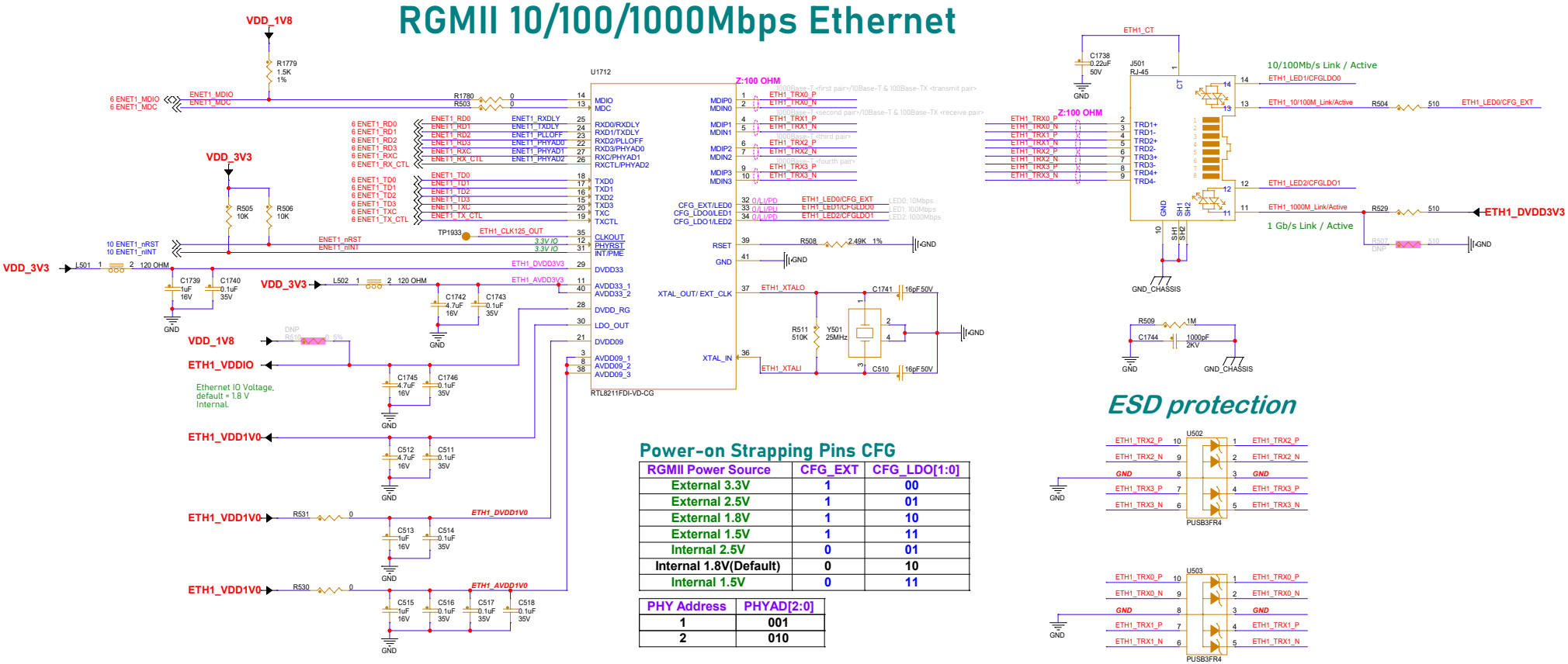
Approved: <Approver>	Size C / Document Number SCH-54852 PDF: SPF-54852	Rev A4
	Date: Thursday, June 27, 2024	Sheet 13 of 23

RGMII 10/100/1000Mbps Ethernet

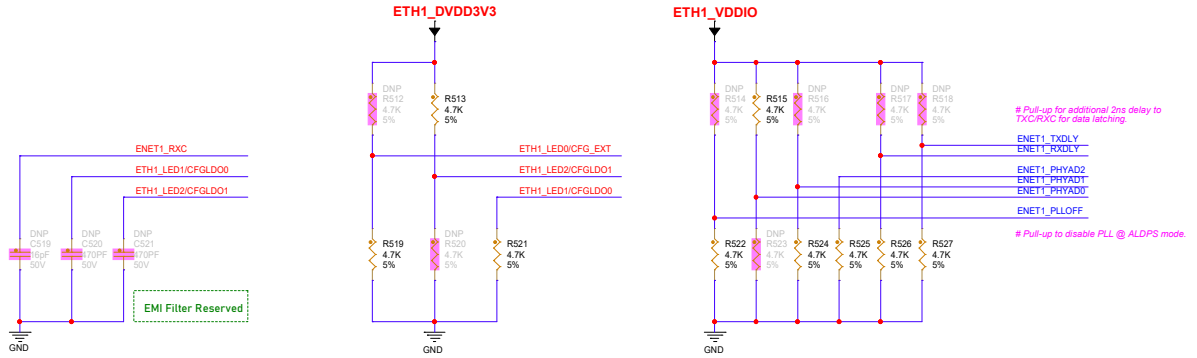


Power-on Strapping Pins CFG

RGMII Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V	1	00
External 2.5V	1	01
External 1.8V	1	10
External 1.5V	1	11
Internal 2.5V	0	01
Internal 1.8V(Default)	0	10
Internal 1.5V	0	11

PHY Address	PHYAD[2:0]
1	001
2	010

ESD protection



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Drawn by: NXP SE	Page Title: ENET1		
Approved: <Approver>	Size C	Document Number SCH-54852 PDF: SPF-54852	Rev A4
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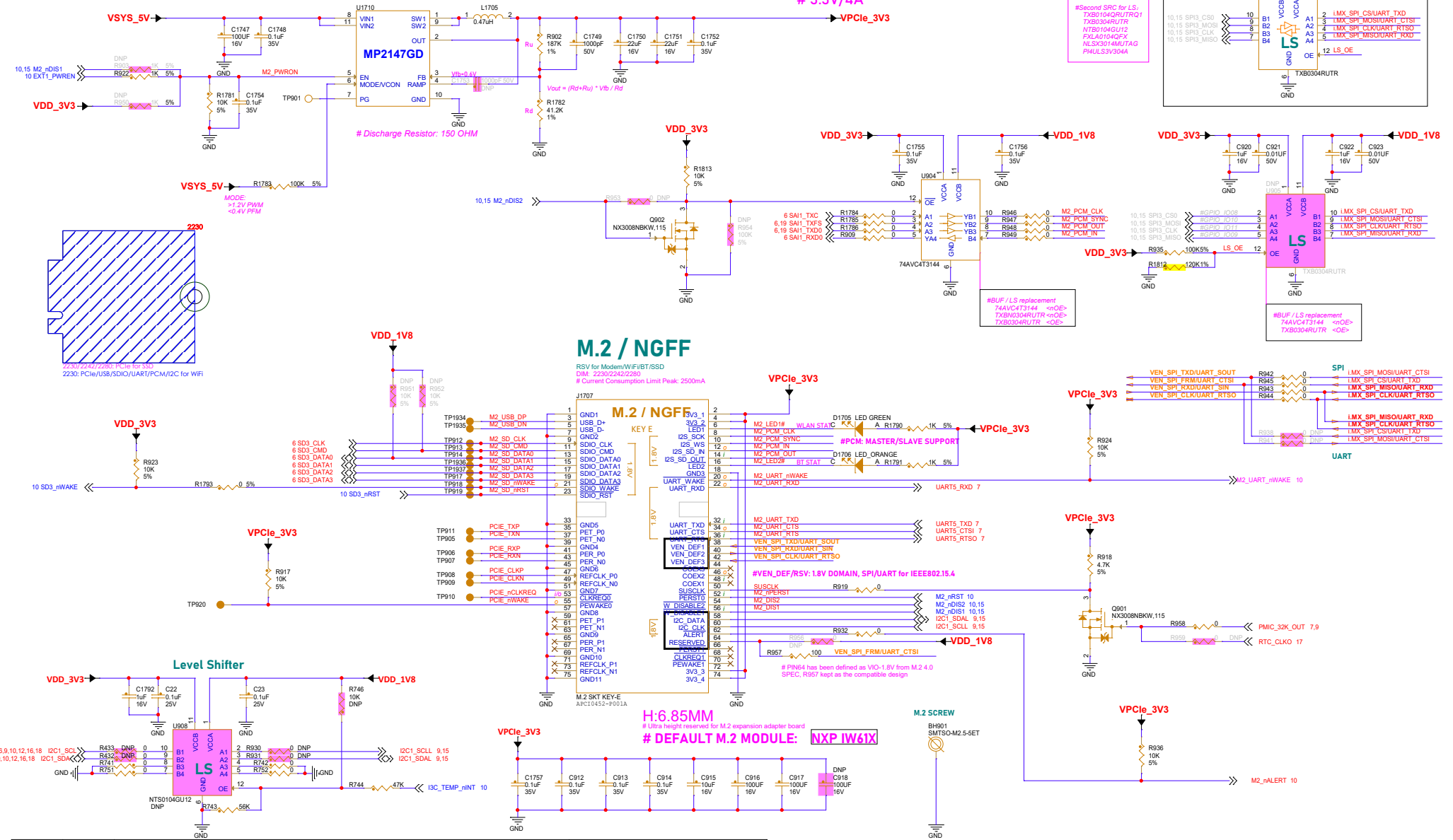
M.2 KEY-E



Key ID	Pin	Interface	Key Definition
A	8-15	2x PCIe x1 / USB 2.0 / I2C / DP x4	Display Port Based Connectivity
B	12-19	PCIe x2 / SATA / USB 2.0 / USB 3.1 Gen1 / HSIC / SSIC / Audio / UIM / I2C / SMBus	WWAN/SSD/Others Primary Key
C	16-23	PCIe/M-PCIe / USB 2.0 / USB 3.1 Gen1 / SSIC / I2C-SlimBUS / UIM / ANTCTL	WWAN Key
D	20-27	Reserved for Future Use (RFU)	RFU
E	24-31	2x PCIe x1 / USB 2.0 / I2C / SDIO / UART / PCM	SDIO Based Connectivity
F	28-35	Future Memory Interface (FMI)	Future Memory Interface
G	39-46	Not Used for M.2; for Custom/Non-Standard Apps	Generic (Not used for M.2)
H	43-50	Reserved for Future Use (RFU)	RFU
J	47-54	Reserved for Future Use (RFU)	RFU
K	51-58	Reserved for Future Use (RFU)	RFU
L	55-62	Reserved for Future Use (RFU)	RFU
M	59-66	PCIe x4 / SATA / SMBus	SSD 4 Lane PCIe

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Approved: <Approver>	Size C	Document Number SCH-54852 PDF: SPF-54852	Rev A4
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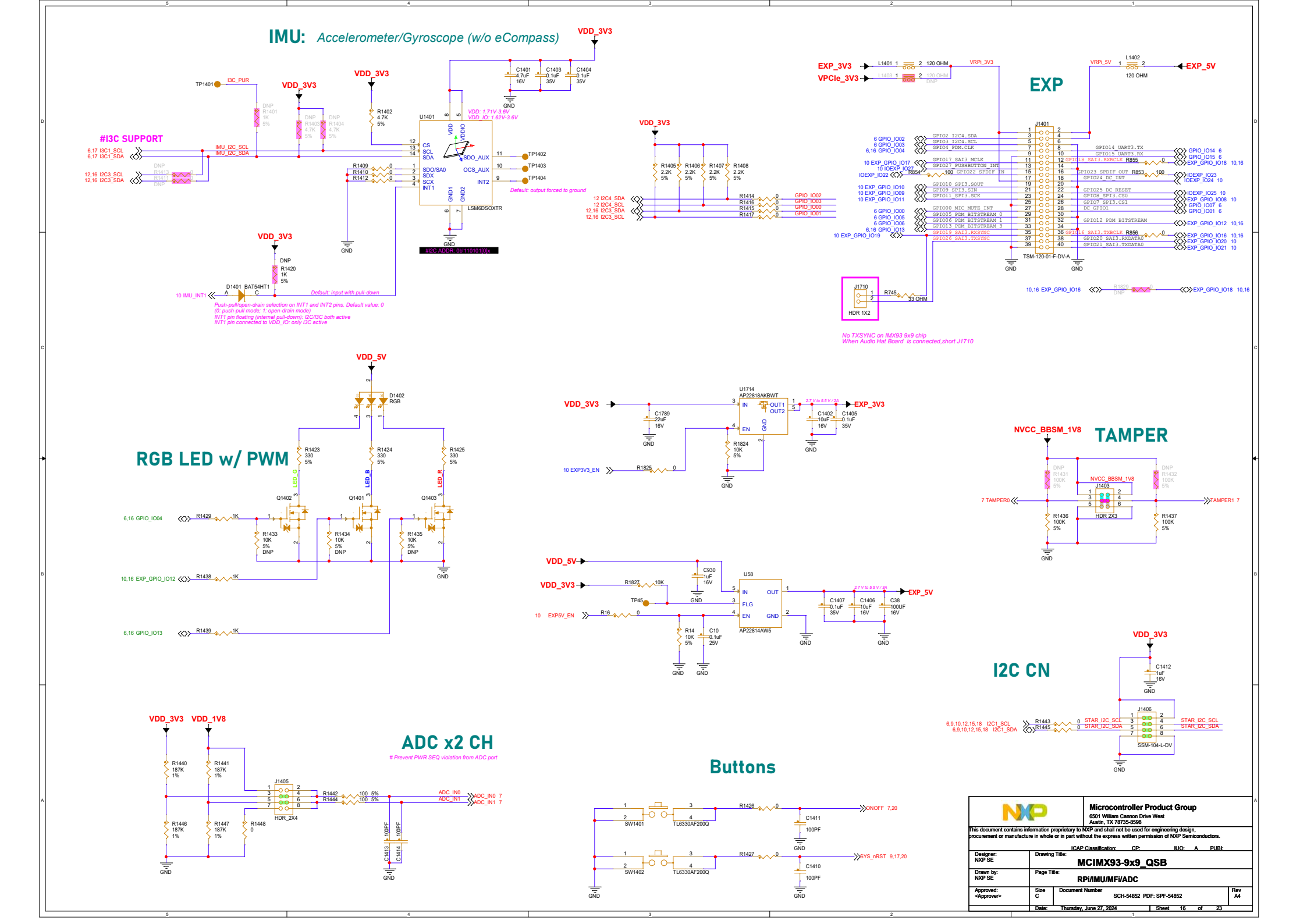
IMU: Accelerometer/Gyroscope (w/o eCompass)
#I3C SUPPORT
U1401
LSM6DSOXTR
#i2c_ADDR: 0b'110101[0]x
Default: output forced to ground
Default: input with pull-down
Push-pull/open-drain selection on INT1 and INT2 pins. Default value: 0
(0: push-pull mode; 1: open-drain mode)
INT1 pin floating (internal pull-down): I2C/I3C both active
INT1 pin connected to VDD_IO: only I3C active
EXP
EXP_3V3
VPCIe_3V3
EXP_5V
J1401
TSM-120-01-F-DV-A
J1710
HDR 1X2
No TXSYNC on IMX93 9x9 chip
When Audio Hat Board is connected,short J1710
RGB LED w/ PWM
D1402
RGB
Q1402
Q1401
Q1403
LED_G
LED_B
LED_R
U1714
AP22818AKBWT
U58
AP22814AW5
TAMPER
NVCC_BSSM_1V8
J1403
HDR 2X3
I2C CN
J1406
SSM-104-L-DV
ADC x2 CH
Prevent PWR SEQ violation from ADC port
J1405
HDR_2X4
Buttons
SW1401
SW1402
TL6330AF200Q
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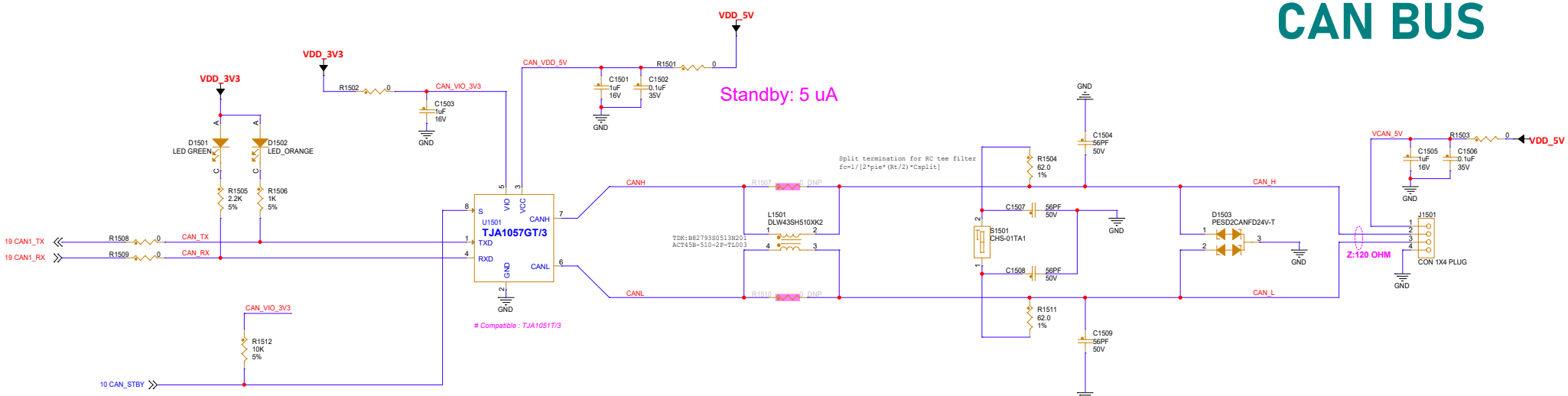
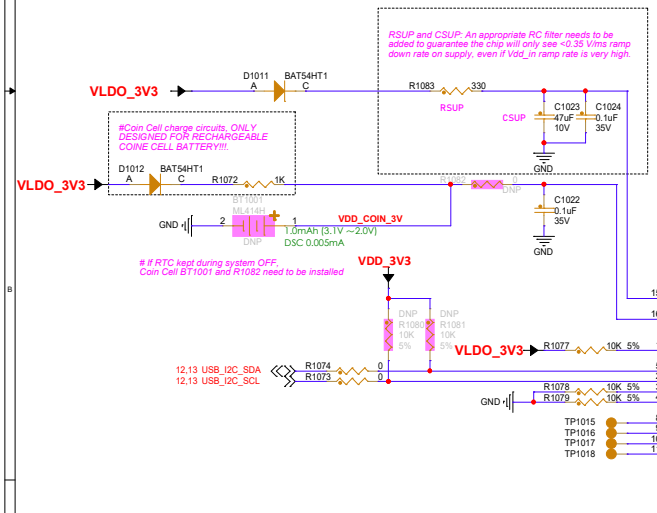
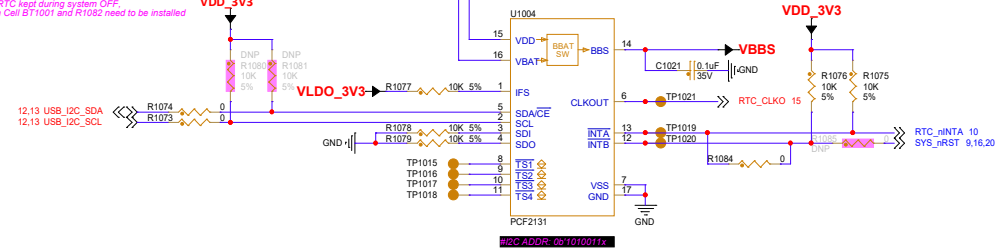
Drawing Title: MCIMX93-9x9_QSB
Page Title: RPi/IMU/MFi/ADC
Size C
Document Number SCH-54852 PDF: SPF-54852
Rev A4
Date: Thursday, June 27, 2024
Sheet 16 of 23

CAN BUS

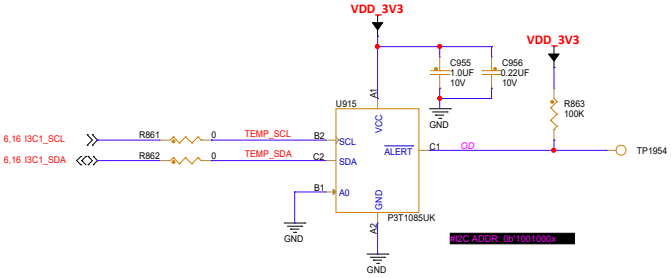


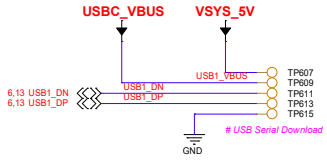


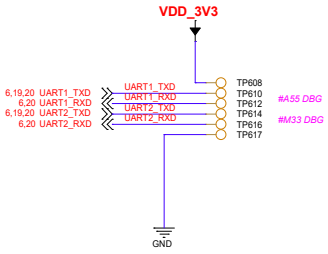
Ext. RTC

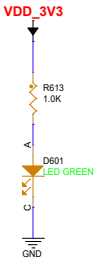


I3C TEMP SENSOR









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Approved: <Approver>	Size C	Document Number SCH-54852 PDF: SPF-54852	Rev A4
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CODEC

DCVDD	1.62V - 2.0V
DBVDD	1.62V - 3.6V
MICVDD	1.70V - 3.6V
AVDD	1.70V - 2.0V
PLLVDD	1.70V - 2.0V
CPVDD	1.70V - 2.0V
SPKVDD	1.70V - 5.5V

Layout note:
Widen the trace SPKVDD
Max ~0.6A

AUD_5V — L1205 120 OHM — C1230 22uF 16V — C1204 4.7uF 16V — C1205 4.7uF 16V — GND
VDD_3V3 — C1201 4.7uF 16V — C1231 4.7uF 16V — C1202 0.1uF 35V — GND
VDD_1V8 — L1201 120OHM — C1209 4.7uF 16V — C1207 4.7uF 16V — C1764 4.7uF 16V — C1765 0.1uF 35V — GND

U1709 WM8962BECSN/R

A2, C2	SPKVDD1, SPKVDD2
G3	DBVDD
A3	MICVDD
G2	DCVDD
D6, C6, G4	AVDD, CPVDD, PLLVDD
D7, F3, C7	AGND, DGND, CPGND
B1, C1	SPKGND1, SPKGND2
G5	PLLGND
B5	HPOUTL
A5, B4	HPOUTR, HPOUTFB
B3, A1	SPKOUTLN, SPKOUTLP
C3, B2	SPKOUTRN, SPKOUTRP
B6	CPCA
B7, A7, A6	CPCB, CPVOUTN, CPVOUTP
E4, F4, G1, E3	CLKOUT2/GPIO2, CLKOUT3/GPIO3, GPIO5, CS/GPIO6
G6	CLKOUT5
C5, A4	VMIDC, MICBIAS
C4, D4	IN1L, IN1R
D5, E5	IN2L, IN2R
F5, F6	IN3L, IN3R
E6, E7	IN4L, IN4R
F1, E2, F2	SCLK, SDA, CIFMODE
E1, D3, D1, D2	BCLK, LRCLK, DACDAT, ADCDAT
G7, F7	MCLK/XTI, XTO

HP JACK

HP_DET:
LOW : REMOVE
HIGH : PLUG

VDD_3V3 — R1202 100K — HP_J_D — R1822 0 — 10 HP_DET

L1202 120 OHM — HPOUTL
L1203 120 OHM — HPOUTR

R1823 10K 5% — R1810 10K 5% — C1769 0.1uF 35V — C1770 0.1uF 35V — R1798 20 — R1801 20 — GND

C1771 1000pF 50V DNP — C1772 1000pF 50V DNP — GND

HP_MICIN — R1800 0 — GND

HP_J_R — HP_J_L — J1201 AUD_JACK — KJ366EYS

ESD585.0ST1G — TVS1201 — TVS1202 — TVS1203 — TVS1204 — GND

3.5mm POLE — HSL HSR GND MIC — CTIA Standard

Layout note:
C1771 & C1772 close to HP Jack, for EMI purpose

Layout note:
Zobel Networks(C1769,C1770,R1798,R1801) close to WM8962B

Layout note:
R1800 close to J1201

HP MIC

MICBIAS — R1809 2.20K — C1787 1.0 UF 16V — IN1R — GND
HP_MICIN — C1788 1.0 UF 16V — IN3R

Layout note:
C1761 should be as close to the WM8962B as possible.

C1761 2.2uF — C1762 2.2uF — C1763 2.2uF — GND

VDD_3V3 — R1203 100K — R1221 100K

6,9,10,12,15,16 I2C1_SCL — R1212 0 — AUD_SCL
6,9,10,12,15,16 I2C1_SDA — R1211 0 — AUD_SDA
R1795 0 — GND

10 SAI3_RXC — R1206 0 — BCLK1
10 SAI3_RXFS — R1205 0 — LRCLK1
10 SAI3_TXD — R1207 0 — DACDAT1
10 SAI3_RXD — R1208 0 — ADCDAT1

CLKOUT2 — TP1948 — R1204 0 — AUD_nINT 10
CLKOUT5 — TP1950

10 SAI3_MCLK — R1209 0 — TP1953

MICBIAS — C1210 4.7uF 16V — GND — C1208 1.0 UF 16V — GND

Layout note:
C1210，C1208 should be as close to the WM8962B as possible.

SPK PWR

VDD_5V — C1219 22uF 16V — GND

U1202 AP22818AKBWT
IN — OUT1 — OUT2 — EN — GND
2.7 V to 5.5 V / 2A

AUD_5V

R1222 10K 5% — GND

Note:
1. Default low to reduce pop noise
2. High enable for speaker output

10 AUD_PWREN — R1219 0

SPK CN

SPK_LP — R1214 0 — C1218 15PF 16V — C1217 15PF 16V — C1221 15PF 16V — GND — SPKOUTLP — TP1942
SPK_LN — R1216 0 — SPKOUTLN — TP1943
SPK_RP — R1218 0 — C1224 15PF 16V — C1223 15PF 16V — C1227 15PF 16V — GND — SPKOUTRP — TP1944
SPK_RN — R1220 0 — SPKOUTRN — TP1945

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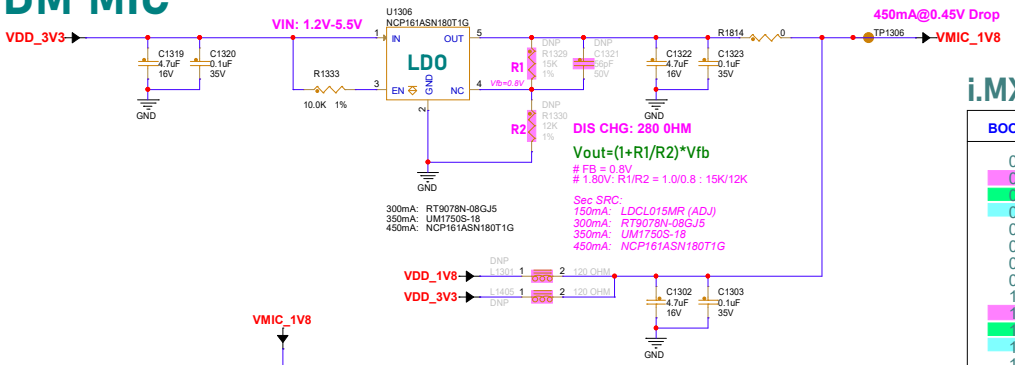
BOOT MODE CFG

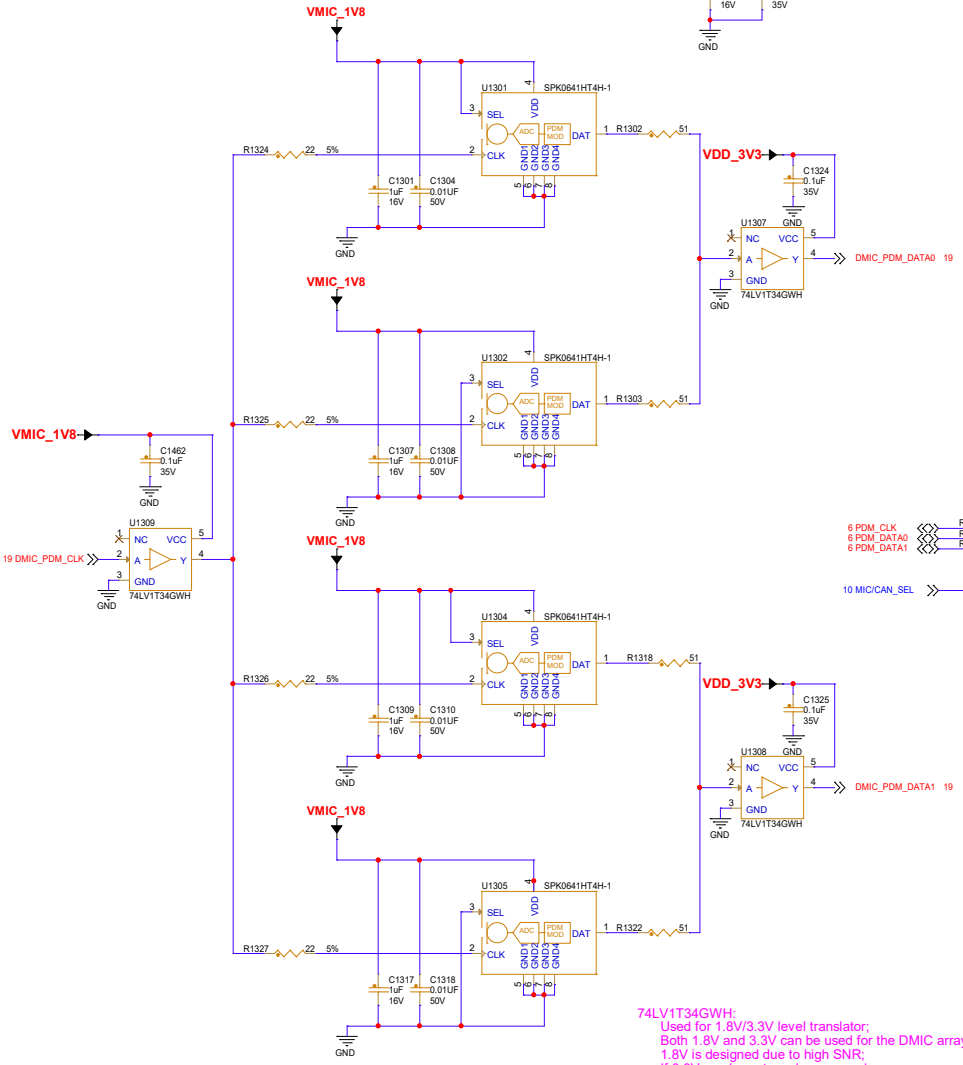
PDM MIC

LDO 1.8V for DMIC



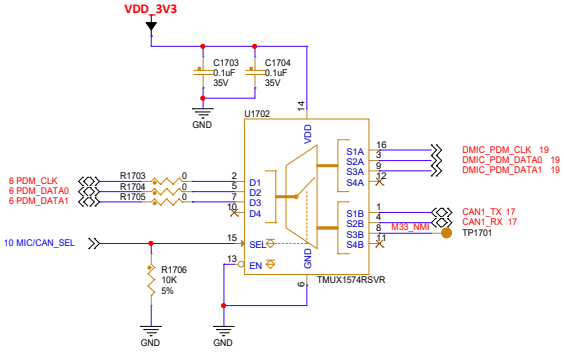
i.MX93 BOOT MODE

BOOT_MODE[3:0]	BOOT CORE	BOOT DEVICE	COMMENT
0000	Cortex-A55	From internal fuses	
0001	Cortex-A55	Serial Downloader(USB1)	USB1
0010	Cortex-A55	USDHC1 8-bit eMMC 5.1	
0011	Cortex-A55	USDHC2 4-bit SD3.0	
0100	Cortex-A55	FlexSPI Serial NOR	with SFDP (JESD-216) discoverable parameters
0101	Cortex-A55	FlexSPI Serial NAND 2K	
0110	Cortex-A55	Infinite Loop	
0111	Cortex-A55	Test Mode (A55)	
1000	Cortex-M33	LPB: Boot From Fuses	
1001	Cortex-M33	LPB: Serial Downloader (USB1)	USB1
1010	Cortex-M33	LPB: USDHC1 8-bit 1.8V eMMC 5.1	
1011	Cortex-M33	LPB: USDHC2 4-bit SD 3.0	
1100	Cortex-M33	LPB: FlexSPI Serial NOR	with SFDP (JESD-216) discoverable parameters
1101	Cortex-M33	LPB: FlexSPI Serial NAND 2K	
1110	Cortex-M33	Infinite Loop	
1111	Cortex-M33	Test Mode (For DFT ATE Test)	

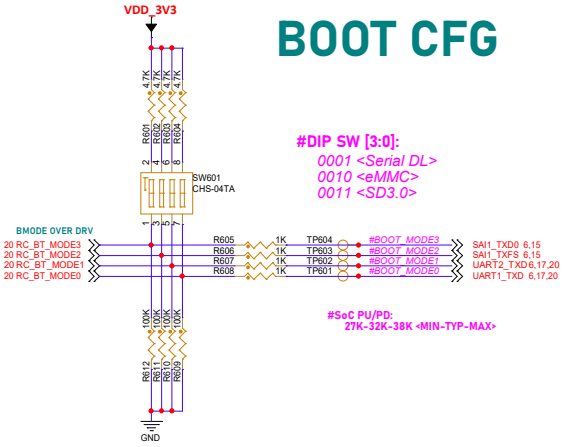


74LV1T34GWH:
Used for 1.8V/3.3V level translator;
Both 1.8V and 3.3V can be used for the DMIC array;
1.8V is designed due to high SNR;
If 3.3V used, part can be removed;

MIC/CAN



BOOT CFG



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REMOTE DEBUG

REMOVE THIS PAGE IF NOT USED!!!

FT PWR

System ID (Back up)

UI LED

IO EXP

FT4232H

U1706

UART BUF

BOOT MODE RC

ONOFF / RST RC

JTAG DBG

SYS TST/ MONITOR

JTAG HDR

i.MX SoC RC I/F

DIP SW

FT-IO EXP

BTN

FT-GPIO

JTAG CN

CPU

STATUS LED

LED	COLOR	ON	OFF
D1410	RED	SYS PWR ON	SYS OFF
D1411	ORANGE	FTDI SUSPEND	FTDI RUN
D1412	RED	Local DBG	Remote DBG
D1413	GREEN	Remote DBG	Local DBG
D1414	ORANGE	WDOG_B TRIG	NORMAL
D1415	ORANGE	SYS SUSPEND	RUN

SEL=H, VTREF= OFF, remote JTAG

SEL=L, VTREF= ON, local JTAG (default)

Power-on default state is input with 100K pull-up

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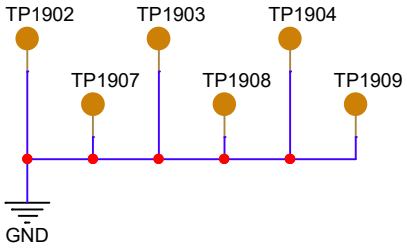
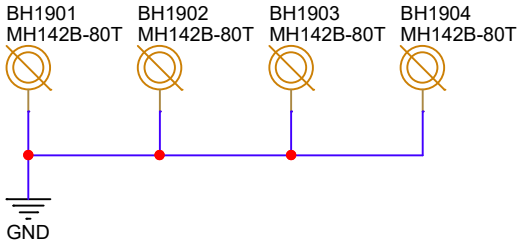
Drawn by: NXP SE	Page Title: Remote Debug
Approved: <Approver>	Size: D; Document Number: SCH-54852 PDF: SPF-54852; Rev: A4
	Date: Thursday, June 27, 2024; Sheet 20 of 23

GND TP

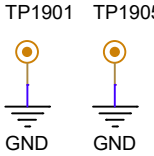


SCREW HOLE



GND TESTLOOP

TOP Layer



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Drawn by: NXP SE	Page Title: **Mechanics**		
Approved: <Approver>	Size A	Document Number SCH-54852 PDF: SPF-54852	Rev A4
	Date: Thursday, June 27, 2024	Sheet 21 of 23	

NOTE:

I2C DEV TABLE

PART	DEVICE	I2C ADDR	PORT	SPEED	VOL	DESCRIPTION
U801	PCAL6524HEAZ	0x22 (0b'01000[10]x)	MX-I2C2	1MHz Fm+	3.3V	IO EXP for IRQ/OUTPUT
U301	PTN5110NHQZ	0x52 (0b'10100[10]x)	MX-I2C1	400KHz	3.3V	USB C PD PHY
U401	PTN5110NHQZ	0x50 (0b'10100[00]x)	MX-I2C1	400KHz	3.3V	USB C PD PHY
U402	NX20P3483UK	0x71 (0b'11100[01]x)	MX-I2C1	400KHz	3.3V	USB Load Switch
U1401	LSM6DSOXTR	0x6A (0b'110101[0]x)	MX-I2C1/I2C3	I3C/I2C-400KHz	3.3V	IMU (I3C support)
U1709	WM8962B	0x1A (0b'0011010x)	MX-I2C1	526KHz	3.3V	Audio CODEC
U701	PCA9451AHN	0x25 (0b'0100101x)	MX-I2C2	1MHz Fm+	3.3V	PMIC
U1409	PCA9655EMTTXG	0x21 (0b'0100001)	FTDI-I2C	1MHz Fm+	3.3V	RDPM IO EXP
U915	P3T1085UK	0x48 (0b'1001000x)	MX-I2C1	I3C/I2C-400KHz	3.3V	Temp Sensor (I3C support)
U1004	PCF2131TF	0x53 (0b'1010011x)	MX-I2C1	400KHz	3.3V	Ext RTC

Microcontroller Product Group
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i.MX93 IOMUX:

IOPAD	Alt0	Alt1	Alt2	Alt3	Alt4	Alt5	Alt6	Alt7	DEF MUX	Reset Status
RTC_XTALI	bbsmmix.RTC								bbsmmix.RTC	
RTC_XTALO										
PMIC_STBY_REQ	bbsmmix.PMIC_STBY_REQ								ccmsrcgpcmix.PMIC_STBY_REQ	output low w/o PU/PD
PMIC_ON_REQ	bbsmmix.PMIC_ON_REQ								bbsmmix.PMIC_ON_REQ	output high w/o PU/PD
ONOFF	bbsmmix.ONOFF								bbsmmix.ONOFF	input w/o PU/PD
POR_B	bbsmmix.POR_B								bbsmmix.POR_B	input w/o PU/PD
TAMPER0	bbsmmix.TAMPER0								bbsmmix.TAMPER0	input w/ PU
TAMPER1	bbsmmix.TAMPER1								bbsmmix.TAMPER1	input w/ PU
GPIO_IO00	gpio2.IO[0]	i2c3.SDA	isi.PCLK	lcdif.PCLK	spi6.PCS0	uart5.TX	i2c5.SDA	flexio1.FLEXIO[0]	gpio2.IO[0]	input w/ PD
GPIO_IO01	gpio2.IO[1]	i2c3.SCL	isi.D[0]	lcdif.DE	spi6.SIN	uart5.RX	i2c5.SCL	flexio1.FLEXIO[1]	gpio2.IO[1]	input w/ PD
GPIO_IO02	gpio2.IO[2]	i2c4.SDA	isi.FRAME_VALID	lcdif.VSYNC	spi6.SOUT	uart5.CTS_B	i2c6.SDA	flexio1.FLEXIO[2]	gpio2.IO[2]	input w/ PD
GPIO_IO03	gpio2.IO[3]	i2c4.SCL	isi.LINE_VALID	lcdif.HSYNC	spi6.SCK	uart5.RTS_B	i2c6.SCL	flexio1.FLEXIO[3]	gpio2.IO[3]	input w/ PD
GPIO_IO04	gpio2.IO[4]	tpm3.CH0	pdm.CLK	lcdif.D[0]	spi7.PCS0	uart6.TX	i2c6.SDA	flexio1.FLEXIO[4]	gpio2.IO[4]	input w/ PD
GPIO_IO05	gpio2.IO[5]	tpm4.CH0	pdm.BIT_STREAM[0]	lcdif.D[1]	spi7.SIN	uart6.RX	i2c6.SCL	flexio1.FLEXIO[5]	gpio2.IO[5]	input w/ PD
GPIO_IO06	gpio2.IO[6]	tpm5.CH0	pdm.BIT_STREAM[1]	lcdif.D[2]	spi7.SOUT	uart6.CTS_B	i2c7.SDA	flexio1.FLEXIO[6]	gpio2.IO[6]	input w/ PD
GPIO_IO07	gpio2.IO[7]	spi3.PCS1	isi.D[1]	lcdif.D[3]	spi7.SCK	uart6.RTS_B	i2c7.SCL	flexio1.FLEXIO[7]	gpio2.IO[7]	input w/ PD
GPIO_IO08	gpio2.IO[8]	spi3.PCS0	isi.D[2]	lcdif.D[4]	tpm6.CH0	uart7.TX	i2c7.SDA	flexio1.FLEXIO[8]	gpio2.IO[8]	input w/ PD
GPIO_IO09	gpio2.IO[9]	spi3.SIN	isi.D[3]	lcdif.D[5]	tpm3.EXTCLK	uart7.RX	i2c7.SCL	flexio1.FLEXIO[9]	gpio2.IO[9]	input w/ PD
GPIO_IO10	gpio2.IO[10]	spi3.SOUT	isi.D[4]	lcdif.D[6]	tpm4.EXTCLK	uart7.CTS_B	i2c8.SDA	flexio1.FLEXIO[10]	gpio2.IO[10]	input w/ PD
GPIO_IO11	gpio2.IO[11]	spi3.SCK	isi.D[5]	lcdif.D[7]	tpm5.EXTCLK	uart7.RTS_B	i2c8.SCL	flexio1.FLEXIO[11]	gpio2.IO[11]	input w/ PD
GPIO_IO12	gpio2.IO[12]	tpm3.CH2	pdm.BIT_STREAM[2]	lcdif.D[8]	spi8.PCS0	uart8.TX	i2c8.SDA	sai3.RX_SYNC	gpio2.IO[12]	input w/ PD
GPIO_IO13	gpio2.IO[13]	tpm4.CH2	pdm.BIT_STREAM[3]	lcdif.D[9]	spi8.SIN	uart8.RX	i2c8.SCL	flexio1.FLEXIO[13]	gpio2.IO[13]	input w/ PD
GPIO_IO14	gpio2.IO[14]	uart3.TX	isi.D[6]	lcdif.D[10]	spi8.SOUT	uart8.CTS_B	uart4.TX	flexio1.FLEXIO[14]	gpio2.IO[14]	input w/ PD
GPIO_IO15	gpio2.IO[15]	uart3.RX	isi.D[7]	lcdif.D[11]	spi8.SCK	uart8.RTS_B	uart4.RX	flexio1.FLEXIO[15]	gpio2.IO[15]	input w/ PD
GPIO_IO16	gpio2.IO[16]	sai3.TX_BCLK	pdm.BIT_STREAM[2]	lcdif.D[12]	uart3.CTS_B	spi4.PCS2	uart4.CTS_B	flexio1.FLEXIO[16]	gpio2.IO[16]	input w/ PD
GPIO_IO17	gpio2.IO[17]	sai3.MCLK	isi.D[8]	lcdif.D[13]	uart3.RTS_B	spi4.PCS1	uart4.RTS_B	flexio1.FLEXIO[17]	gpio2.IO[17]	input w/ PD
GPIO_IO18	gpio2.IO[18]	sai3.RX_BCLK	isi.D[9]	lcdif.D[14]	spi5.PCS0	spi4.PCS0	tpm5.CH2	flexio1.FLEXIO[18]	gpio2.IO[18]	input w/ PD
GPIO_IO19	gpio2.IO[19]	sai3.RX_SYNC	pdm.BIT_STREAM[3]	lcdif.D[15]	spi5.SIN	spi4.SIN	tpm6.CH2	sai3.TX_DATA[0]	gpio2.IO[19]	input w/ PD
GPIO_IO20	gpio2.IO[20]	sai3.RX_DATA[0]	pdm.BIT_STREAM[0]	lcdif.D[16]	spi5.SOUT	spi4.SOUT	tpm3.CH1	flexio1.FLEXIO[20]	gpio2.IO[20]	input w/ PD
GPIO_IO21	gpio2.IO[21]	sai3.TX_DATA[0]	pdm.CLK	lcdif.D[17]	spi5.SCK	spi4.SCK	tpm4.CH1	sai3.RX_BCLK	gpio2.IO[21]	input w/ PD
GPIO_IO22	gpio2.IO[22]	usdhc3.CLK	spdif1.IN	lcdif.D[18]	tpm5.CH1	tpm6.EXTCLK	i2c5.SDA	flexio1.FLEXIO[22]	gpio2.IO[22]	input w/ PD
GPIO_IO23	gpio2.IO[23]	usdhc3.CMD	spdif1.OUT	lcdif.D[19]	tpm6.CH1		i2c5.SCL	flexio1.FLEXIO[23]	gpio2.IO[23]	input w/ PD
GPIO_IO24	gpio2.IO[24]	usdhc3.DATA0		lcdif.D[20]	tpm3.CH3	dap.TDO_TRACESWO	spi6.PCS1	flexio1.FLEXIO[24]	gpio2.IO[24]	input w/ PD
GPIO_IO25	gpio2.IO[25]	usdhc3.DATA1	can2.TX	lcdif.D[21]	tpm4.CH3	dap.TCLK_SWCLK	spi7.PCS1	flexio1.FLEXIO[25]	gpio2.IO[25]	input w/ PD
GPIO_IO26	gpio2.IO[26]	usdhc3.DATA2	pdm.BIT_STREAM[1]	lcdif.D[22]	tpm5.CH3	dap.TDI	spi8.PCS1	sai3.TX_SYNC	gpio2.IO[26]	input w/ PD
GPIO_IO27	gpio2.IO[27]	usdhc3.DATA3	can2.RX	lcdif.D[23]	tpm6.CH3	dap.TMS_SWDIO	spi5.PCS1	flexio1.FLEXIO[27]	gpio2.IO[27]	input w/ PD
GPIO_IO28	gpio2.IO[28]	i2c3.SDA						flexio1.FLEXIO[28]	gpio2.IO[28]	input w/ PD
GPIO_IO29	gpio2.IO[29]	i2c3.SCL						flexio1.FLEXIO[29]	gpio2.IO[29]	input w/ PD
CCM_CLKO1	ccmsrcgpcmix.CLKO1				flexio1.FLEXIO[26]	gpio3.IO[26]			ccmsrcgpcmix.CLKO1	input w/ PU
CCM_CLKO2	ccmsrcgpcmix.CLKO2				flexio1.FLEXIO[27]	gpio3.IO[27]			ccmsrcgpcmix.CLKO2	input w/ PU
CCM_CLKO3	ccmsrcgpcmix.CLKO3				flexio2.FLEXIO[28]	gpio4.IO[28]			gpio4.IO[28]	input w/ PU
CCM_CLKO4	ccmsrcgpcmix.CLKO4				flexio2.FLEXIO[29]	gpio4.IO[29]			gpio4.IO[29]	input w/ PU
DAP_TDI	dap.TDI	mqs2.LEFT		can2.TX	flexio2.FLEXIO[30]	gpio3.IO[28]	uart5.RX		dap.TDI	input w/ PU
DAP_TMS_SWDIO	dap.TMS_SWDIO				flexio2.FLEXIO[31]	gpio3.IO[29]	uart5.RTS_B		dap.TMS_SWDIO	input w/ PU
DAP_TCLK_SWCLK	dap.TCLK_SWCLK				flexio1.FLEXIO[30]	gpio3.IO[30]	uart5.CTS_B		dap.TCLK_SWCLK	input w/ PD
DAP_TDO_TRACESWO	dap.TDO_TRACESWO	mqs2.RIGHT		can2.RX	flexio1.FLEXIO[31]	gpio3.IO[31]	uart5.TX		dap.TDO_TRACESWO	input w/ PD
ENET1_MDC	enet_qos.MDC	uart3.DCB_B	i3c2.SCL	usb1.OTG_ID	flexio2.FLEXIO[0]	gpio4.IO[0]			gpio4.IO[0]	input w/ PD
ENET1_MDIO	enet_qos.MDIO	uart3.RIN_B	i3c2.SDA	usb1.OTG_PWR	flexio2.FLEXIO[1]	gpio4.IO[1]			gpio4.IO[1]	input w/ PD
ENET1_TD3	enet_qos.RGMII_TD3		can2.TX	usb2.OTG_ID	flexio2.FLEXIO[2]	gpio4.IO[2]			gpio4.IO[2]	input w/ PD
ENET1_TD2	enet_qos.RGMII_TD2	enet_qos.TX_CLK/.ENET_REF_CLK_ROOT	can2.RX	usb2.OTG_OC	flexio2.FLEXIO[3]	gpio4.IO[3]			gpio4.IO[3]	input w/ PD
ENET1_TD1	enet_qos.RGMII_TD1	uart3.RTS_B	i3c2.PUR	usb1.OTG_OC	flexio2.FLEXIO[4]	gpio4.IO[4]	i3c2.PUR_B		gpio4.IO[4]	input w/ PD
ENET1_TD0	enet_qos.RGMII_TD0	uart3.TX			flexio2.FLEXIO[5]	gpio4.IO[5]			gpio4.IO[5]	input w/ PD
ENET1_TX_CTL	enet_qos.RGMII_TX_CTL	uart3.DTR_B			flexio2.FLEXIO[6]	gpio4.IO[6]			gpio4.IO[6]	input w/ PD
ENET1_TXC	enet_qos.RGMII_TXC	enet_qos.TX_ER			flexio2.FLEXIO[7]	gpio4.IO[7]			gpio4.IO[7]	input w/ PD
ENET1_RX_CTL	enet_qos.RGMII_RX_CTL	uart3.DSR_B		usb2.OTG_PWR	flexio2.FLEXIO[8]	gpio4.IO[8]			gpio4.IO[8]	input w/ PD
ENET1_RXC	enet_qos.RGMII_RXC	enet_qos.RX_ER			flexio2.FLEXIO[9]	gpio4.IO[9]			gpio4.IO[9]	input w/ PD
ENET1_RD0	enet_qos.RGMII_RD0	uart3.RX			flexio2.FLEXIO[10]	gpio4.IO[10]			gpio4.IO[10]	input w/ PD
ENET1_RD1	enet_qos.RGMII_RD1	uart3.CTS_B		lptmr2.ALT1	flexio2.FLEXIO[11]	gpio4.IO[11]			gpio4.IO[11]	input w/ PD
ENET1_RD2	enet_qos.RGMII_RD2			lptmr2.ALT2	flexio2.FLEXIO[12]	gpio4.IO[12]			gpio4.IO[12]	input w/ PD
ENET1_RD3	enet_qos.RGMII_RD3		wakeupmix.flexspi_usdhc_tester_trigger	lptmr2.ALT3	flexio2.FLEXIO[13]	gpio4.IO[13]			gpio4.IO[13]	input w/ PD
ENET2_MDC	enet2.MDC	uart4.DCB_B	sai2.RX_SYNC		flexio2.FLEXIO[14]	gpio4.IO[14]			gpio4.IO[14]	input w/ PD
ENET2_MDIO	enet2.MDIO	uart4.RIN_B	sai2.RX_BCLK		flexio2.FLEXIO[15]	gpio4.IO[15]			gpio4.IO[15]	input w/ PD
ENET2_TD3	enet2.RGMII_TD3		sai2.RX_DATA[0]		flexio2.FLEXIO[16]	gpio4.IO[16]			gpio4.IO[16]	input w/ PD
ENET2_TD2	enet2.RGMII_TD2	enet2.TX_CLK/ENET_REF_CLK_ROOT	sai2.RX_DATA[1]		flexio2.FLEXIO[17]	gpio4.IO[17]			gpio4.IO[17]	input w/ PD
ENET2_TD1	enet2.RGMII_TD1	uart4.RTS_B	sai2.RX_DATA[2]		flexio2.FLEXIO[18]	gpio4.IO[18]			gpio4.IO[18]	input w/ PD
ENET2_TD0	enet2.RGMII_TD0	uart4.TX	sai2.RX_DATA[3]		flexio2.FLEXIO[19]	gpio4.IO[19]			gpio4.IO[19]	input w/ PD
ENET2_TX_CTL	enet2.RGMII_TX_CTL	uart4.DTR_B	sai2.TX_SYNC		flexio2.FLEXIO[20]	gpio4.IO[20]			gpio4.IO[20]	input w/ PD
ENET2_TXC	enet2.RGMII_TXC	enet2.TX_ER	sai2.TX_BCLK		flexio2.FLEXIO[21]	gpio4.IO[21]			gpio4.IO[21]	input w/ PD
ENET2_RX_CTL	enet2.RGMII_RX_CTL	uart4.DSR_B	sai2.TX_DATA[0]		flexio2.FLEXIO[22]	gpio4.IO[22]			gpio4.IO[22]	input w/ PD
ENET2_RXC	enet2.RGMII_RXC	enet2.RX_ER	sai2.TX_DATA[1]		flexio2.FLEXIO[23]	gpio4.IO[23]			gpio4.IO[23]	input w/ PD
ENET2_RD0	enet2.RGMII_RD0	uart4.RX	sai2.TX_DATA[2]		flexio2.FLEXIO[24]	gpio4.IO[24]			gpio4.IO[24]	input w/ PD
ENET2_RD1	enet2.RGMII_RD1	spdif1.IN	sai2.TX_DATA[3]		flexio2.FLEXIO[25]	gpio4.IO[25]			gpio4.IO[25]	input w/ PD
ENET2_RD2	enet2.RGMII_RD2	uart4.CTS_B	sai2.MCLK	mqs2.RIGHT	flexio2.FLEXIO[26]	gpio4.IO[26]			gpio4.IO[26]	input w/ PD
ENET2_RD3	enet2.RGMII_RD3	spdif1.OUT	spdif1.IN	mqs2.LEFT	flexio2.FLEXIO[27]	gpio4.IO[27]			gpio4.IO[27]	input w/ PD
SD1_CLK	usdhc1.CLK				flexio1.FLEXIO[8]	gpio3.IO[8]			gpio3.IO[8]	input w/ PD
SD1_CMD	usdhc1.CMD				flexio1.FLEXIO[9]	gpio3.IO[9]			gpio3.IO[9]	input w/ PD
SD1_DATA0	usdhc1.DATA0				flexio1.FLEXIO[10]	gpio3.IO[10]			gpio3.IO[10]	input w/ PD
SD1_DATA1	usdhc1.DATA1				flexio1.FLEXIO[11]	gpio3.IO[11]			gpio3.IO[11]	input w/ PD
SD1_DATA2	usdhc1.DATA2				flexio1.FLEXIO[12]	gpio3.IO[12]			gpio3.IO[12]	input w/ PD
SD1_DATA3	usdhc1.DATA3	flexspi.A_SS1_B			flexio1.FLEXIO[13]	gpio3.IO[13]			gpio3.IO[13]	input w/ PD
SD1_DATA4	usdhc1.DATA4	flexspi.A_DATA[4]			flexio1.FLEXIO[14]	gpio3.IO[14]			gpio3.IO[14]	input w/ PD
SD1_DATA5	usdhc1.DATA5	flexspi.A_DATA[5]	usdhc1.RESET_B		flexio1.FLEXIO[15]	gpio3.IO[15]			gpio3.IO[15]	input w/ PD
SD1_DATA6	usdhc1.DATA6	flexspi.A_DATA[6]	usdhc1.CD_B		flexio1.FLEXIO[16]	gpio3.IO[16]			gpio3.IO[16]	input w/ PD
SD1_DATA7	usdhc1.DATA7	flexspi.A_DATA[7]	usdhc1.WP		flexio1.FLEXIO[17]	gpio3.IO[17]			gpio3.IO[17]	input w/ PD
SD1_STROBE	usdhc1.STROBE	flexspi.A_DQS			flexio1.FLEXIO[18]	gpio3.IO[18]			gpio3.IO[18]	input w/o PU/PD
SD2_VSELECT	usdhc2.VSELECT	usdhc2.WP	lptmr2.ALT3		flexio1.FLEXIO[19]	gpio3.IO[19]			gpio3.IO[19]	input w/ PD
SD3_CLK	usdhc3.CLK	flexspi.A_SCLK			flexio1.FLEXIO[20]	gpio3.IO[20]			gpio3.IO[20]	input w/ PD
SD3_CMD	usdhc3.CMD	flexspi.A_SS0_B			flexio1.FLEXIO[21]	gpio3.IO[21]			gpio3.IO[21]	input w/ PD
SD3_DATA0	usdhc3.DATA0	flexspi.A_DATA[0]			flexio1.FLEXIO[22]	gpio3.IO[22]			gpio3.IO[22]	input w/ PD
SD3_DATA1	usdhc3.DATA1	flexspi.A_DATA[1]			flexio1.FLEXIO[23]	gpio3.IO[23]			gpio3.IO[23]	input w/ PD
SD3_DATA2	usdhc3.DATA2	flexspi.A_DATA[2]			flexio1.FLEXIO[24]	gpio3.IO[24]			gpio3.IO[24]	input w/ PD
SD3_DATA3	usdhc3.DATA3	flexspi.A_DATA[3]			flexio1.FLEXIO[25]	gpio3.IO[25]			gpio3.IO[25]	input w/ PD
SD2_CD_B	usdhc2.CD_B	enet_qos.1588_EVENT0_IN	i3c2.SCL		flexio1.FLEXIO[0]	gpio3.IO[0]			gpio3.IO[0]	input w/ PD
SD2_CLK	usdhc2.CLK	enet_qos.1588_EVENT0_OUT	i3c2.SDA		flexio1.FLEXIO[1]	gpio3.IO[1]			gpio3.IO[1]	input w/ PD
SD2_CMD	usdhc2.CMD	enet2.1588_EVENT0_IN	i3c2.PUR	i3c2.PUR_B	flexio1.FLEXIO[2]	gpio3.IO[2]			gpio3.IO[2]	input w/ PD
SD2_DATA0	usdhc2.DATA0	enet2.1588_EVENT0_OUT	can2.TX		flexio1.FLEXIO[3]	gpio3.IO[3]	i3c1.PUR_B		gpio3.IO[3]	input w/ PD
SD2_DATA1	usdhc2.DATA1	enet2.1588_EVENT1_IN	can2.RX		flexio1.FLEXIO[4]	gpio3.IO[4]			gpio3.IO[4]	input w/ PD
SD2_DATA2	usdhc2.DATA2	enet2.1588_EVENT1_OUT	mqs2.RIGHT		flexio1.FLEXIO[5]	gpio3.IO[5]			gpio3.IO[5]	input w/ PD
SD2_DATA3	usdhc2.DATA3	lptmr2.ALT1	mqs2.LEFT		flexio1.FLEXIO[6]	gpio3.IO[6]			gpio3.IO[6]	input w/ PD
SD2_RESET_B	usdhc2.RESET_B	lptmr2.ALT2			flexio1.FLEXIO[7]	gpio3.IO[7]			gpio3.IO[7]	input w/ PD
I2C1_SCL	i2c1.SCL	i3c1.SCL	uart1.DCB_B	tpm2.CH0		gpio1.IO[0]			gpio1.IO[0]	input w/ PD
I2C1_SDA	i2c1.SDA	i3c1.SDA	uart1.RIN_B	tpm2.CH1		gpio1.IO[1]	can1.TX		gpio1.IO[1]	input w/ PD
I2C2_SCL	i2c2.SCL	i3c1.PUR	uart2.DCB_B	tpm2.CH2	sai1.RX_SYNC	gpio1.IO[2]	can1.RX		gpio1.IO[2]	input w/ PD
I2C2_SDA	i2c2.SDA		uart2.RIN_B	tpm2.CH3	sai1.RX_BCLK	gpio1.IO[3]			gpio1.IO[3]	input w/ PD
UART1_RXD	uart1.RX	seco.RX	spi2.SIN	tpm1.CH0		gpio1.IO[4]			gpio1.IO[4]	input w/ PD
UART1_TXD	uart1.TX	seco.TX	spi2.PCS0	tpm1.CH1		gpio1.IO[5]/ccmsrcgpcmix.BOOT_MODE[0]			gpio1.IO[5]/ccmsrcgpcmix.BOOT_MODE[0]	input w/ PD
UART2_RXD	uart2.RX	uart1.CTS_B	spi2.SOUT	tpm1.CH2	sai1.MCLK	gpio1.IO[6]			gpio1.IO[6]	input w/ PD
UART2_TXD	uart2.TX	uart1.RTS_B	spi2.SCK	tpm1.CH3		gpio1.IO[7]/ccmsrcgpcmix.BOOT_MODE[1]			gpio1.IO[7]/ccmsrcgpcmix.BOOT_MODE[1]	input w/ PD
PDM_CLK	pdm.CLK	mqs1.LEFT			lptmr1.ALT1	gpio1.IO[8]			gpio1.IO[8]	input w/ PD
PDM_BIT_STREAM0	pdm.BIT_STREAM[0]	mqs1.RIGHT	spi1.PCS1	tpm1.EXTCLK	lptmr1.ALT2	gpio1.IO[9]			gpio1.IO[9]	input w/ PD
PDM_BIT_STREAM1	pdm.BIT_STREAM[1]	m33.NMI	spi2.PCS1	tpm2.EXTCLK	lptmr1.ALT3	gpio1.IO[10]			gpio1.IO[10]	input w/ PD
SAI1_TXFS	sai1.TX_SYNC	sai1.TX_DATA[1]	spi1.PCS0	uart2.DTR_B	mqs1.LEFT	gpio1.IO[11]/ccmsrcgpcmix.BOOT_MODE[2]			gpio1.IO[11]/ccmsrcgpcmix.BOOT_MODE[2]	input w/ PD
SAI1_TXC	sai1.TX_BCLK	uart2.CTS_B	spi1.SIN	uart1.DSR_B	can1.RX	gpio1.IO[12]			gpio1.IO[12]	input w/ PD
SAI1_TXD0	sai1.TX_DATA[0]	uart2.RTS_B	spi1.SCK	uart1.DTR_B	can1.TX	gpio1.IO[13]/ccmsrcgpcmix.BOOT_MODE[3]			gpio1.IO[13]/ccmsrcgpcmix.BOOT_MODE[3]	input w/ PD
SAI1_RXD0	sai1.RX_DATA[0]	sai1.MCLK	spi1.SOUT	uart2.DSR_B	mqs1.RIGHT	gpio1.IO[14]			gpio1.IO[14]	input w/ PD
WDOG_ANY	wdog1.WDOG_ANY					gpio1.IO[15]			gpio1.IO[15]	input w/ PD
CLKIN1	anamix.CLKIN1	anamix.esd_diode								input w/o PU/PD
CLKIN2	anamix.CLKIN2	anamix.atx								input w/o PU/PD
XTALI_24M	anamix.xtali_24M									
XTALO_24M	anamix.xtalo_24M									
ADC_IN0	anamix.adc_in0									input w/o PU/PD
ADC_IN1	anamix.adc_in1									input w/o PU/PD
ADC_IN2	anamix.adc_in2									input w/o PU/PD
ADC_IN3	anamix.adc_in3									input w/o PU/PD

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