

Table of Content

Page 1	TITLE PAGE
Page 2	USB Supply Interface
Page 3	System Power
Page 4	RT6xx IO
Page 5	Memory
Page 6	Audio Code
Page 7	DMIC
Page 8	Audio Amp - class-D
Page 9	Pmod / UART/Flexcomm
Page 10	Pheriperals
Page 11	SD & M2 mini card
Page 12	System Reset / Debug Trace
Page 13	Debug UART
Page 14	Link2 Debug

X-MIMXRT685-EVK

POWER MANAGEMENT

INPUT	NET/ PWR NAME	OUTPUT VOLTAGE
TARGET USB USB AB	USB_HS_VBUS TRGT VBUS0_TARGET	5V
LINK USB MICRO-B USB	USB_VBUS_LINK	5V
EXTERNAL PWR MICRO-B USB	+5V_EXT +5V	5V
+5V (JS10)	5V_SYS	5V
uPMIC (U20)	SW1_OUT	0.5V ~ 1.5V
	SW2_OUT	1.5V ~ 2.1V / 2.7V ~ 3.3V
	LDO1_OUT	1.7V ~ 1.9V
	LDO2_OUT	1.5V ~ 2.1V / 2.7V ~ 3.3V
SW2_OUT	VDD_MEM VDD_RST P1V8_CODEC	1.8V (default)
LDO2_OUT/SW2_OUT	VDDIO1	1.8V / 3.3V
VDDIO1 (JP12)	VDD_CODEC VDD_E_A VDD_FMOD	1.8V / 3.3V
LDO2_OUT	VDD_TARGET	3.3V (default)
VDD_TARGET (JS11)	V_LED VDD_ACCEL	3.3V
NCP692 (U25)	VDD_LDO_3V3	3.3V
VDD_LDO_3V3	DCDC_3V3	3.3V
NCP1117 (U14)	+2.5V_LINK	2.5V
NCP692 (U23)	USDHC_SPWR	3.3V
JP11	VDD_AMP	+5V_EXT/ EXTERNAL JACK

GENERAL DESIGN NOTES

1. Unless Otherwise Specified:
All resistors are in ohms, 5%, 1/16 Watt
All capacitors are in uF, 20%, 50V
All voltages are DC
2. Critical compenents that require tolerances tighter than listed in Note 1 are labeled with required tolerance on schematic. Non-critical components may be filled with tighter tolerance parts for BOM consolidation purposes, but may be changed to meet the general tolerances of Note 1 if desired.
3. Interrupted lines coded with the same letter or letter combinations are electrically connected.
4. Device type number is for reference only. The number varies with the manufacturer.
5. Special signal usage:
_B or 'n' Denotes - Active-Low Signal
<> or [] Denotes - Vectored Signals
6. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

Jumper Configuration

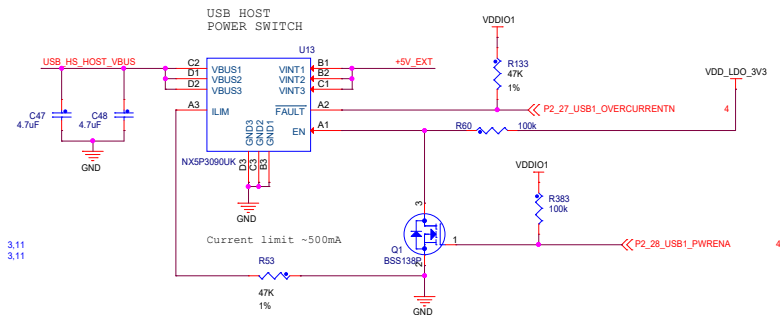
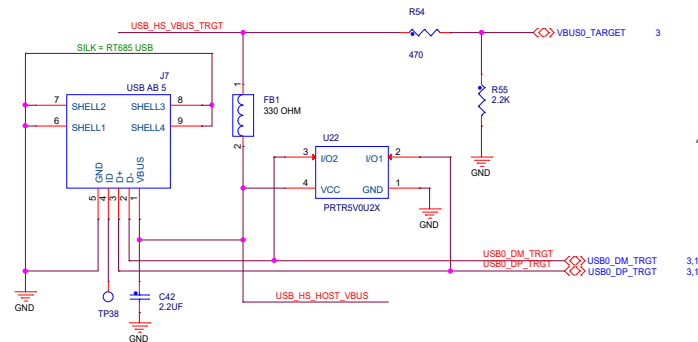
LOCATION	PIN
JP2, JP11, JP12, JP15-JP21, JP23-JP30	1-2
JP6, JP7, JP8	2-3
JP1, JP3, JP4, JP9, JP10, JP13, JP14	1-OPEN
SW5	ON, OFF, ON

Revision History

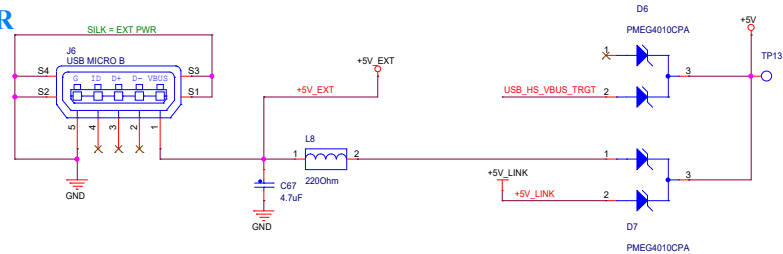
Rev. Code	Date	Description
X1	07/12/2018	Rev X1 Draft
X2	07/19/2018	Parallel I2C translator 1v8 - 3v3 Audio Amplifier connections updated, adding supply voltage for high current application
A	08/16/2018	Released files
B	09/13/2018	xxxx
C	11/23/2018	R133, 47k pull-up added 100k pull-up added to nRESET_POR IF_ICK_SWCLK & IF_SWDIO isolated from debug probe P1_12_SPI_MISO drive through a separate level translator BATTERY HOLDER BT1 changed for a 2x1 header (S2B-FH-KL) U6 replaced for FXOS8700CQ J24 replaced for a 6.3mm OD, 2.1/2.5mm ID P0_10 now connected to User switch2 P0_27 now connected to J27 pin4 (D3) Jumper added to MCU, can be selected SW2_OUT or LDO2_OUT domains Update RST control for RT6xx to reset OSPI
D	07/01/2019	JP21, R146 & R147 added
D1	09/17/2019	I2S CODEC/AMP TX/RX signals swapped TP38 added for J7 USB ID signal Breakouts added for PWR measurement. R148 added to IF_RST signal, VDD_RST supply by LDO1_OUT LDO_ENABLE pullup & pulldown options added PCA9420UK changed for QFN Octal Flash and pSRAM section updated/added SD card and M2 mini card updated J38 Trace connector added Accel reset updated Audio Codec to work at 1.8V (SW2_OUT) Audio AMP to work at 3.3V (VDDE_A) CoinCell option removed. OnBoard DMIC added, I2C availavle at J31 J47 added for Flexcomm availability
E	10/14/2019	Released
E1	12/19/2019	J45 as DNP
E2	02/04/2020	Jumper configuration added



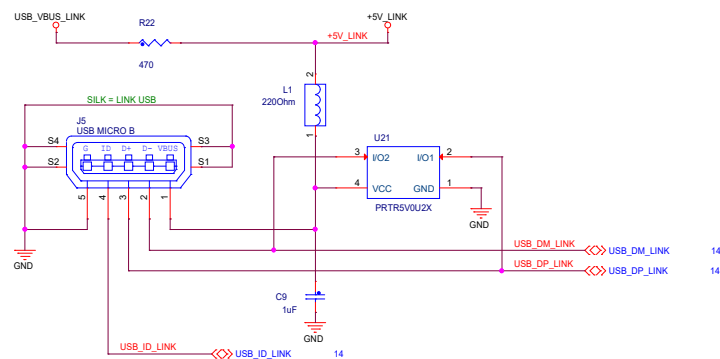
TARGET Hi-SPD
USB DEVICE / HOST
MICRO AB



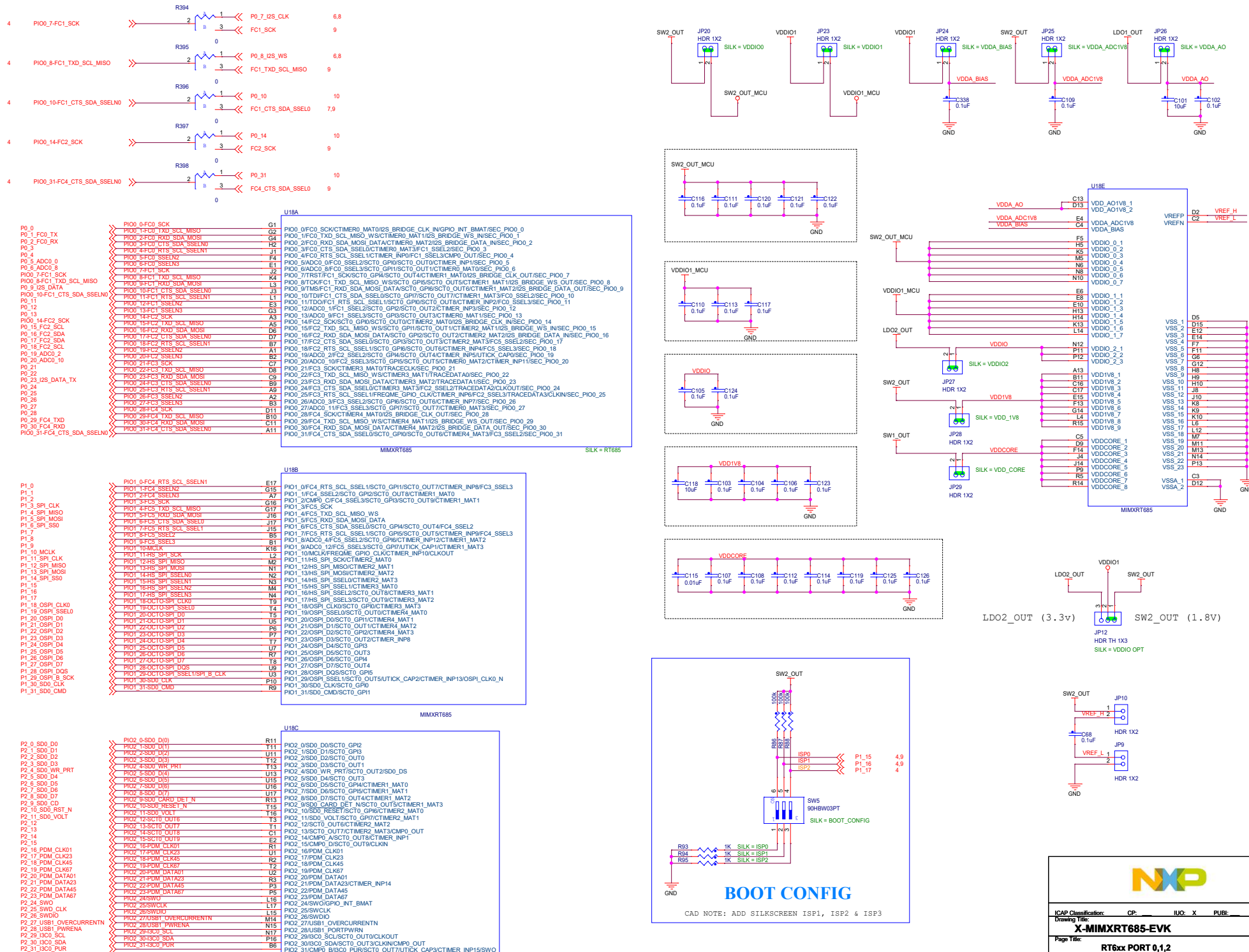
External +5V
Power only
Micro-B



Link
USB Device
Micro-B



ICAP Classification:		CP:	IJO: X	PUBI:
Drawing Title:				
X-MIMXRT685-EVK				
Page Title:				
RT6xx POWER / USB				
Size C	Document Number			Rev E2
	SCH-35099 PDF: SPF-35099			
Date:	Tuesday, February 04, 2020	Sheet	2 of	14



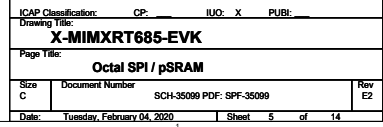
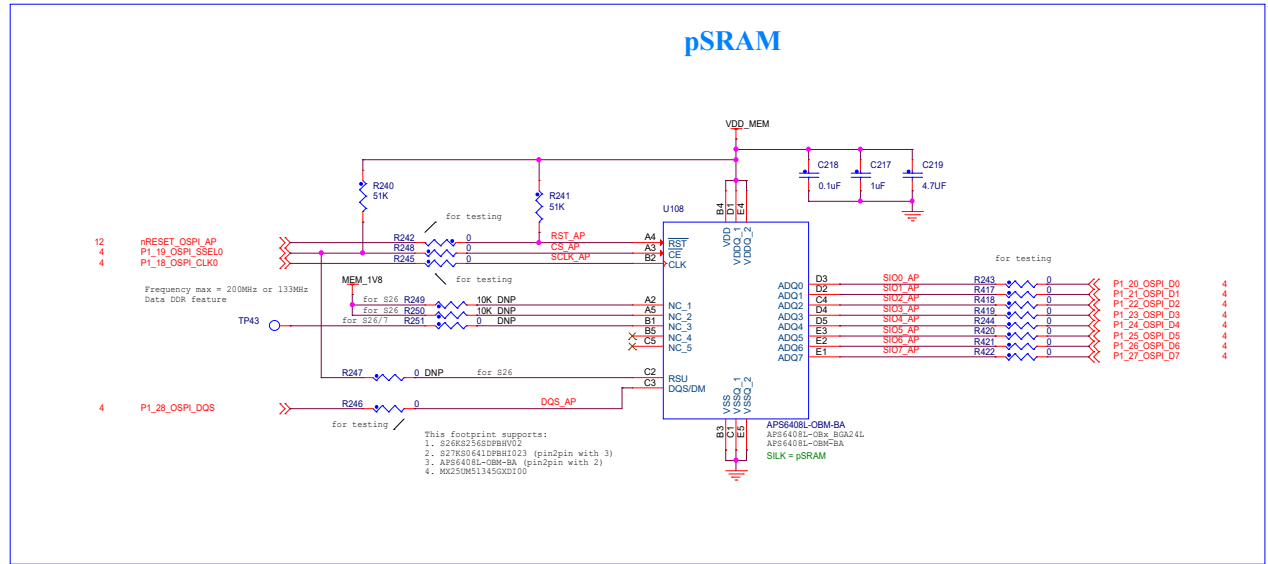
OCTAL FLASH

Frequency max = 160MHz
Data DDR feature

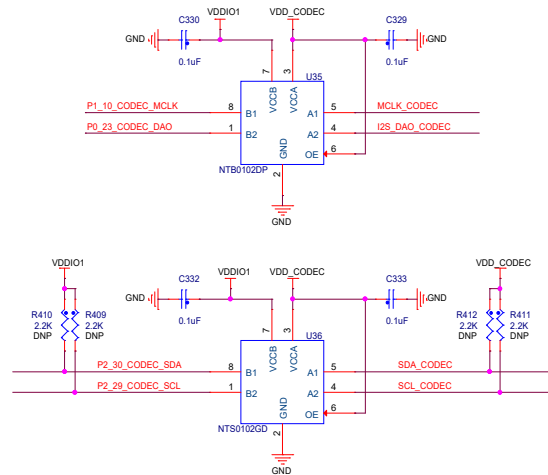
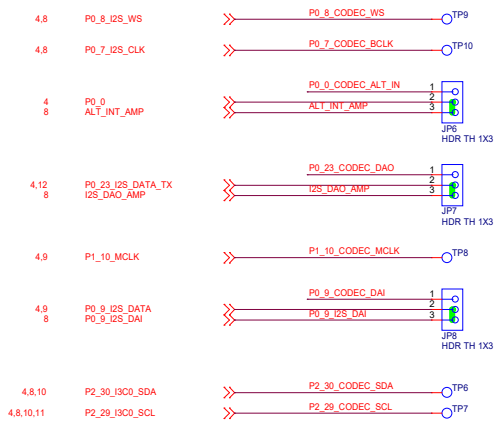
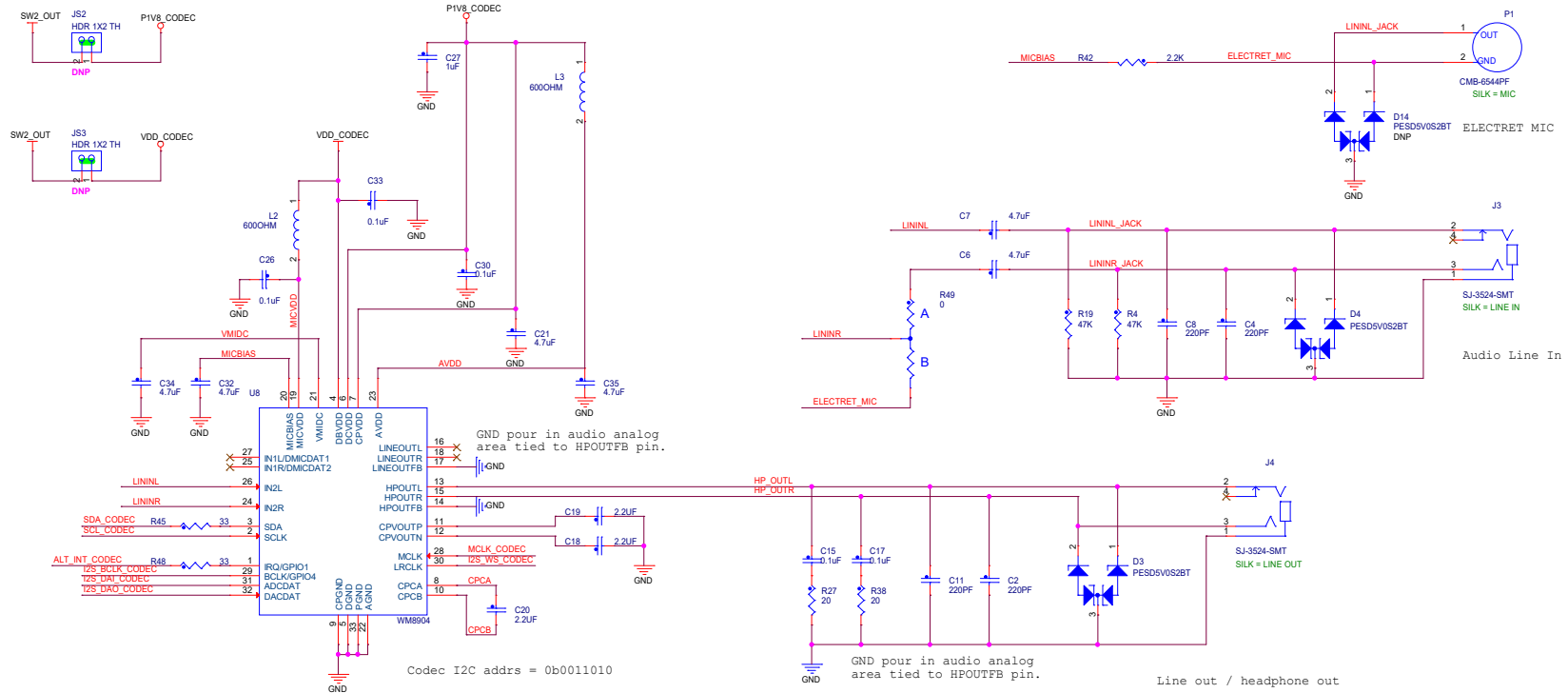
Schematic Note: MX25UM134SGXD010
Typical values at VCC=1.8V (VCC = 1.65V - 2.0V)
Output High Voltage = VCC+0.2
Input High Voltage = VCC+0.4

CSPI/PSRAM	Populated	DNP
MX25UM134SGXD010	A,B,C,D,E1,E2,F,G,H,M	J,K,L
B2K6S214SDP6W02	A,B,C,D,E1,E2,F,G,H,J,K,L	L
B27K8064IDPBH1023	A,B,C,D,E1,E2,F,G,H,J,K,L	H,R
AP9440S1-QM8A	B,C,D,E1,E2,F,G,H,J,K,L	H,K

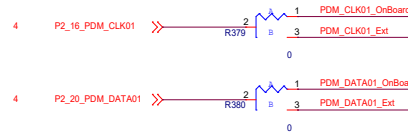
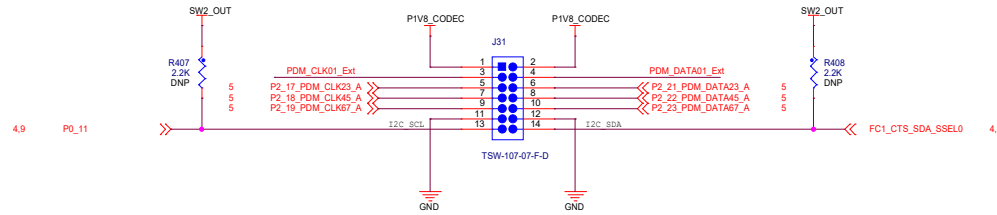
This footprint supports:
 1. B2K6S214SDP6W02
 2. B27K8064IDPBH1023 (pin2pin with 3)
 3. AP9440S1-QM8A (pin2pin with 2)
 4. MX25UM134SGXD010



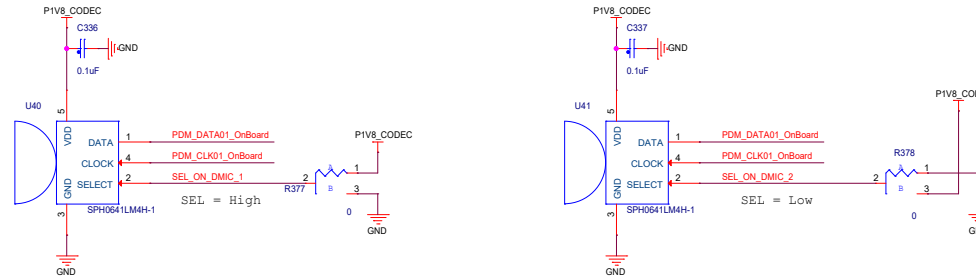
AUDIO CODEC



External DMIC



On Board DMIC

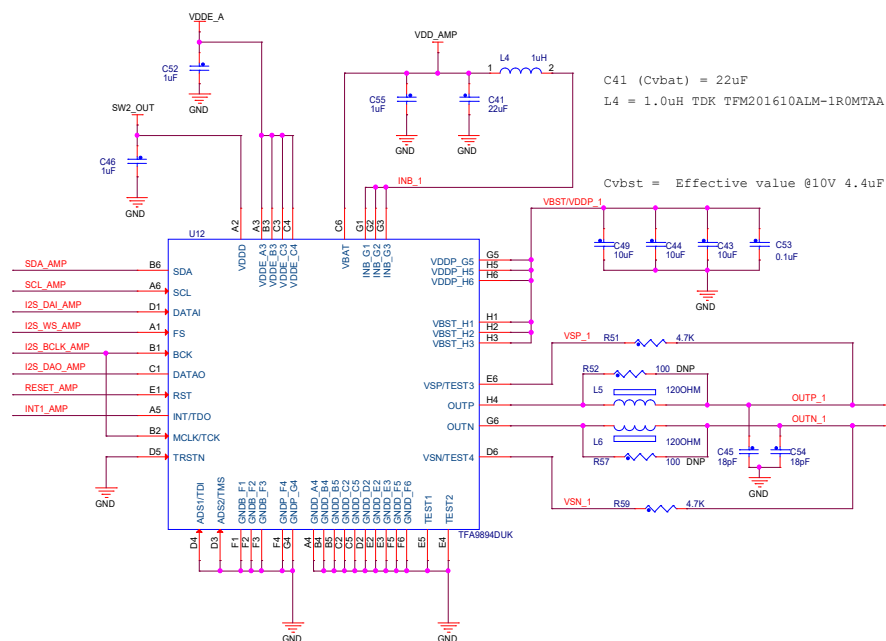
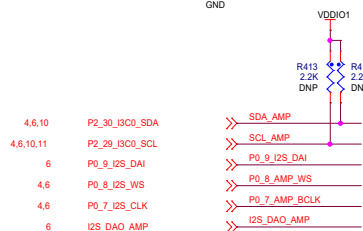
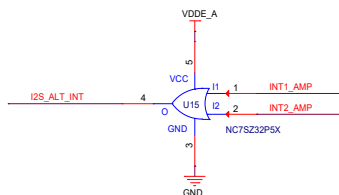


Place U40 & U41 at least 1.5" apart each other

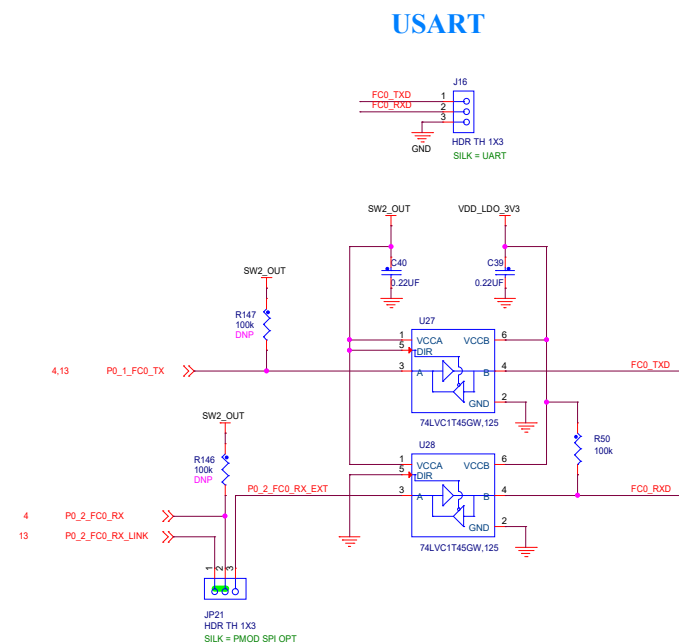
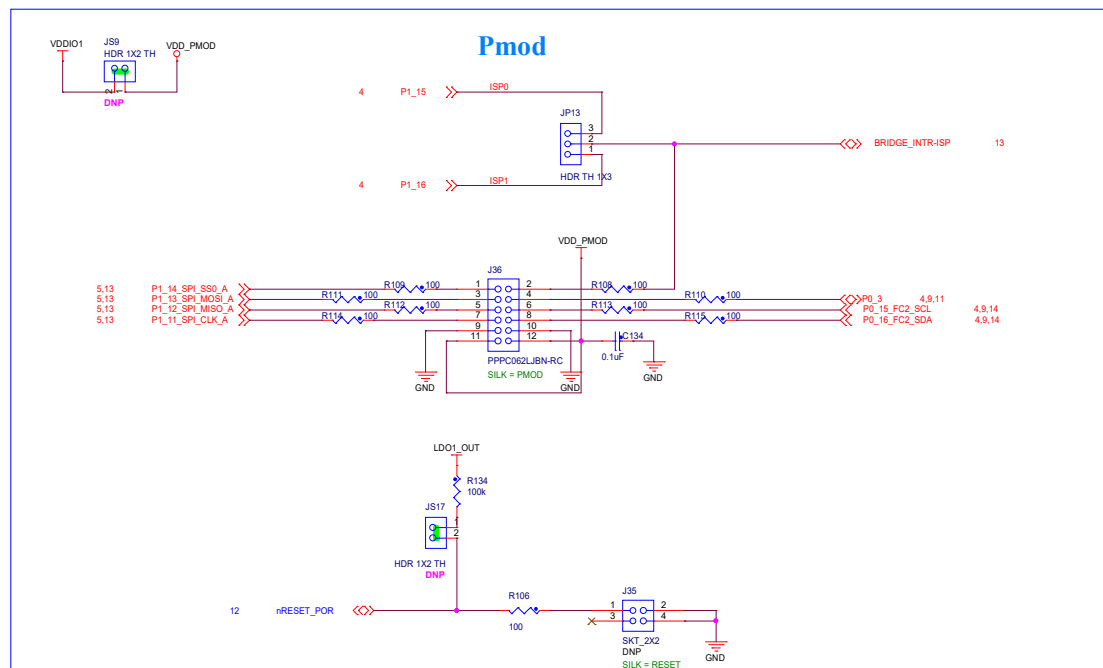
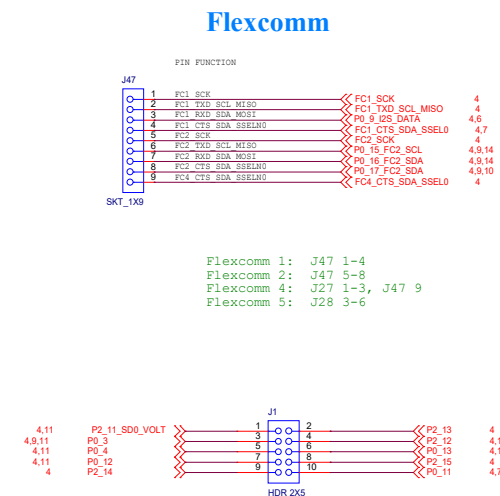
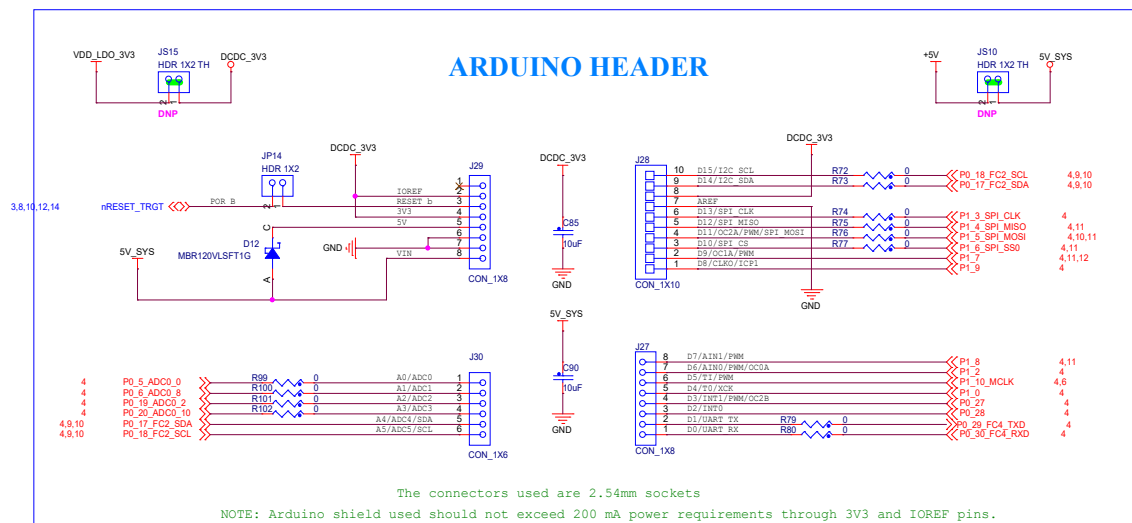


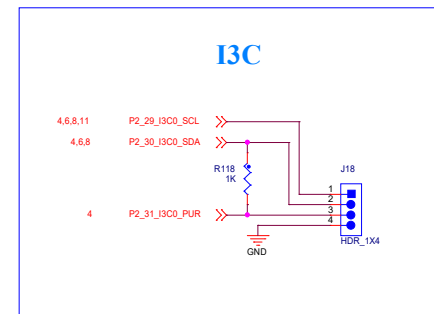
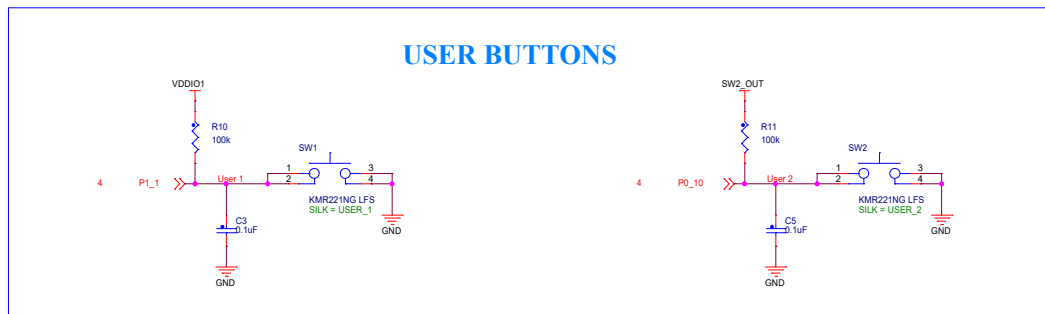
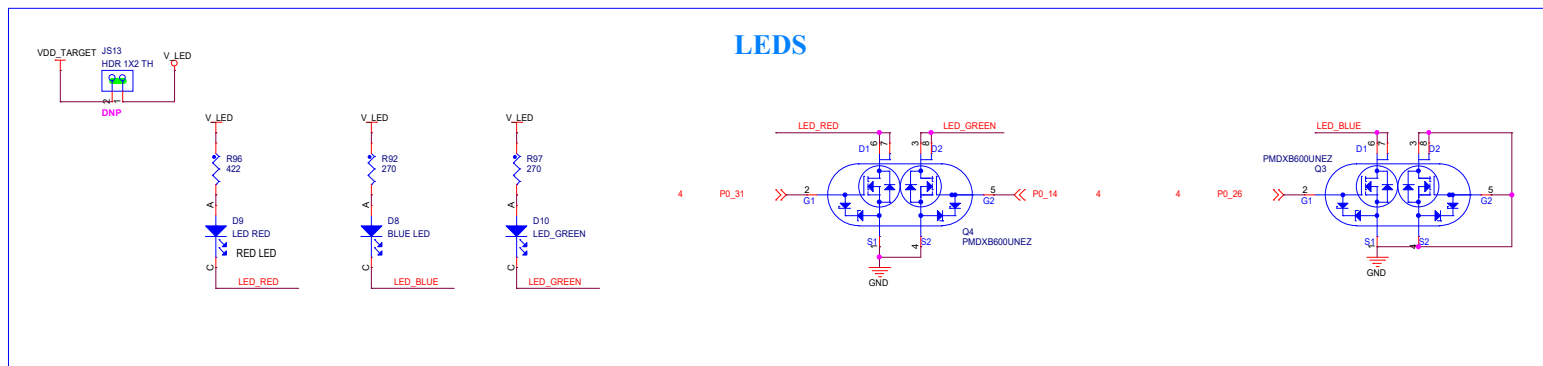
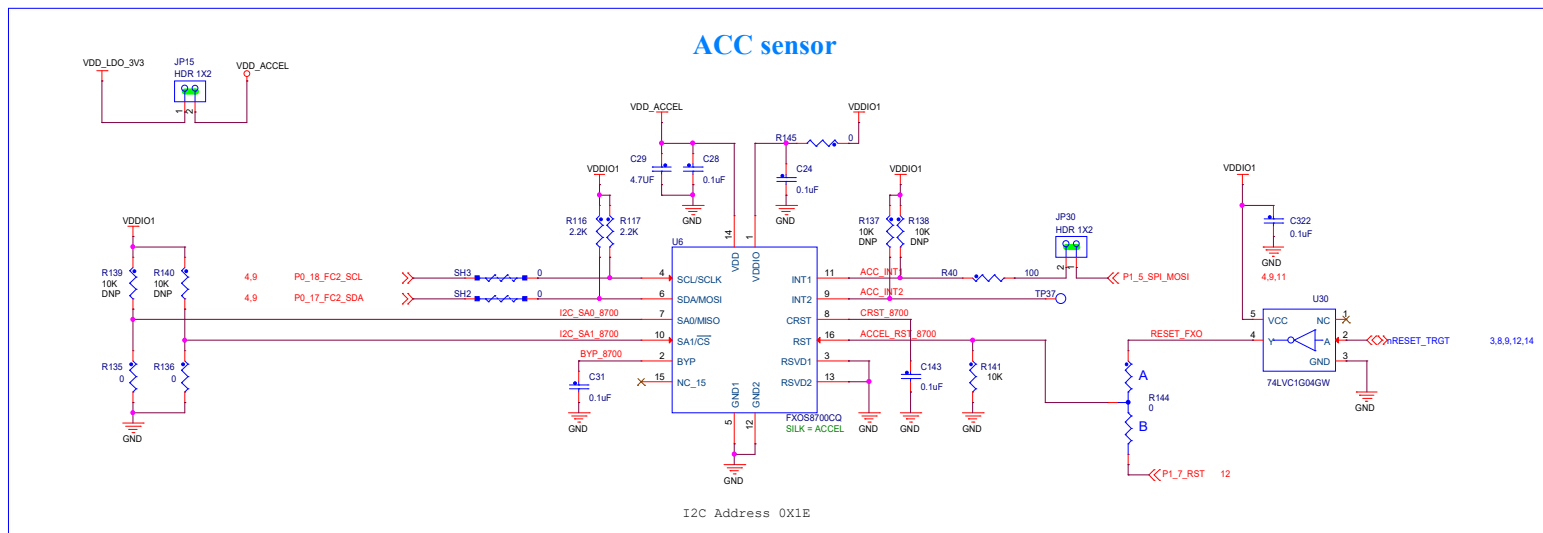
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X-MIMXRT685-EVK			
Page Title:			
AUDIO DMIC			
Size	Document Number	SCH-35099 PDF: SPF-35099	
C		Rev E2	
Date:	Tuesday, February 04, 2020	Sheet 7	of 14

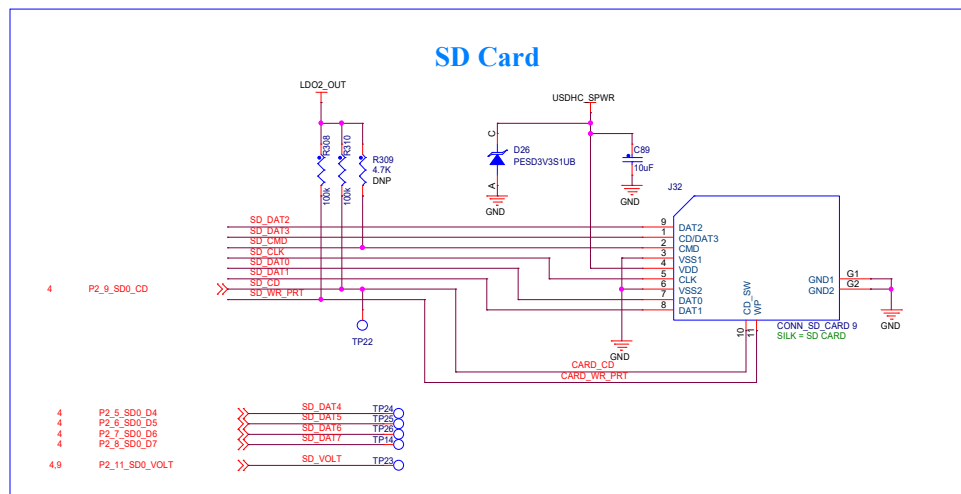
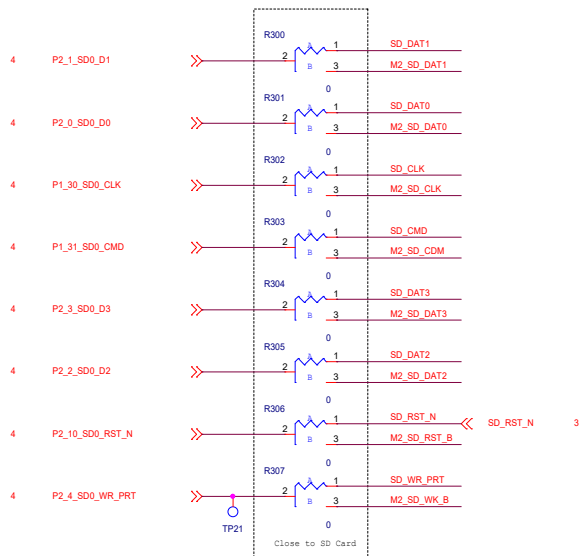
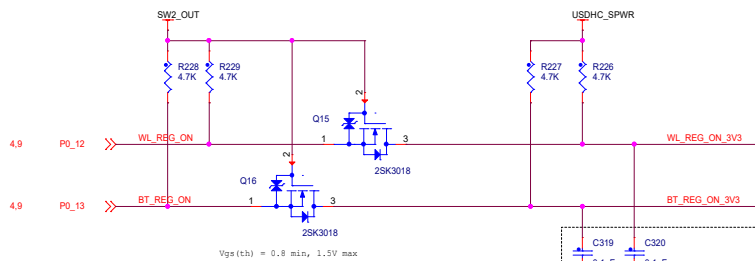
The schematic diagram illustrates the power supply section of the J24 module. A DC10LP SILK = 5V JACK is connected to a VDD_JACK input. The circuit includes a 100uF capacitor (C76) and a 0.1uF capacitor (C75) connected to ground (GND). The output of the jack is connected to a 4.7uF capacitor (C77) and a 0.1uF capacitor (C78) connected to ground (GND). The output is also connected to a JP11 HDR TH 1X3 header.



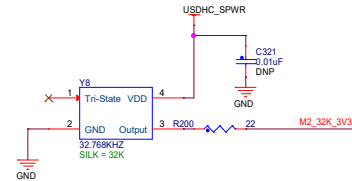
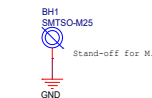
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Page Title:				
AUDIO AMP				
Size C	Document Number			Rev E2
	SCH-35099 PDF: SPF-35099			
Date:	Tuesday, February 04, 2020	Sheet	8 of 14	





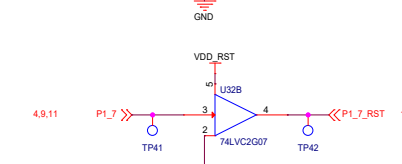
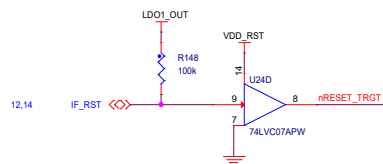
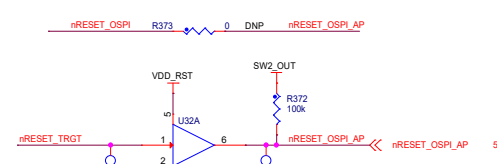
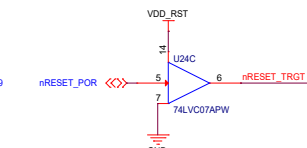
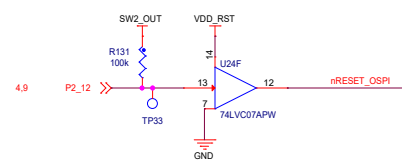
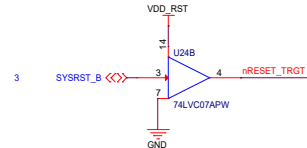
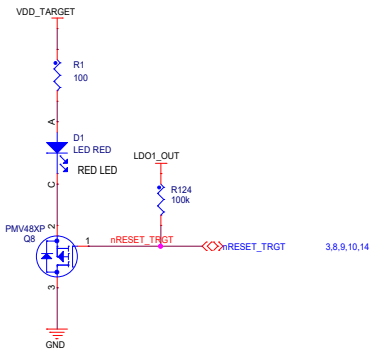
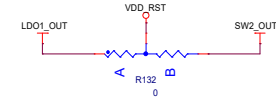
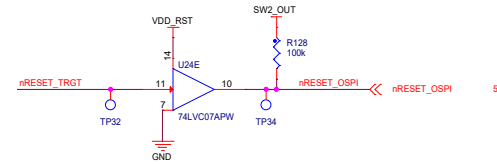
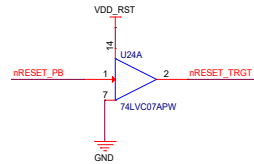
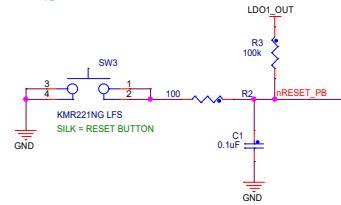


M.2 mini Card



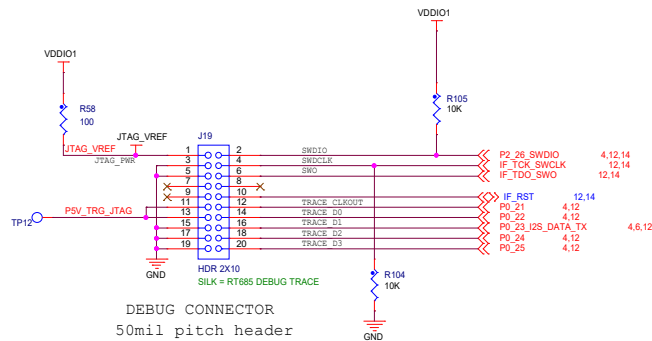
RESET

RESET PB

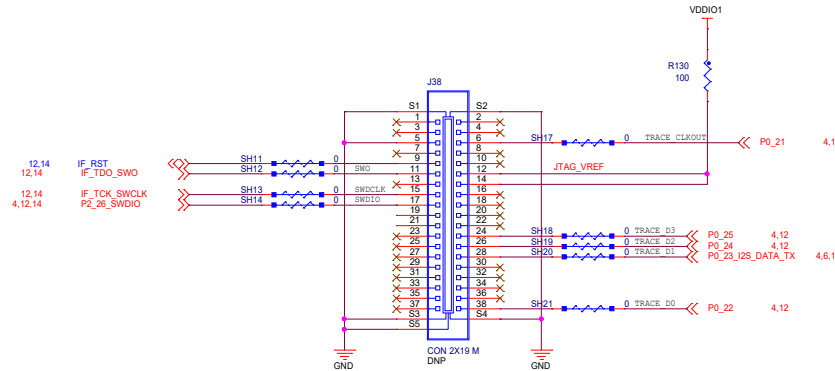


RESET LED

Debug Trace Connector



Mictor 38 - Trace Adapter

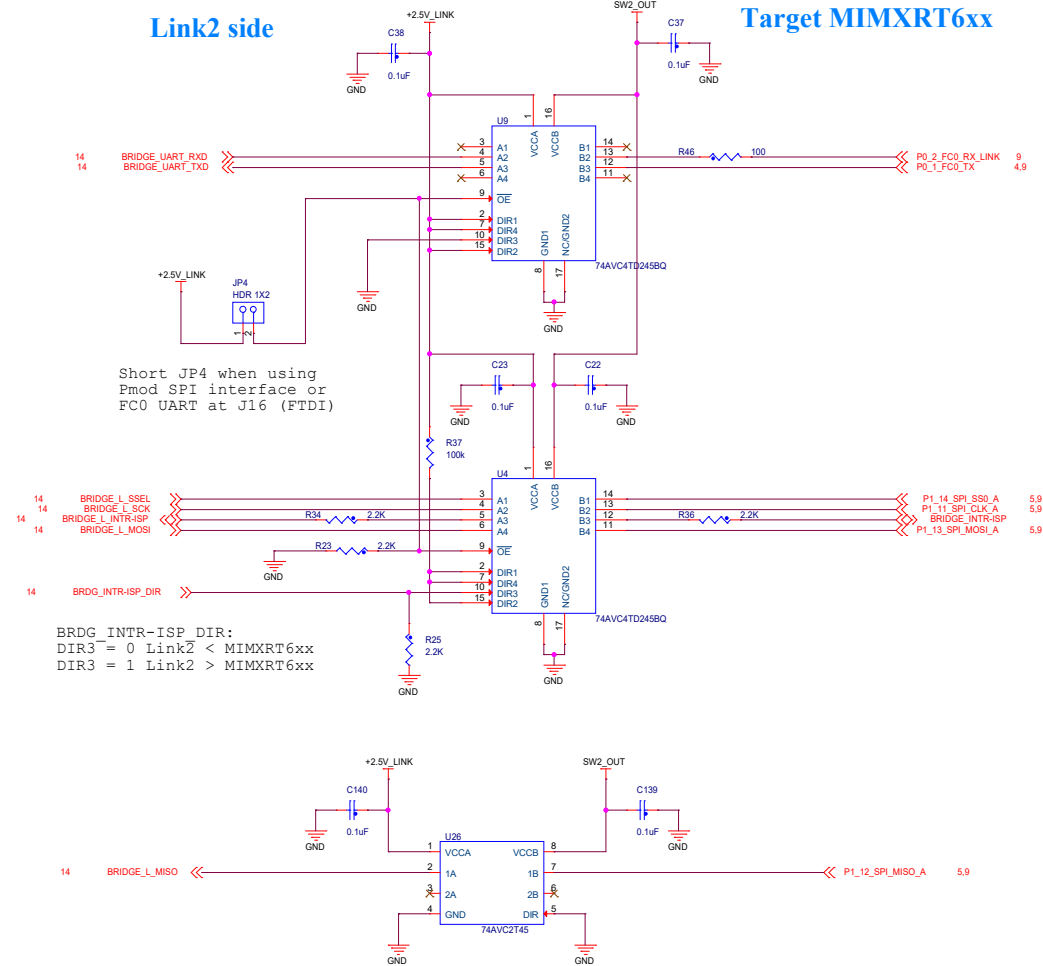


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Size	Document Number	SCH-35099 PDF: SPF-35099	Rev E2
C			
Date:	Tuesday, February 04, 2020	Sheet 12	of 14

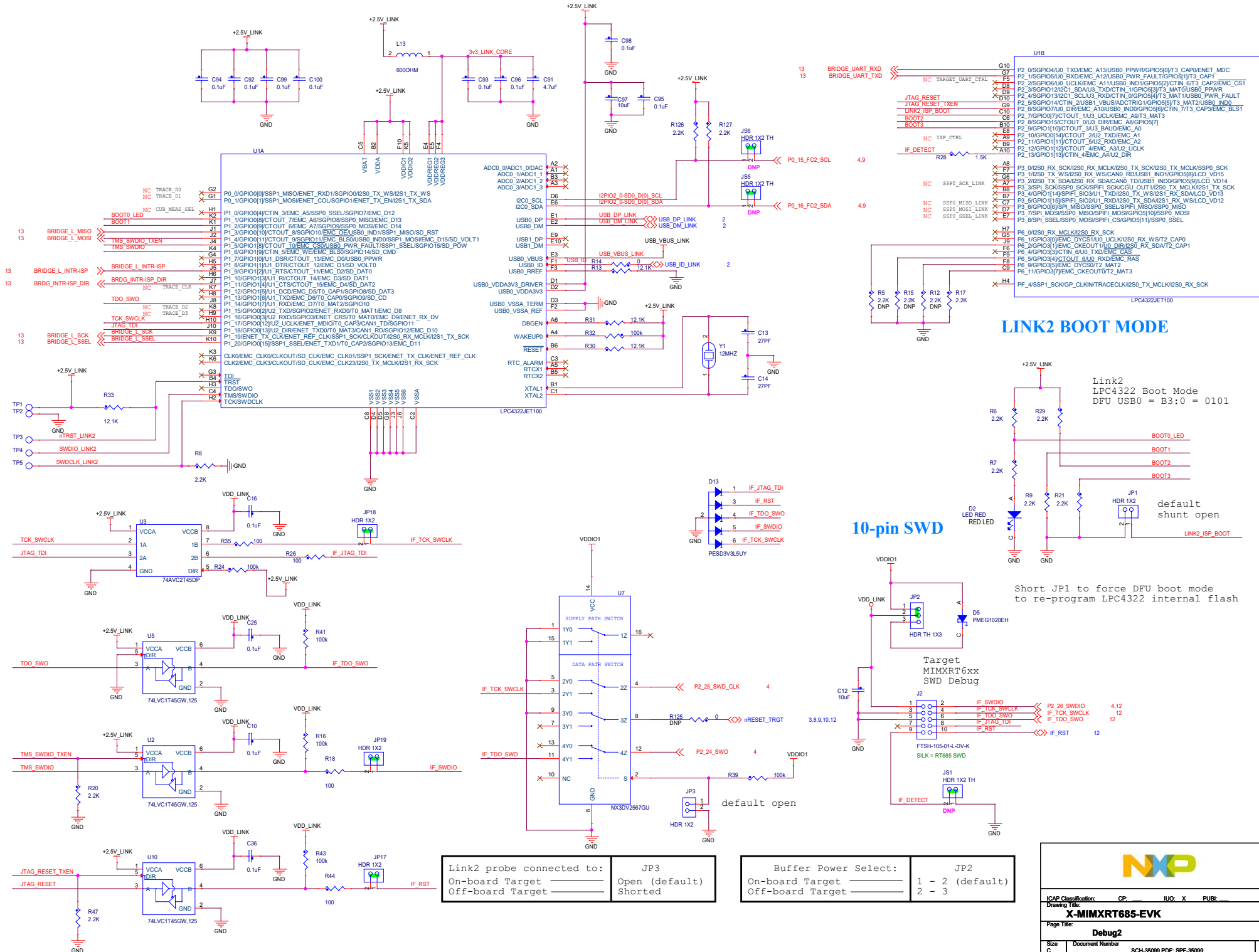
Link Level Translators

Link2 side

Target MIMXRT6xx



ICAP Classification: CP: IUQ: X PUB:			
Drawing Title:			
X-MIMXRT685-EVK			
Page Title:			
Debug UART			
Size	Document Number	SCH-35099 PDF: SPF-35099	Rev E2
Date:	Tuesday, February 04, 2020	Sheet 13	of 14



LINK2 BOOT MODE

Link2
LPC4322 Boot Mode
DFU USB0 = B3:0 = 0101

10-pin SWD

Short JP1 to force DFU boot mode to re-program LPC4322 internal flash

Link2 probe connected to:
On-board Target _____
Off-board Target _____

JP3
Open (default)
Shorted

Buffer Power Select:
On-board Target _____
Off-board Target _____

JP2
1 - 2 (default)
2 - 3



ICAP Classification:		CP:	IUC:	X	PUB:
Drawing Title:		X-MIMXRT685-EVK			
Page Title:		Debug2			
Size	Document Number	SCH-35099 PDF: SPF-35099		Rev E2	
C					
Date:	Tuesday, February 04, 2020	Sheet	14	of 14	