

1. THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE WITH SPECIFICATION IPC-A-600 CLASS 2 (LATEST REVISION).
2. THE FRB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 260 DEGREES CELSIUS FOR 10 SECONDS.
3. BASE MATERIAL - LAMINATE AND PREPREG SHALL MEET IPC-4101B-26, 83 or 98
Tg - MUST BE EQUAL TO OR EQUAL TO 150 DEGREES CELSIUS.
Td - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.
4. COPPER FOIL WEIGHT - SEE STACKUP DETAIL 'A'
5. CHARACTERISTIC IMPEDANCE - SEE DETAIL 'B'
6. MINIMUM CONDUCTIVE WIDTH/SPACING TO BE .004"/.004"
7. PLATING FINISH - BOTH SIDES ENIG (ELECTROLESS NICKEL IMMERSION GOLD):
.05800-.212 MICRON (2-8 MICRONS) OF GOLD OVER
2.540-6.350 MICRON (100-250 MICRONS) OF NICKEL.

ALL THROUGH HOLE VIAS MAY BE PLATED SHUT.

9. SOLDERMASK - GREEN COLOR (TATYO OR EQUIVALENT), BOTH SIDES.
MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM NXP.

10. SILKSCREEN - WHITE EPOXY INK, BOTH SIDES. NO SILK ON PADS.

11. ELECTRICAL TEST - 100% IPCD356. PCB FABRICATOR TO PERFORM A NET COMPARE AGAINST THE IP.

12. PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.

13. DRC'S MUST BE RUN ON THE GERBER BEFORE BUILDING BOARDS,
UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY NXP.

14. TEARDROPS MAYBE ADDED AT THE FAB HOUSE TO ALL SIGNAL LAYERS.

15. TWO SOLDER SAMPLES TO BE PROVIDED.

16. BASIC GRID INCREMENT AT 1:1 IS .0001.

17. SUPPLIER MARKINGS - ON SOLDER SIDE ONLY, WHERE SHOWN.
- MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0

18. THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP

19. THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP

20. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP.
ALL HOLE LOCATION TOLERANCES ARE TO BE +/- .002 IN REFERENCE TO THE PRIMARY DATUM.

21. THIS BOARD USES VIA-IN-PAD: SEE FAR_VIAFILED.ART
A. ALL VIA USING X.1 DRILL SIZES ARE TO BE FILLED WITH NON-CONDUCTIVE VIA FILL.
LACKWERRER-PETERS PP2795 OR EQUIVALENT AND MADE PLANAR TO THE PADS.
B. OVERPLATE THE FILLED VIA AND APPLY FINISH METAL TREATMENT.
C. DIMPLE OR PROTRUSION ON VIA-IN-PAD MUST BE NO GREATER THAN 0.001",

22. FINISHED PCB MUST BE PANELIZED FOR ASSEMBLY ACCORDING TO CONTRACT MANUFACTURERS REQUIREMENTS.
THE ADDITION OF BAILS AND .125" NON-DRILLED TIGHTENING HOLES ARE AT THE DISCRETION OF CONTRACT MANUFACTURER. PANELIZATION MUST BE APPROVED BY CONTRACT MANUFACTURER.

DETAIL B
IMPEDANCE REQUIREMENTS
IMPEDANCE TOLERANCE IS 10%

Layers	Single Ended		Differential	
	Trace Width (Mils)	Impedance (Ohms)	Trace Width (Mils)	Trace Spacing "Always" (Mils) Impedance (Ohms)
L1_P5	10.00	50		
L4_SS	10.00	50		

DRILL CHART: TOP to BOTTOM
ALL UNITS ARE IN MILS

FIGURE	FINISHED SIZE	TOLERANCE DRILL	PLATED	QTY
○	10.0	+0.0/-10.0	PLATED	53
⊖	10.1	+0.0/-10.1	PLATED	22
⊖	31.0	+2.0/-2.0	PLATED	10
⊖	40.0	+3.0/-3.0	PLATED	12
⊖	48.0	+3.0/-3.0	PLATED	16
⊖	52.0	+3.0/-3.0	PLATED	10
▲	63.0	+3.0/-3.0	PLATED	32
▲	73.0	+3.0/-3.0	PLATED	10
○	126.0	+3.0/-3.0	PLATED	4
◆	35.0	+2.0/-2.0	NON-PLATED	4
○	63.0x52.0	+3.0/-3.0	PLATED	2
○	63.0x52.0	+3.0/-3.0	PLATED	1

DESIGN CROSS SECTION CHART

DETAIL A
LAYER STACKUP
SCALE: NONE

PART NO. 170-48220

NXP SEMICONDUCTORS

6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA

PRINTED WIRING BOARD
KITFS6507LAEVVM

21	SIZE	CAD FILE NAME	CMC. NO.	REV
21	□	LAY-48220	FAB-48220	A

SCALE	1/1	DO NOT SCALE DRAWING	SHEET	1	OF	1
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ALL PARTS, MATERIALS AND FINISHED ASSEMBLY SHALL MEET THE BASES COMMISSION DELEGATED DIRECTIVE (EU 2015/863 OF 31 MARCH 2015 AMENDING ANNEX II TO DIRECTIVE 2011/65/EU). CERTIFICATE OF COMPLIANCE IS REQUESTED UPON REQUEST.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:

DECIMALS		ANGLES
JX	.01	30°-30'
JXX	.005	

✓ RNS ALL MACHINED SURFACES
BREAK ALL SHARP EDGES AND CORNERS
REMOVE BURRS
UNDERLINED DIM. NOT TO SCALE
THIRD ANGLE ORTHOGRAPHIC PROJECT
IS USED.

	APPROVALS	DATE
	DRAWN MARTIN V.	03-01-2016
	CHECKED JONATHAN HERNZ.	03-01-2016
DESIGN ENGINEER	FERNANDA ISLAS	02-16-2016

-21	TITLE
-21	SIZE
-21	D