


Table of Contents

1	TITLE PAGE
2	INTERFACE CONNECTOR

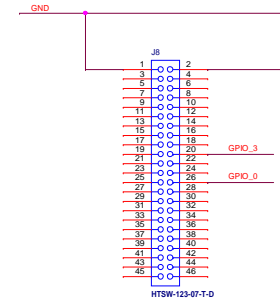
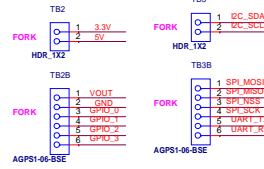
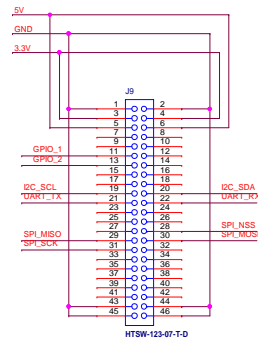
Revisions History

Rev	Description	Date	Approved
X1	INITIAL DRAFT	10-22-2020	J. Geslin
	A055, Initial Level PPL release into Agile PDM	11-02-2020	J. Geslin
	A070, Released of initial level schematic with netlist in Agile PDM.	11-04-2020	J. Geslin
A	swapped SPI_MISO signal to J9 connector pin #29 and SPI_SCK signal to J9 connector pin #34.	11-05-2020	J. Geslin
	A085, Final Level Schematic and netlist release into Agile PDM	11-09-2020	J. Geslin
A1	Updated the connector with alternate Footprint. No logic symbol and schematic update.	01-02-2021	J. Geslin
	A085, Final Level Schematic and netlist release into Agile PDM	02-02-2021	J. Geslin

OM29110BBB-B

		Connectivity & Security (C&S) Group 6410 Oak Canyon, Suite 200 Irvine, CA, 92618	
<small>This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.</small>			
© NXP SEMICONDUCTORS		Classification: <u>Company Internal/Proprietary</u>	
Designer: Ravi Kanth	Drawing Title: OM29110BBB-B		
Drawn by: Ravi Kanth	Page Title: Title Page		
Approved: J. Geslin	Size C	Document Number SCH-47955 PDF: SPF-47955	Rev A1
Date: <u>Tuesday, February 02, 2021</u>		Sheet <u>1</u> of <u>2</u>	

Interface board



Classification: Company Internal/Proprietary			
Drawing Title: OM29110BBB-B			
Page Title: INTERFACE CONNECTORS			
Size C	Document Number SCH-47955 PDF: SPF-47955	Rev A1	
Date: Wednesday, February 03, 2021	Sheet 2 of 2		