AN13540

LPC553x/LPC55S3x 高速比较器 - 基本性能评估

第 1 版 — 2022 年 5 月 20 日 应用笔记

1 简介

本应用笔记介绍了系统设计人员在使用 LPC553x/LPC55S3x 系列微处理器实现 HSCMP 设计时应考虑的各种设计重点。本应用笔记还讲解了 HSCMP 子系统的关键部分及其与相关 MCU 外围模块的互连，特别是那些与快速系统保护（过流或过压保护）有关的部分。

目录

本应用笔记介绍了 LPC553x/LPC55S3x 芯片的基本的比较器功能。它展现了对于实时控制应用，构建和评估 HSCMP 模块的各种可能性。

对于想要了解 HSCMP 模块的内部外围设备的互连可能性和各种使用实例的工程师来说，本文档是非常有用的。在恩智浦 MCUXpresso IDE 中有附带例子的软件包。FreeMASTER 实时调试器用于应用程序的监测和控制。本应用笔记中的示例是在 LPCxpresso55S36 EVK 上实现的。

1.1 HSCMP 简介

高速比较器（HSCMP）模块提供了一个用于比较两个模拟输入电压的电路。它包括一个比较器（CMP）、比较器输入选择器、8 位 DAC 和用于每个比较器输入的模拟多路复用器。

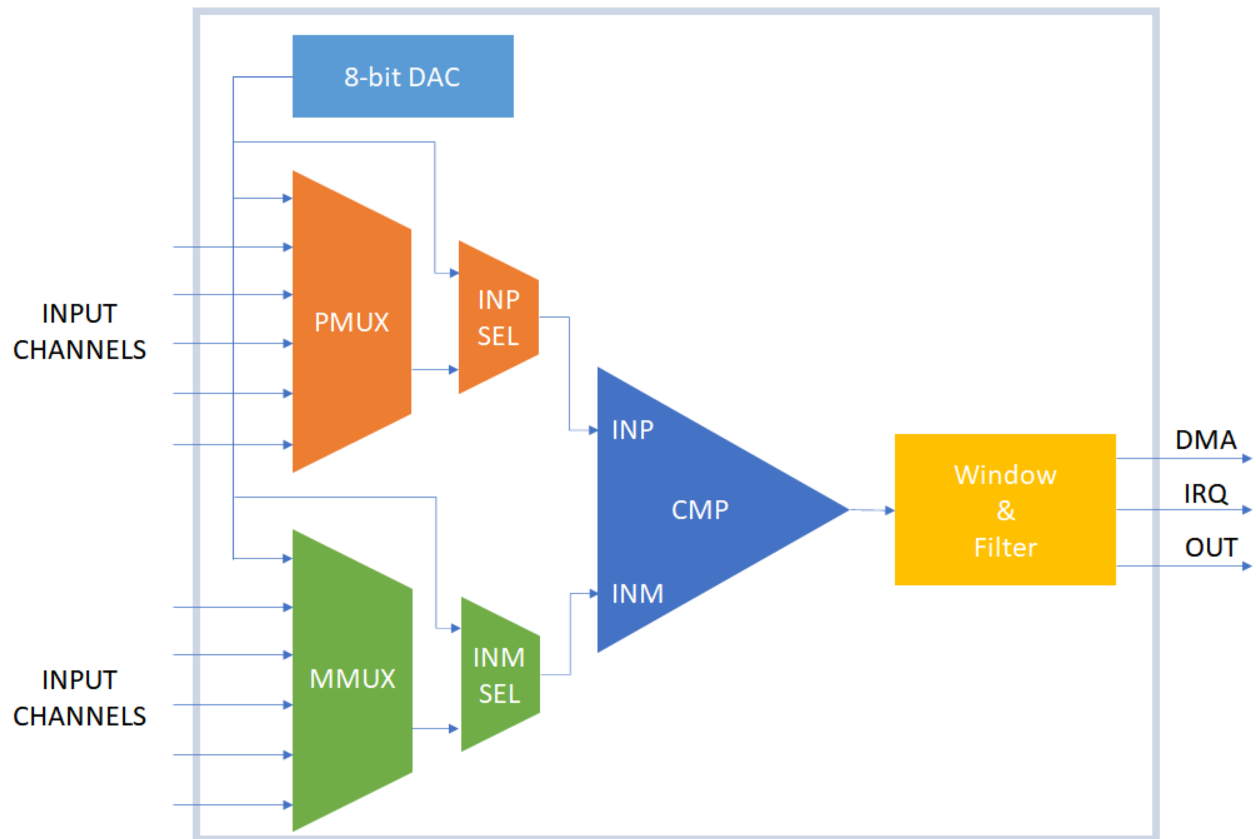

图 1. HSCMP 框图

比较器（CMP）可以在电源电压的整个范围工作，即所谓的轨到轨工作。DAC 是一个 256 抽头的电阻梯形网络，为需要电压参考的应用提供可选择的电压参考。256 抽头电阻梯形网络将电源参考（Vin）划分为 256 个电压等级。一个 8 位数字信号输入选择输出电压电平，从 Vin 到 Vin/256 不等。Vin 可以从两个电压源中选择，即 vrefh0 和 vrefh1。HSCMP 的内部 DAC 的输出只能作为片上的内部信号使用。它不能引到芯片的外部引脚上。一个内部 8 位 DAC 连接到所有两个输入多路复用器（mux），以及比较器的输入选择器上，允许在输入多路复用器或 DAC 之间直接进行选择。也可以连接一个 12 位 DAC，它只在特定的输入通道上可用（参见下面的章节）。

1.2 HSCMP 的特性

HSCMP 模块的特性包括：

- 两个 MUX，可以从 8 个通道中选择输入信号
- 多种操作模式，可产生多种不同的输出，如：
  - 采样的
  - 窗口化的，这是某些 PWM 过零检测应用的理想选择
  - 数字滤波的
- 对于窗口和采样的高级功能：
  - 窗口/采样信号可以被反转
  - 窗口可以通过 COUT 上升沿、下降沿或所有两个边沿关闭
  - 关闭窗口时，用户可以定义 COUT 电平
- 可选择的性能级别：超低功率模式、低功率（速度）模式、高功率（速度）模式

- 可编程的回差控制
- 可选择比较器输出的反转
- 在输出滤波器用于内部功能时，可同时使用外部回差
- 支持中断和 DMA
- 触发模式
- 包含一个 8 位分辨率的 DAC
- 用于 DAC 的可选择电源参考源
- 可配置 DAC 的低或高功率模式

HSCMP 的目标是应用的实时控制和快速响应的场合，如过流检测。它可以通过传导硬件比较事件来关断 PWM，因此 HSCMP 可作为硬件的过流保护。它也可以用于各种应用中的信号电平交叉检测，如功率转换器。HSCMP 比较事件也可以重启 PWM。

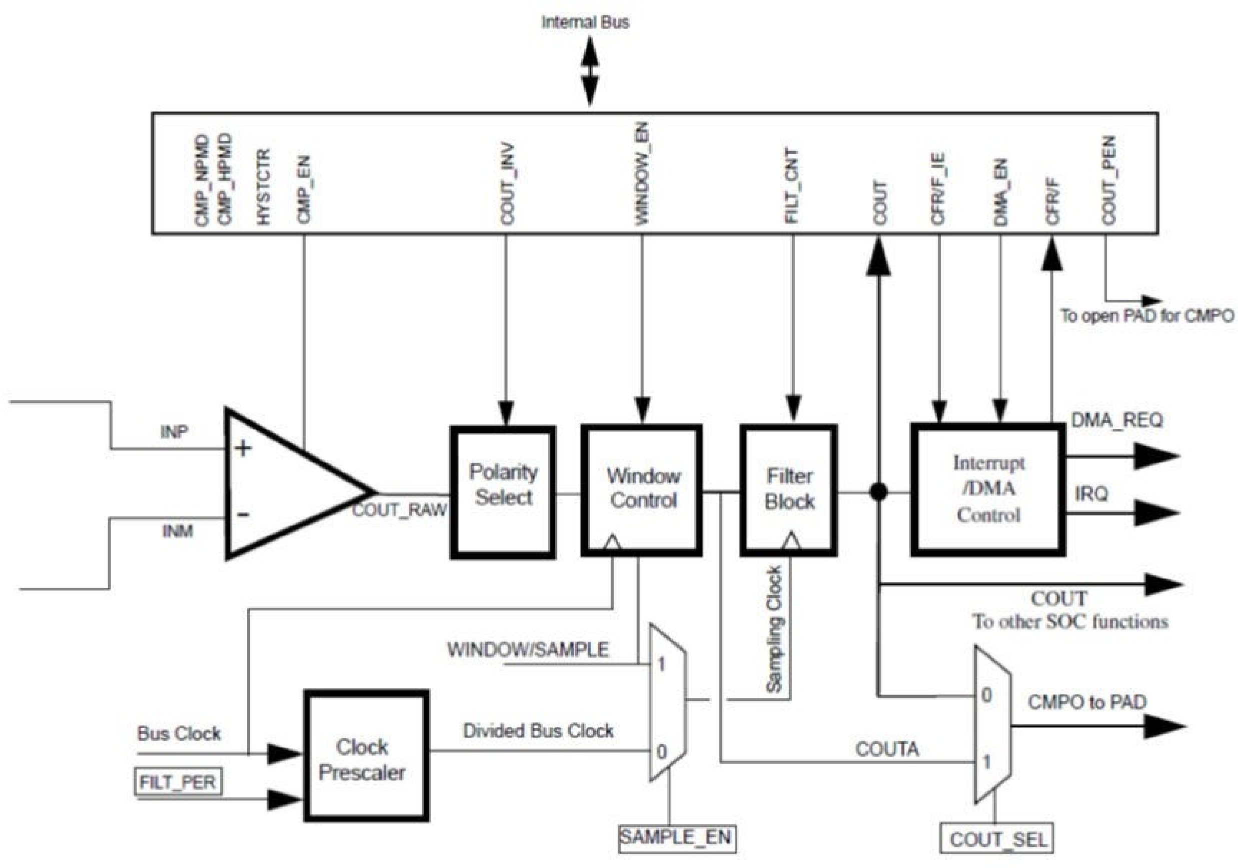

图 2. HSCMP 框图

2 引脚配置

必须设置 HSCMP 多路复用器输入引脚的模拟模式。有关更多细节，请参阅参考手册中的“I/O 引脚配置（IOCON）”章节（引脚多路复用和 IOCON 寄存器描述）和后面的底层软件示例。表 1 总结了 LPC553x/LPC55S3x 芯片上的所有 HSCMP 引脚，以及它们在 HSCMP 输入多路复用器上的可用性。不管是在正极还是负极多路复用器，或是在寄存器 HSCMP_CCR2_MSEL 和 HSCMP_CCR2_PSEL 中，输入和索引都是相同的。

表 1. HSCMP 输入

输入MUX索引	HSCMP0	HSCMP1	HSCMP2
0	HSCMP0_IN0 PIO0_24	HSCMP1_IN0 PIO0_7	HSCMP2_IN0 PIO0_17
1	HSCMP0_IN1 PIO1_12	HSCMP1_IN1 DAC0_OUT PIO1_22	HSCMP2_IN1 PIO1_23
2	不连接	不连接	不连接
3	HSCMP0_IN3 PIO1_5	HSCMP1_IN3 PIO1_10	不连接
4	HSCMP0_IN4 OPAMP0_OUT PIO1_9	OPAMP1_OUT	OPAMP2_OUT
5	DAC0_OUT PIO1_22	HSCMP1_IN5 DAC1_OUT PIO1_19	DAC2_OUT
6	保留	保留	保留
7	HSCMP0 DAC	HSCMP1 DAC	HSCMP2 DAC

2.1 比较器的评估

本应用笔记和评估软件描述的是基本的功能。该示例演示了两个信号的比较：12 位 DAC 产生的锯齿信号和 HSCMP 内部 8 位 DAC 产生的恒定电压参考信号。HSCMP 比较的结果可以在输出引脚上观察到。你可以反转输出逻辑，设置不同的阈值（内部 8 位 DAC、外部 12 位 DAC，或根据表 1 的 MCU 输入引脚信号）。必须安装 MCUXpresso、LPC553x/LPC55S3x SDK 包和 FreeMASTER 工具。

要运行 SDK HSCMP 示例，请执行以下步骤：

1. 将示例解压缩到您的硬盘驱动器位置。
2. 将示例导入 MCUXpresso IDE。
3. 构建示例。
4. 将示例写入 Flash。
5. 启动 FreeMASTER HSCMP 项目。
6. 点击“Run”（运行）按钮。
7. 使用 FreeMASTER 实时调试器在运行时设置变量（特别是阈值）。可以用示波器监测结果。

示波器可以连接到 LPCXpresso55S36 上的 J10-11，以监测 12 位 DAC 输出；第二个探头可以连接到 J10-9，以观察比较器的输出（见图 3）。连接到 J9-9 的外部信号（HSCMP0_IN3）可以不是 12 位 DAC 的输出。在评估该软件示例时，预期的默认波形应该与图 3 中的信号类似。

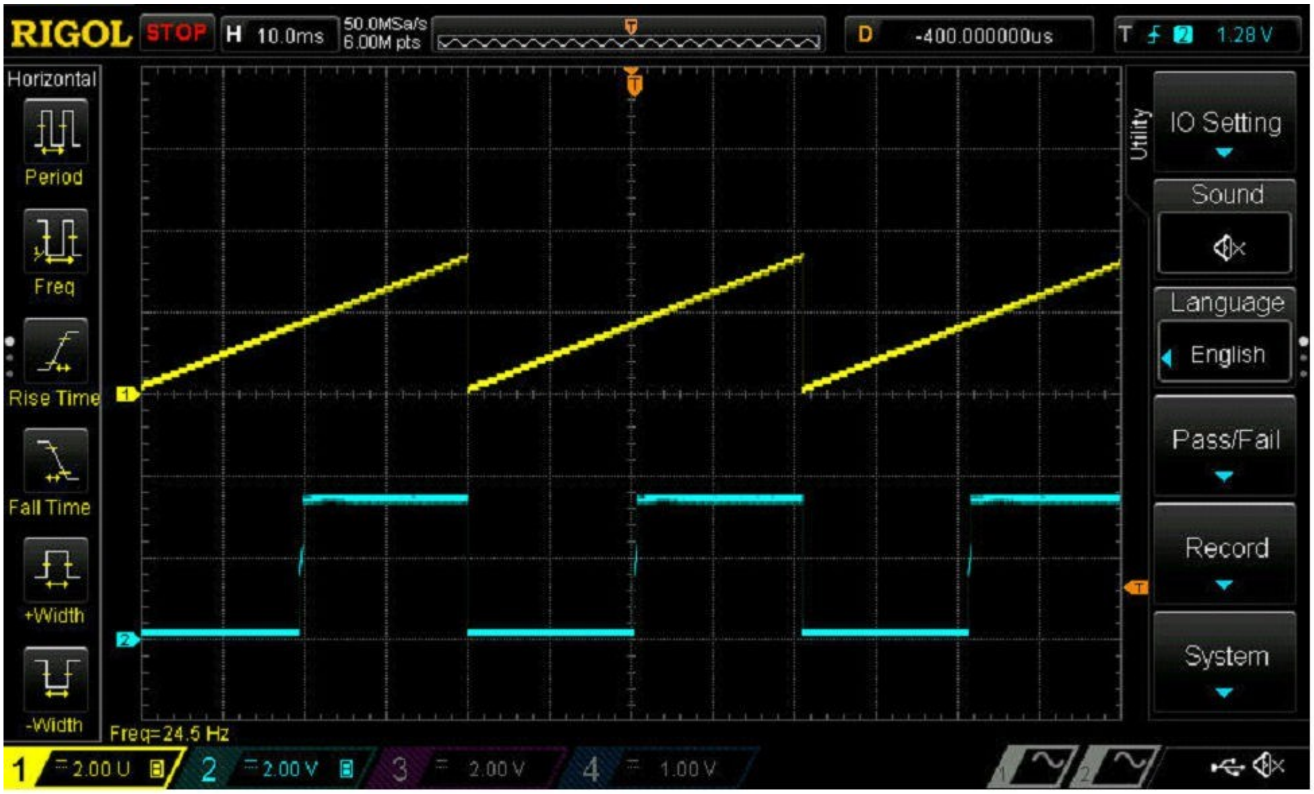

图 3. 预期的波形

3 使用 HSCMPs 进行过流保护

下面的原理图显示了用于电机控制应用的典型 3 电阻配置。$R_{sh\_<x>}$ 是一个低侧电流感应配置的采样电阻。这个电阻上的电压降被内部可变增益 OPAMP 放大。R_1 和 R_2 是内部电阻网络的一部分，它们的值与正参考电压（PREF）源一起，可通过 OPAMP_CTR 寄存器配置。

OPAMP 的输出信号（OPAMP<x>_OUT）在内部被连接到 ADC、HSCMP 和输出引脚。根据特定的 OPAMP<x>_OUT – HSCMP<y> 输入组合，可能需要通过在 IOCON 模块 PIO 寄存器中设置各自的 ASW0 或 ASW1 位来关闭一个模拟开关。参见参考手册中的相应表格。

HSCMP 正和负输入信号可通过 HSCMP CCR2 寄存器进行配置。

HSCMP 输出信号通过 INPUTMUX 模块被连通到相关的 eFlexPWM 子模块的故障输入（参见 INPUTPUX 的 PWM0_FAULT0 – PWM0_FAULT3 寄存器）。

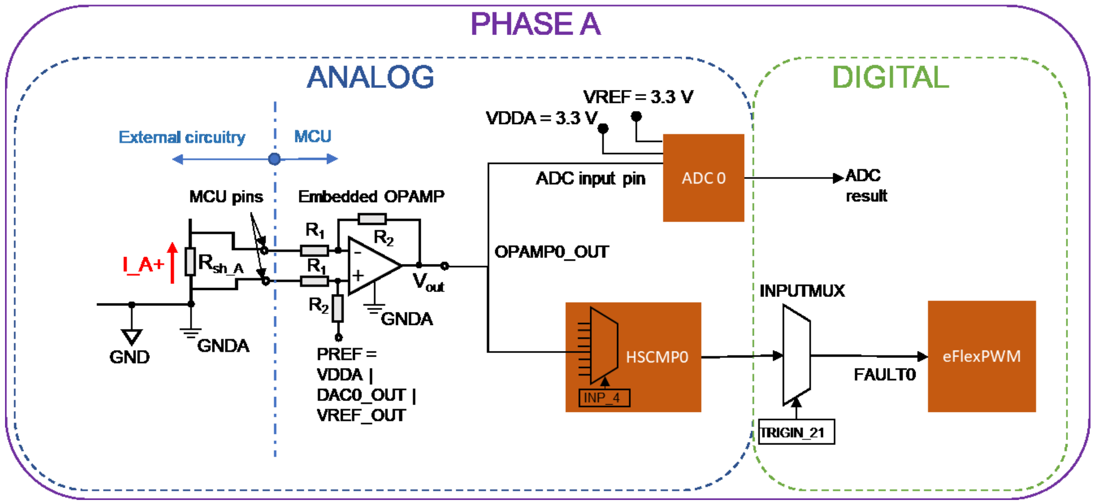

图 4. 过流保护框图（A 相）

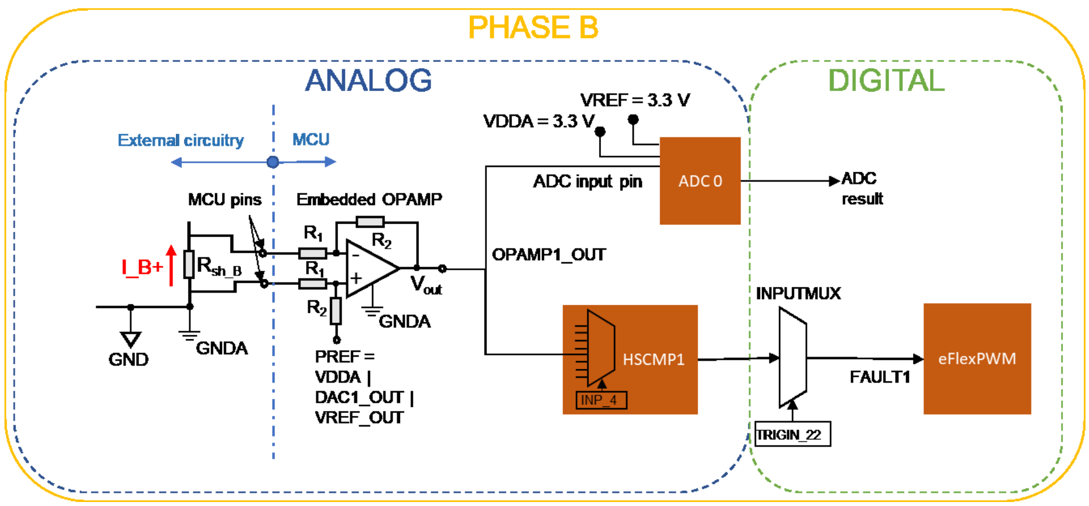

图 5. 过电流保护框图（B 相）

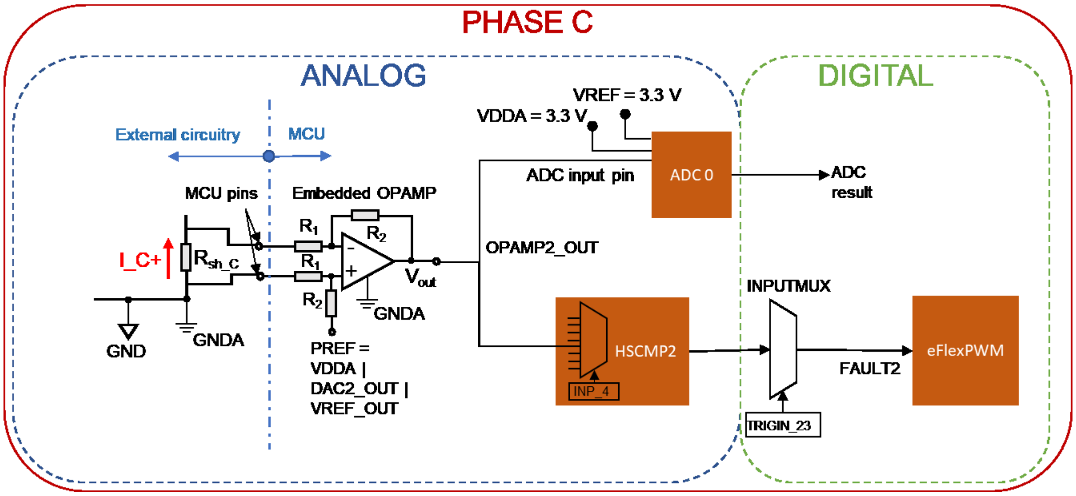

图 6. 过流保护框图（C 相）

3.1 过流保护设计指南

最大电流对应的 $OPAMPn\_OUT_{max}$ 电压可由下式确定：

$$OPAMPnOUT_{max} = (I_{max} * R_{sh} * GAIN) + PREF \qquad [V]$$

请注意，在所描述的场景中，电流方向约定是这样的，从 DC-Bus 流到 GND 的过电流在采样电阻上产生负的电压降，因此 $OPAMPnOUT_{max} < PREF$。

这个计算值表示比较器参考电压，它可以是由 HSCMP 的内部 8 位 DAC 产生的。或者，也可以将外部 12 位 DAC 设置为参考源。比较器参考电压应该被连通到比较器的 INM 输入。OPAMPn_OUT 信号应该连接到 INP 输入引脚。HSCMP 配置示例（使用内部 DAC）如下：

```
/* Port 2, pin 14 (OPAMP1_OUT) to HSCMP1_IN4 - close the analog switch */
IOCON_PinMuxSet(IOCON, 2, 14, IOCON_FUNC0 | IOCON_ANALOG_EN | (1U << 10 ));
/* Power up the CMP bias circuitry */
POWER_DisablePD(kPDRUNCFG_PD_CMPBIAS);
/* Power up the HSCMP and its internal DAC */
 POWER_DisablePD(kPDRUNCFG_PD_HSCMP1);
 POWER_DisablePD(kPDRUNCFG_PD_HSCMP1_DAC);
HSCMP1->CCR1 = (1U << 5) | /* Enable comparator output*/
(1U << 4);
/* Use COUTA (unfiltered comparator output) */
HSCMP1->CCR2 = (0U << 28) | /* INM - 8-bit DAC */
(1U << 24) | /* INP - Analog 8-1 mux */
(7U << 20) | /* MSEL - 8-bit DAC */
(4U << 16) | /* PSEL - OPAMP1_OUT */
(1U << 0);
/* High power mode */
/* Set DAC_OUT to 1.225V (2.5A current through 0.020 Ohm shunt) */
HSCMP1->DCR = (94U << 16) | /* (3.3V / 256) * (94 + 1) = 1.224 V */
(1U << 15) | /* DAC output enable */
(1U << 1) | /* High power mode enabled */
(1U << 0);
/* DAC enable */
/* HSCMP enable */
HSCMP1->CCR0 = 1U;
```

HSCMP 的输出应该被连通（通过 INPUTMUX 模块）到某些 PWM 子模块各自的 FAULT（故障）输入，这些 PWM 子模块负责生成相应相位的 PWM 信号。INPUTMUX 配置举例如下：

```
/* Separate fault per each OPAMP */
INPUTMUX->PWM0_FAULT[0] = 21U;
/* PWM0 fault 0 = HSCMP0 */
INPUTMUX->PWM0_FAULT[1] = 22U;
/* PWM0 fault 1 = HSCMP1 */
INPUTMUX->PWM0_FAULT[2] = 23U;
/* PWM0 fault 2 = HSCMP2 */
```

FAULT（故障）信号是边缘敏感的，其极性是可配置的。PWM 必须配置为检测故障信号并做出适当的反应。FlexPWM 故障处理配置示例如下：

```
/* Separate fault per each OPAMP */
PWM0->SM[0].DISMAP[0] = 0xF777U;
PWM0->SM[1].DISMAP[0] = 0xF777U;
PWM0->SM[2].DISMAP[0] = 0xF777U;
PWM0->SM[3].DISMAP[0] = 0xF777U;
/* PWM fault filter - 3 Fast periph. clocks sample rate, 5 agreeing samples to activate */
PWM0->FFILT |= PWM_FFILT_FILT_PER(2);
PWM0->FFILT |= PWM_FFILT_FILT_CNT(2);
/* All interrupts disabled, safe manual fault clearing */
PWM0->FCTRL &= ~(PWM_FCTRL_FLVL_MASK | PWM_FCTRL_FAUTO_MASK | PWM_FCTRL_FSAFE_MASK |
PWM_FCTRL_FIE_MASK);
/* Clear FCTRL register prior further settings */
PWM0->FCTRL |= PWM_FCTRL_FIE(0U);
/* FAULT 0 & FAULT 1 - Interrupt disable */
/* Internal OPAMP fault signals are active low. */
PWM0->FCTRL |= PWM_FCTRL_FLVL(0x0U);
PWM0->FCTRL |= PWM_FCTRL_FAUTO(0U);
PWM0->FCTRL |= PWM_FCTRL_FSAFE(0xFU);
```

4 修订历史

表 2. 修订历史

版本号	日期	实质性变更
0	2022 年 1 月 27 日	初版发布
1	2022 年 5 月 20 日	用 LPC553x/LPC55S3x 替代 LPC55S36

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