AN14512

如何调校MCX A系列上的时钟

第1.0版—2024年11月21日 应用笔记

文档信息

信息	内容
关键词	AN14512、MCXA、调校时钟、SCG、FIRC、SIRC
摘要	本应用笔记介绍了MCX A系列中的SCG模块，并描述了如何调校MCX A系列上的时钟。

1 介绍

MCX A系列微控制器是采用Arm Cortex-M33内核的通用型MCU，旨在以其可扩展的设备选项、低功耗以及智能外设满足广泛的应用需求。MCX A系列提供了多种时钟源，包括系统振荡器时钟（SOSC）、慢速内部参考时钟（SIRC，FRO12M）、快速内部参考时钟（FIRC，FRO192M）以及实时振荡器时钟（ROSC）。系统时钟生成器（SCG）模块可用于控制这些时钟，其中FIRC和SIRC均支持手动调校和自动调校功能。在开环条件下，FIRC和SIRC的精度为±3%。在需要更高精度的应用中，可使用自动调校功能来提高时钟精度。启用自动调校功能后，FIRC和SIRC的精度可分别达到±0.25%和±0.6%。本应用笔记介绍了MCX A系列中的SCG模块，并描述了如何调校MCX A系列上的时钟。

2 系统时钟生成器（SCG）概述

SCG模块为MCU提供主时钟及其他外设时钟。SCG从各种时钟源接收时钟输入，并生成MCU所需的时钟。

2.1 功能

图1展示了SCG模块的结构框图。

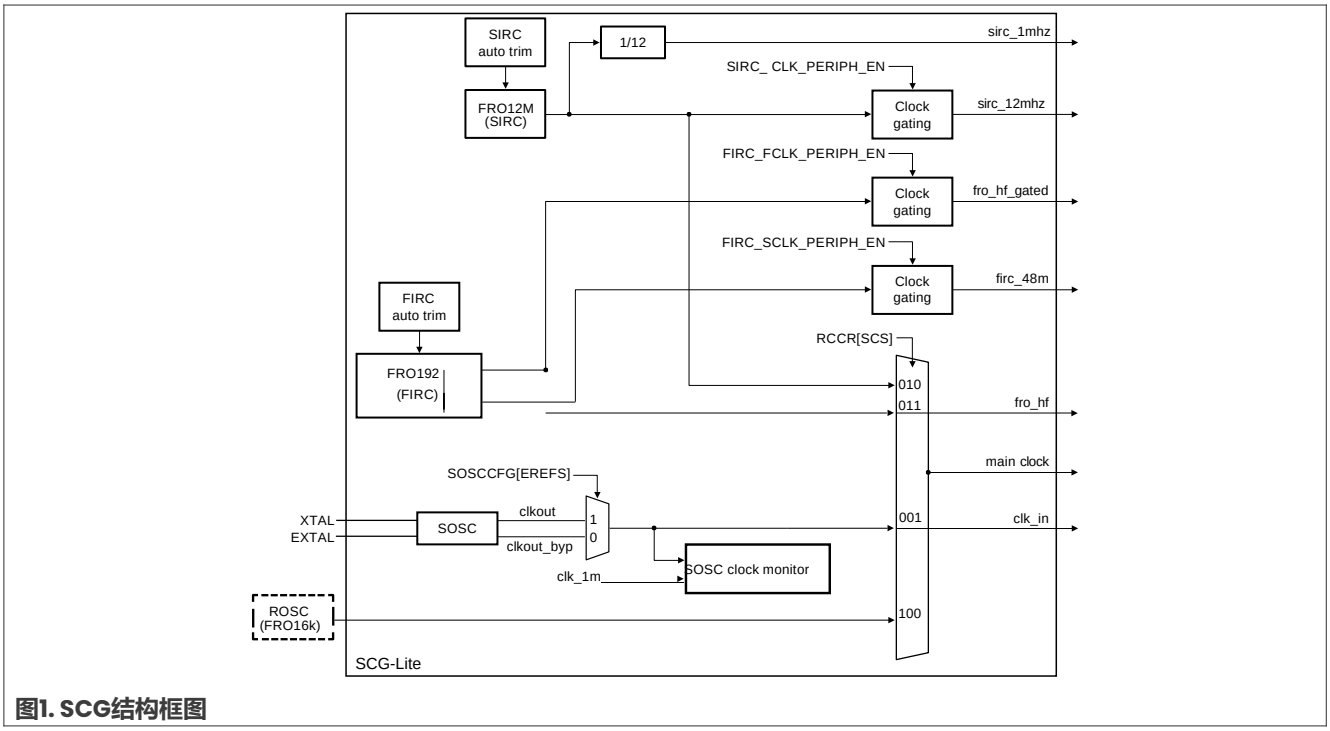

图1. SCG结构框图

系统启动时默认使用FIRC时钟源。系统时钟可在以下时钟源之间切换：FIRC、SIRC、SOSC和ROSC。

- FIRC (FRO192M)
  - FIRC可通过寄存器配置输出192/96/64/48MHz的时钟。
  - FIRC可通过频率虚像限制输出频率。

– FIRC具有调校功能
- SIRC (FRO12M)
  – SIRC可以输出12MHz时钟和由其分频得到的1MHz时钟。
  – SIRC具有调校功能
- SOSC
  – 需要一个外部晶振，工作频率范围为8MHz至50MHz。
- ROSC
  – ROSC的时钟源来自VBAT模块中的FRO16K时钟。

3 软件设计

本节介绍了调校时钟的具体步骤，并提供了示例代码。此代码基于FRDM-MCXA153 SDK 2.16.1，并使用FRDM-MCXA153开发板作为测试平台。

3.1 手动调校

FIRC时钟在芯片出厂前已经校准，其调校值在复位后被记录在FIRC调校寄存器（FIRCTRIM）中。用户可以使用FIRCTRIM手动调校时钟，如图2所示。

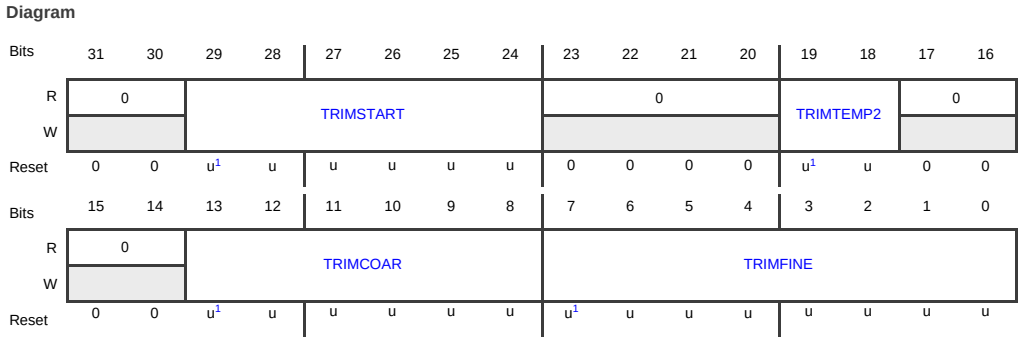

图2. FIRC调校寄存器

有两种调校精度：

- TRIMCOAR位用于粗调FIRC时钟，使其频率达到目标频率的约±3.2%范围内。
- TRIMFINE位用于细调FIRC时钟，使其频率达到目标频率的约±0.25%范围内。

***注：**对于TRIMCOAR，增加其值会使频率降低。中心点附近的频率变化率大约为每位2.5%，且数值越大，变化率越小。对于TRIMFINE，增加其值会使频率增加。中心点附近的频率变化率大约为每位0.06%，且数值越大，变化率越小。*

要手动调校FIRC时钟，请按照以下步骤操作：

1. 从FIRCTRIM寄存器中读取当前值并记录下来。
2. 将**0x5A5A**写入`TRIM_LOCK[TRIM_LOCK_KEY]`，将**1**写入`TRIM_LOCK[TRIM_UNLOCK]`，以解锁调校寄存器。
3. 将调校值与步骤1中记录的值相加，并写入FIRCTRIM寄存器。
4. 将**0x5A5A**写入`TRIM_LOCK[TRIM_LOCK_KEY]`，将**0**写入`TRIM_LOCK[TRIM_UNLOCK]`，以锁定调校寄存器。

FIRC手动调校的核心代码如下：

```
typedef enum
{
  TRIM_COARSE,
  TRIM_FINE
} trim_type;

/**
 * @brief     app_ FircManualTrim  Manual TrimFIRC clock
 * @param  type     TRIM_COARSE about 2.5%, TRIM_FINE about 0.06%
 *                 value   FIRCTRIM + value
 * @return   NULL
*/
void app_FircManualTrim(trim_type type,char value)
{
  uint32_t trim_value  = SCG0 -> FIRCTRIM;
  uint8_t  trim_coarse = (uint8_t)(trim_value >> 8);
  uint8_t  trim_fine   = (uint8_t)trim_value;
  PRINTF("%x\r\n", trim_value);
  /* UNLOCK the trim */
  SCG0 -> TRIM_LOCK = (SCG_TRIM_LOCK_TRIM_LOCK_KEY(0x5A5A)) |
 (SCG_TRIM_LOCK_TRIM_UNLOCK(1));
  if (type == TRIM_COARSE)   // coarse trim mode, use coarse trim register
  {
    trim_coarse = trim_coarse + value;
    SCG0 -> FIRCTRIM = (trim_value & 0xFFFF0000) | (trim_fine & 0xff) | ((trim_coarse &
 0x3f) << 8);
  }
  else if(type == TRIM_FINE) // fine trim mode, use fine trim register
  {
    trim_fine = trim_fine + value;
    SCG0 -> FIRCTRIM = (trim_value & 0xFFFF0000) | (trim_fine & 0xff)   | ((trim_coarse &
 0x3f) << 8);
  }
  trim_value  = SCG0 -> FIRCTRIM;
  /* LOCK the trim */
  SCG0 -> TRIM_LOCK = (SCG_TRIM_LOCK_TRIM_LOCK_KEY(0x5A5A)) |
 (SCG_TRIM_LOCK_TRIM_UNLOCK(0));
  PRINTF("%x\r\n", trim_value);
}
```

3.2 自动调校

FIRC和SIRC的精度为±3%（环境温度Ta在-40°C ~ 125°C之间）。在某些应用场景中，需要更高精度的时钟，此时可启用自动调校功能。自动调校后，FIRC和SIRC的精度可分别达到 ±0.25% 和 ±0.6%。

时钟调校需要一个外部晶振作为参考源。

要自动调校FIRC时钟，请按照以下步骤操作：

1. 启用SOSC时钟。
2. 等待SOSC时钟生效。
3. 将**2**写入`FIRCTCFG[TRIMSRC]`，以选择SOSC作为自动调校的时钟源。
4. 将**7**写入`FIRCTCFG[TRIMDIV]`，以将SOSC分频为1MHz（8MHz外部晶振）。
5. 将**0**写入`FIRCCSR[LK]`，以解锁FIRCCSR寄存器。
6. 将**1**写入`FIRCCSR[FIRCTREN]`，以启用自动调校。
7. 将**1**写入`FIRCCSR[FIRCTRUP]`，以启用更新。
8. 读取`FIRCCSR[FIRCVLD]`，直至其返回**1**，表示FIRC有效。
9. 读取`FIRCCSR[FIRCERR]`，以确保其返回**0**。

10. 读取FIRCCSR[TRIM_LOCK]，直至其返回**1**。
11. 将**1**写入FIRCCSR[LK]，以锁定FIRCCSR寄存器。

FIRC自动调校的核心代码如下：

```
/**
 * @brief     app_FircAutoTrim   Run Auto Trim to trim the clock using external crystal
 * @param   NULL
 * @return    NULL
*/
void app_FircAutoTrim()
{
 CLOCK_SetupExtClocking(8000000U);              // Enable the 8MHz external crystal
 SCG0 -> FIRCTCFG |= SCG_FIRCTCFG_TRIMSRC(2);    // Select the external crystal(SOSC) as the source
 SCG0 -> FIRCTCFG |= SCG_FIRCTCFG_TRIMDIV(7);    // Divide the SOSC to 1MHz
 SCG0 -> FIRCCSR  &= ~SCG_FIRCCSR_LK(1);         // Unlock the FIRCCSR register
 SCG0 -> FIRCCSR  |= SCG_FIRCCSR_FIRCTREN(1);    // Enable auto trim
 SCG0 -> FIRCCSR  |= SCG_FIRCCSR_FIRCTRUP(1);    // Enable update
 /* Until it returns 1, indicating FIRC is valid */
 while(!(SCG0 -> FIRCCSR & SCG_FIRCCSR_FIRCVLD_MASK));
 /* Until it returns 0, indicating no error */
 while( SCG0 -> FIRCCSR & SCG_FIRCCSR_FIRCERR_MASK);
 /* Until it returns 1, indicating FIRC auto trim locked to target frequency range */
 while(!(SCG0 -> FIRCCSR & SCG_FIRCCSR_TRIM_LOCK_MASK));
 SCG0 -> FIRCCSR  |= SCG_FIRCCSR_LK(1);           // Lock the FIRCCSR register
}
```

要自动调校SIRC时钟，请按照以下步骤操作：

1. 启用SOSC时钟。
2. 等待SOSC时钟生效。
3. 将**2**写入SIRCTCFG[TRIMSRC]，以选择SOSC作为自动调校时钟源。
4. 将**7**写入SIRCTCFG[TRIMDIV]，以将SOSC分频为1MHz（8MHz外部晶振）。
5. 将**0**写入SIRCCSR[LK]，以解锁SIRCCSR寄存器。
6. 将**1**写入SIRCCSR[SIRCTREN]，以启用自动调校。
7. 将**1**写入SIRCCSR[SIRCTRUP]，以启用更新。
8. 读取SIRCCSR[SIRCVLD]，直至其返回**1**，表示SIRC有效。
9. 读取SIRCCSR[SIRCERR]，确保其返回**0**。
10. 读取SIRCCSR[TRIM_LOCK]，直至其返回**1**。
11. 将**1**写入SIRCCSR[LK]，以锁定SIRCCSR寄存器。

SIRC自动调校的核心代码如下：

```
/**
 * @brief   app_SircAutoTrim   Run Auto Trim to trim the clock using external crystal
 * @param   NULL
 * @return  NULL
*/
void app_SircAutoTrim()
{
 CLOCK_SetupExtClocking(8000000U);              // Enable the 8MHz external crystal
 SCG0 -> SIRCTCFG |= SCG_SIRCTCFG_TRIMSRC(2);    // Select the external crystal(SOSC) as the source
 SCG0 -> SIRCTCFG |= SCG_SIRCTCFG_TRIMDIV(7);    // Divide the SOSC to 1MHz
 SCG0 -> SIRCCSR  &= ~SCG_SIRCCSR_LK(1);         // Unlock the SIRCCSR register
 SCG0 -> SIRCCSR  |= SCG_SIRCCSR_SIRCTREN(1);    // Enable auto trim
 SCG0 -> SIRCCSR  |= SCG_SIRCCSR_SIRCTRUP(1);    // Enable update
 /* Until it returns 1, indicating SIRC is valid */
 while(!(SCG0 -> SIRCCSR & SCG_SIRCCSR_SIRCVLD_MASK));
 /* Until it returns 0, indicating no error */
 while( SCG0 -> SIRCCSR & SCG_SIRCCSR_SIRCERR_MASK);
 /* Until it returns 1, indicating SIRC auto trim locked to target frequency range */
 while(!(SCG0 -> SIRCCSR & SCG_SIRCCSR_TRIM_LOCK_MASK));
 SCG0 -> SIRCCSR  |= SCG_SIRCCSR_LK(1);         // Lock the SIRCCSR register
}
```

注：*调校时钟完成后，请配置所需的外设。*

3.3 时钟输出

时钟输出功能是一个用于时钟监测的有用特性。某些引脚可以配置为时钟输出引脚，有关详情请参阅参考手册中的SYSCON章节。以MCXA153为例，可将P0_6、P3_6或P3_8配置为时钟输出引脚。配置引脚后，按照以下步骤设置SYSCON和MRCC寄存器：

1. 将**0**写入CLKUNLOCK[UNLOCK]，以解锁时钟配置寄存器。
2. 将**1**写入MRCC_CLKOUT_CLKSEL[MUX]，以选择**FIRC_DIV**作为时钟源（测量SIRC时，将**0**写入MRCC_CLKOUT_CLKSEL[MUX]）。
3. 将**15**写入MRCC_CLKOUT_CLKDIV[DIV]，以将分频值设置为**16**（测量SIRC时，将**11**写入MRCC_CLKOUT_CLKSEL[MUX]）。
4. 将**1**写入CLKUNLOCK[UNLOCK]，以锁定时钟配置寄存器。

时钟输出配置的核心代码如下：

```
  /* PORT3: Peripheral clock is enabled */
  CLOCK_EnableClock(kCLOCK_GatePORT3);
  /* PORT3 peripheral is released from reset */
  RESET_ReleasePeripheralReset(kPORT3_RST_SHIFT_RSTn);
  const port_pin_config_t port3_8_config = {/* Internal pull-up resistor is enabled */
                        kPORT_PullUp,
                        /* Low internal pull resistor value is selected. */
                        kPORT_LowPullResistor,
                        /* Fast slew rate is configured */
                        kPORT_FastSlewRate,
                        /* Passive input filter is disabled */
                        kPORT_PassiveFilterDisable,
                        /* Open drain output is disabled */
                        kPORT_OpenDrainDisable,
                        /* Low drive strength is configured */
                        kPORT_LowDriveStrength,
                        /* Normal drive strength is configured */
                        kPORT_NormalDriveStrength,
                        /* Pin is configured as CLKOUT */
                        kPORT_MuxAlt12,
                        /* Digital input enabled */
                        kPORT_InputBufferEnable,
                        /* Digital input is not inverted */
                        kPORT_InputNormal,
                        /* Pin Control Register fields [15:0] are not locked */
                        kPORT_UnlockRegister};
  /* PORT3_8 is configured as CLK_OUT */
  PORT_SetPinConfig(PORT3, 8U, &port3_8_config);
/**
 * @brief    app_ClockOut   clock output set, to observe clock signal
 * @param    NULL
 * @return   NULL
*/
void app_ClockOut()
{
 SYSCON -> CLKUNLOCK           = SYSCON_CLKUNLOCK_UNLOCK(0);       // Unlock the register
 MRCC0  -> MRCC_CLKOUT_CLKSEL = MRCC_MRCC_CLKOUT_CLKSEL_MUX(1);   // FIRC_DIV
 MRCC0  -> MRCC_CLKOUT_CLKDIV = MRCC_MRCC_CLKOUT_CLKDIV_DIV(15); // 1/16 Frequency
 SYSCON -> CLKUNLOCK           = SYSCON_CLKUNLOCK_UNLOCK(0);       // Lock the register
}
```

4 板级测试

为了测试时钟调校功能，使用了FRDM-MCXA153 开发板，如图3所示。该开发板配备了板载调试器。使用USB-C电缆通过J15接口将开发板连接到计算机，用于下载和调试。在本测试中，P3_8被用作时钟输出引脚。将P3_8（开发板上的J3-11）和GND连接到示波器探头，并捕获输出信号。

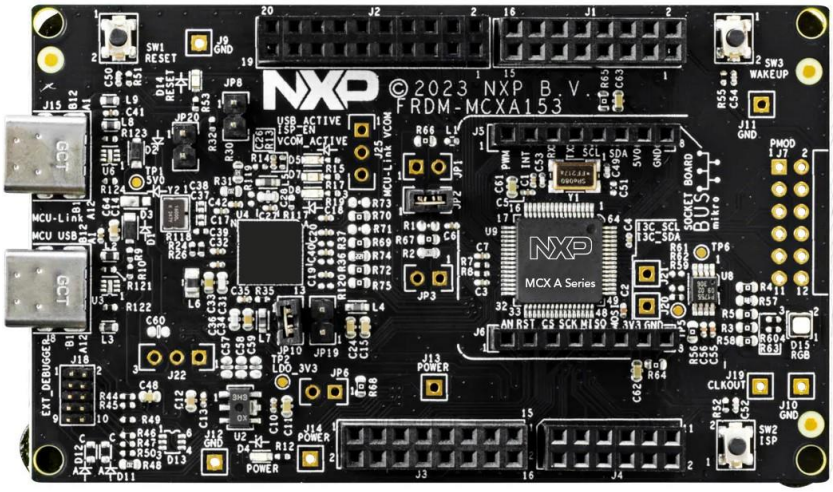

图3. FRDM-MCXA153开发板

4.1 测试结果

在测量FIRC频率时，将**15**写入MRCC_CLKOUT_CLKDIV[DIV]，以将分频值设置为**16**。在本测试中，将FIRC设置为96MHz，并通过P3_8输出时钟。调校前，时钟输出如下所示，频率约为6.045MHz，大约为96MHz的1/16，如图4所示。

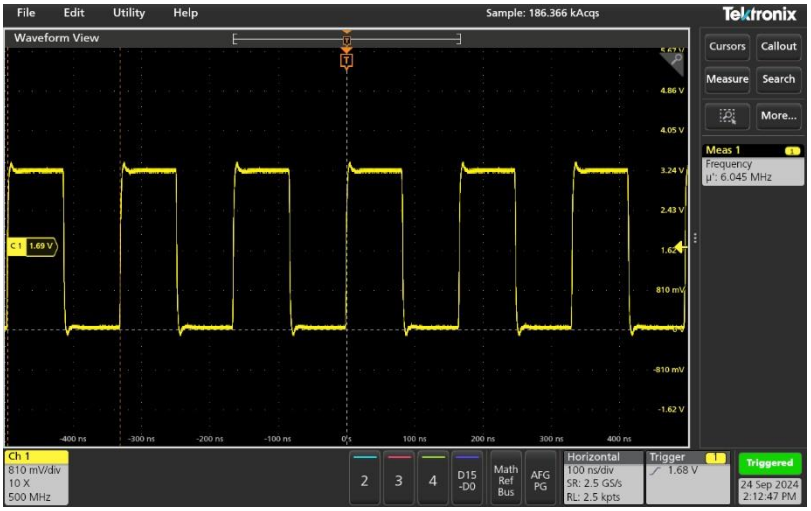

图4. 调校前的FIRC时钟输出

如果给FIRCTRIM[TRIMCOAR]加上**1**，频率约为5.911MHz，频率降低了约2.2%，如图5所示。

图5. FIRCTRIM[TRIMCOAR] + 1后的FIRC时钟输出

如果给`FIRCTRIM[TRIMCOAR]`减去**1**，频率约为6.183MHz，频率增加了约2.3%，如图6所示。

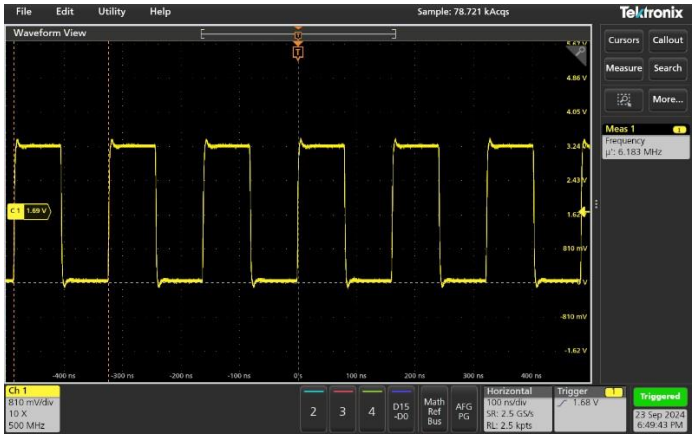

图6. FIRCTRIM[TRIMCOAR] - 1后的FIRC时钟输出

如果给`FIRCTRIM[TRIMFINE]`加上**4**，频率约为6.059MHz，频率增加了约0.23%，如图7所示。

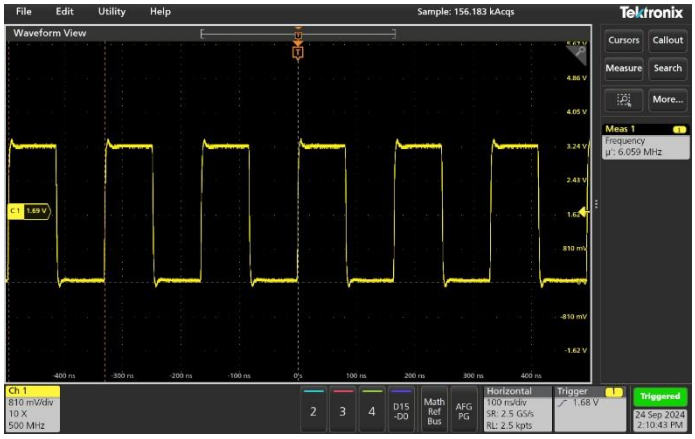

图7. FIRCTRIM[TRIMFINE] + 4后的FIRC时钟输出

如果给FIRCTRIM[TRIMFINE]减去**4**，频率约为6.032MHz，频率降低了约0.22%，如图8所示。

图8. FIRCTRIM[TRIMFINE] - 4后的FIRC时钟输出

运行FIRC自动调校功能后，频率约为6.000MHz，如图9所示，FIRC时钟的精度得到了提升。

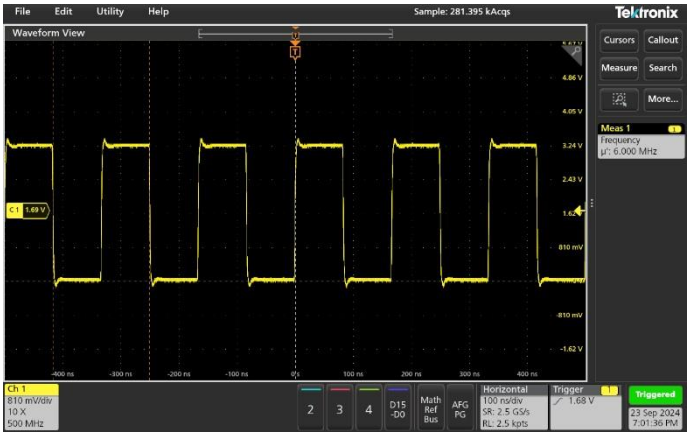

图9. 自动调校后的FIRC时钟输出

在测量SIRC频率时，将**11**写入MRCC_CLKOUT_CLKDIV[DIV]，以将分频值设置为**12**。在本测试中，将SIRC设置为12MHz，并通过P3_8输出时钟。调校前，时钟输出如下所示，频率约为1.007MHz，大约为12MHz的1/12，如图10所示。

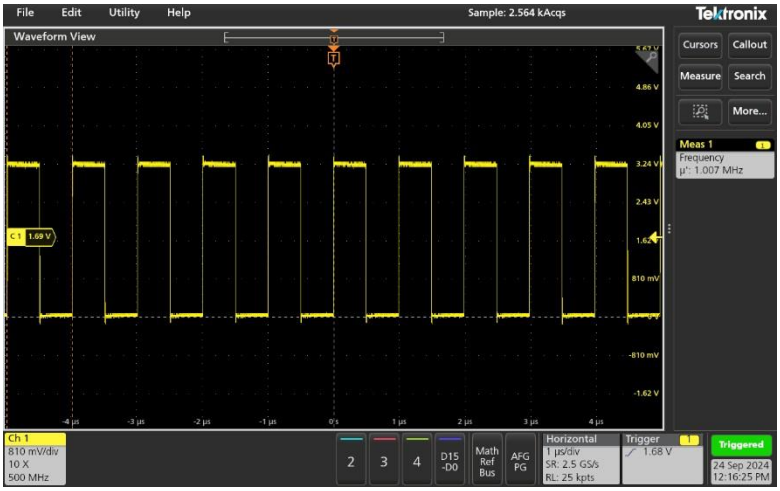

图10. 调校前的SIRC时钟输出

运行SIRC自动调校功能后，频率约为1.000MHz，如图11所示。SIRC时钟的精度得到了提升。

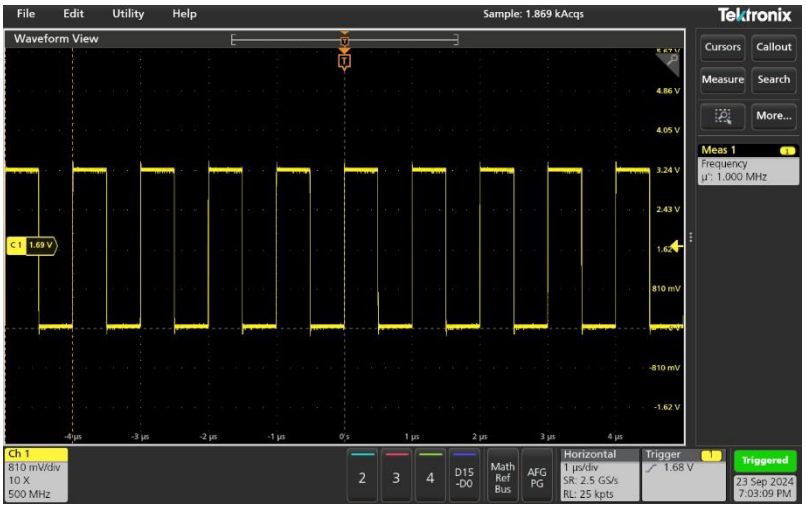

图11. 自动调校前的SIRC时钟输出

5 结论

本应用笔记提供了相关信息和代码，以帮助用户调校MCX A系列上的时钟，并进行测试来验证时钟输出。

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7 修订历史

表1汇总了本文档的修订情况。

表1. 修订历史

文档编号	发布日期	说明
AN14512 v.1.0	2024年11月21日	首次公开发布

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