WIMAX8360EWP
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# Using the PowerQUICC™ II Pro MPC8360E to Build a Line Card in 802.16 (WiMAX) Wireless Equipment

The IEEE-defined 802.16 standards are designed to ensure an always-on wireless broadband data connection for both fixed (first generation, 802.16-2004) and mobile (802.16e) users. With the ability to support multiple Quality of Service (QoS) classes, an 802.16 network can support mobile voice, high-speed data, and video in a wireless network. The 802.16 standards are endorsed by the WiMAX (Worldwide Interoperability for Microwave Access) forum. This ensures both equipment interoperability and promotion of the standard.

With the potential to offer three revenue streams from a single IP packet network, the triple play of voice, video, and data is the goal of every telecoms operator. IP is the key enabler toward this goal and in time it will be universal. Designed to support IP, 802.16 can thus benefit the network vendors. An overview of an IP-based 802.16 network is shown in Figure 1.

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freescale™ semiconductor

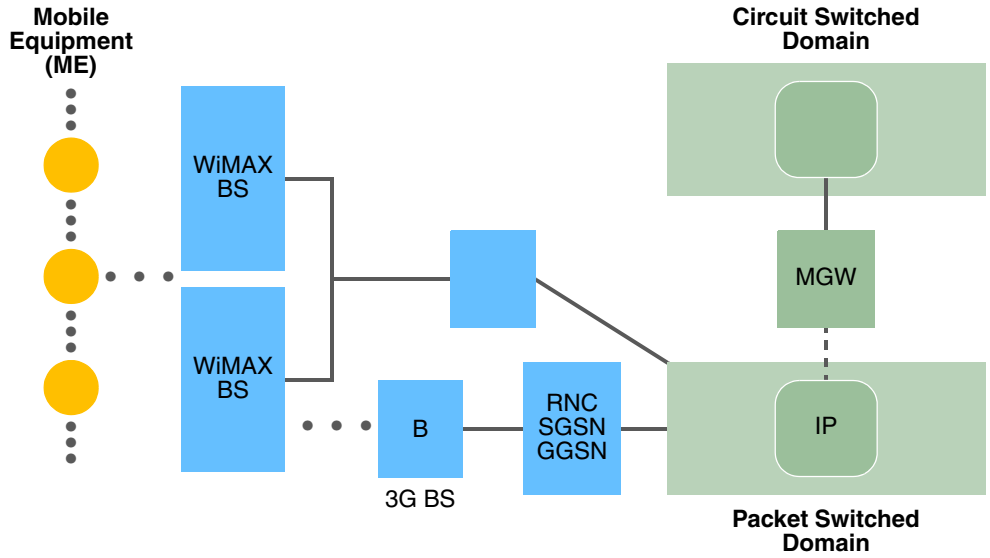


**Figure 1. Overview of WiMAX Wireless Network**

Designing a high-performance, cost-effective 802.16-2004 or 802.16e compatible base station provides many challenges to wireless equipment designers, including migration from RF and PHY to MAC processing. This document addresses implementation of the MAC-layer using Freescale devices that use the QUICC Engine™.

# 1 Design Challenges

The 802.16-2004 and 802.16e standards are still maturing and so support a large number of options. Ongoing modifications and uncertainty about the options needed for an implementation require a flexible and programmable solution.

In system design, the designer must decide how to partition the PHY and MAC layer processing among the different devices. This decision is challenging due to the large amount of interworking needed between the 802.16 MAC and PHY layers compared to other wireless systems such as 802.11, GSM and various 3G standards. Depending on the physical layer implementation, the MAC chip must be able to perform high-speed encryption/decryption, CRC, HCS calculation and frame building, and to offload PDU and frame formatting from the physical layer.

Within the MAC layer, the split between the MAC CPS, CS and network layers depends on board/rack, device and interconnect requirements. Protocols, traffic types and traffic volumes used on the network interface vary. In addition, advanced systems will be developed that could include co-location of 802.16 with 2G or 3G base stations. Such trends push the processing and interfacing demands even further. Inside a base station, the MAC CPS (Common Part Sublayer) and CS (Convergence Sublayer) layers can be either implemented in the same device/physical location or split among multiple devices or locations. In a multi-sector base station, a possible solution is to implement a single network interface card for MAC CS execution for multiple (up to 6) sectors, providing GbE and optional TDM interfaces towards the network carrying data and voice traffic with optional uplink QoS. In a single sector base station or super access point, the MAC CS and MAC CPS can be run on the same physical device in order to keep the cost low.

The scheduling algorithms for uplink and downlink form the core of any 802.16 MAC. Scheduling algorithms must be easy to program but also must have access to many input parameters such as input queue status and size (in bytes), ARQ data availability, physical layer performance, and system configurations.

The option for re-use of base station software for development of high end customer premises equipment, such as super access points, requires a low-cost, low-power and highly integrated silicon solution that provides flexibility to add new features and functions through in field software upgrades as market demands dictate in the future.

# 2 Freescale Semiconductor Solutions

As technology standards for 802.16 WiMax change, a programmable communication-processing platform that can evolve with technology provides equipment vendors with a competitive advantage. With these system requirements in mind, Freescale is pleased to introduce the latest addition to its popular PowerQUICC™ family of microprocessors—the PowerQUICC II Pro MPC8360E.

The MPC8360E incorporates the e300, 603e core which includes 32 Kbytes of L1 instruction and data caches, 32-bit PCI bridge, four DMA channels, USB support, dual 32-bit DDR memory controller, a double precision floating point unit and on-board memory management units. A block diagram of the MPC8360E is shown in Figure 2.

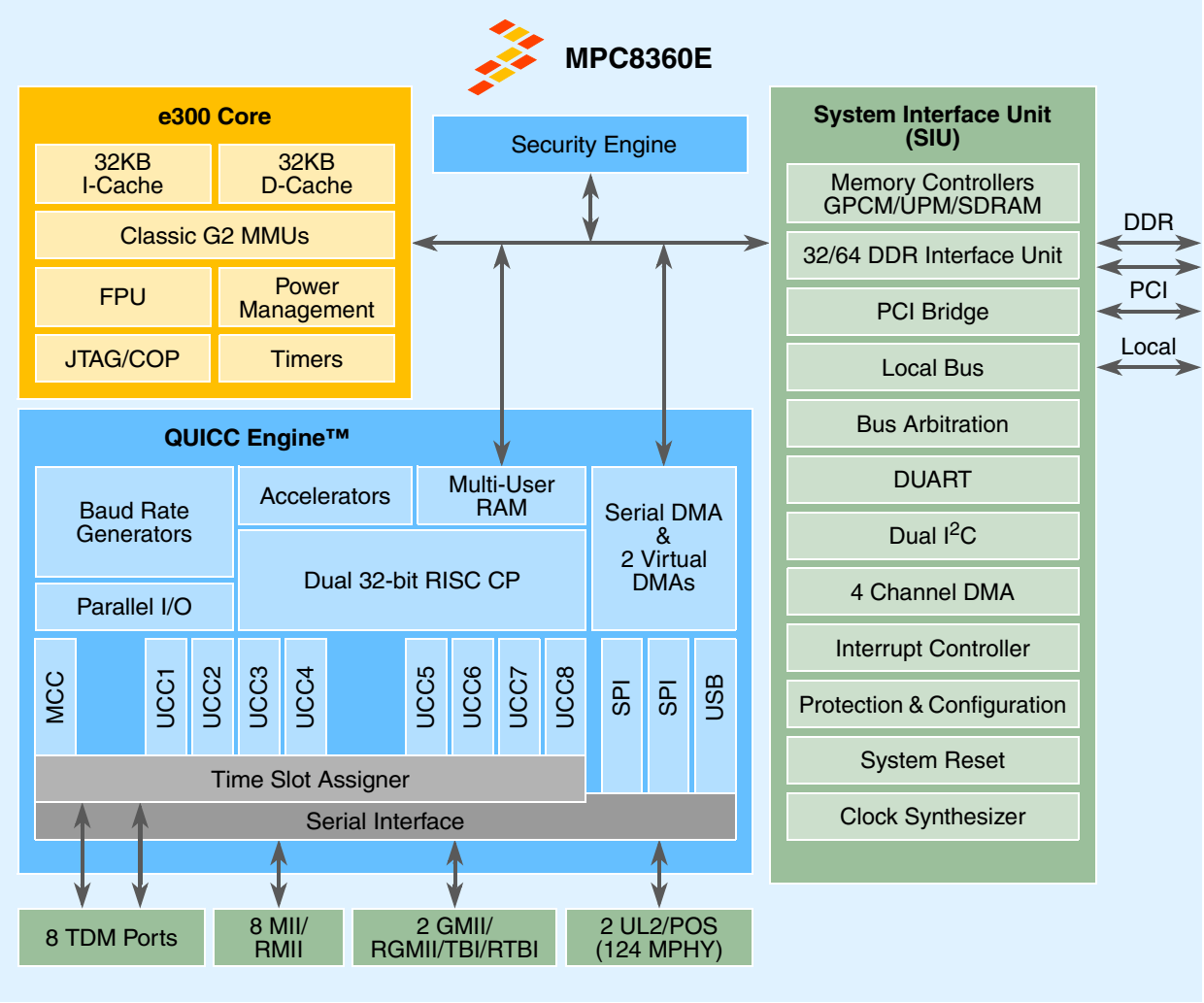


**Figure 2. MPC8360E Block Diagram**

A new communications complex—the QUICC Engine™—forms the heart of the networking capability of the MPC8360E. The QUICC Engine contains several peripheral controllers and integrates two 32-bit RISC controllers.

Each RISC controller can control multiple peripherals and work together to provide increased aggregated system bandwidth for higher throughput applications. Protocol support is provided by the main workhorses of the device—the unified communication controllers (UCCs) and multi-channel communication controller (MCC).

Each of the eight UCCs can support a variety of communication protocols: 10/100/1000 Mbps Ethernet through a Media-Independent Interface, ATM / POS PHY support up to OC-12 speeds, Serial ATM, Multi-PHY ATM, HDLC, UART, Multi-Link/Class PPP, BISYNC and 64 TDM channels. Each MCC is capable of supporting up to 256 TDM channels in either transparent or HDLC channel modes and multiplexing almost any combination of sub-groups into a single or multiple TDM stream. Inverse Multiplexing over ATM is supported and allows ATM traffic to be distributed across multiple E1/T1 circuits. This allows service providers to lease the exact bandwidth that subscriber's request.

In addition, the QUICC Engine can also support two UTOPIA level 2 or two POS interfaces, each interface capable of supporting 124 Multi-PHY, or up to two, 128 Multi-PHY interfaces using extended address mode. The QUICC Engine also features an integrated 8-port, L2 Ethernet switch which can provide 4 priority levels on each port, VLAN functionality, IGMP snooping, network auto-negotiation function, store-and-forward switching and packet-error filtering. Enhanced interworking features within the QUICC Engine helps offload the main CPU. The QUICC Engine can provide ATM-to-ATM switching, Ethernet to ATM switching with L3 / L4 support and PPP interworking.

The MPC8360E's security engine allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. The security-processing accelerator provides hardware acceleration for the DES, 3DES, AES, SHA-1, MD-5, and ARC-4 algorithms. It includes a public key accelerator and an on-chip random number generator.

In summary, the MPC8360E provides a highly integrated, fully programmable communications processor that allows reuse of existing legacy PowerQUICC II and III software drivers and microcode packages. This helps ensure that a low cost system solution can be quickly developed and will offer flexibility to accommodate new standards and evolving system requirements.

## 2.1 The PowerQUICC II Pro MPC8360E

The PowerQUICC II Pro MPC8360E is a high performance, highly integrated communication processor solution that offers the following.

### 2.1.1 MPC8360E Features

- High-performance, low power (< 5W typical power dissipation), and cost-effective communications processor
- The MPC8360E QUICC Engine offers a future proof solution for next generation designs by supporting programmable protocol termination, network interface termination, and interworking features to meet evolving protocol standards
- Single platform architecture supports the convergence of IP packet networks and ATM networks, including interworking between these networks
- Simplified network interface card design with a cost-effective single chip data plane/control plane solution for ATM or IP packet processing (or both). This reduced component count, board power consumption and board real estate.
- Universal network interface card design for multiple applications, which lowers costs and reduces time-to-market

- Built-in proprietary, hardware accelerators that accelerate data plane traffic, such as interworking, and control plane packet snooping, such as IGMP, VLAN tagging, DHCP, and so on
- DDR memory controller—one 64-bit or 2x32-bit interfaces that split data and control plane traffic at up to 333 MHz
- e300 PowerPC core (enhanced version of 603e core with 32K bytes of Level 1 Instruction and 32K bytes of Level 1 Data caches)
- 32-bit PCI interface
- 32-bit Local Bus interface
- USB
- Integrated 8-port L2 Ethernet switch
  - 8 connection ports of 10/100 Mbps MII/RMII & one CPU internal port
  - Each port supports four priority levels
  - Priority levels used with VLAN tags or IP TOS field to implement QoS
  - QoS types of traffic, such as voice, video, and data
- Security engine provides termination or encrypted plane traffic
- High degree of software compatibility with previous-generation PowerQUICC processor-based designs for backward compatibility and easier software migration
- Seamless connection to PowerQUICC III family devices for increased control (CPU) application processing requirements

#### 2.1.1.1 Protocols

- ATM SAR up to 622Mbps (OC-12) full duplex, with ATM traffic shaping (ATF TM4.1) for up to 64K ATM connections
- Support for ATM AAL1 structured and unstructured Circuit Emulation Service (CES 2.0)
- Support for IMA and ATM Transmission Convergence sub-layer
- ATM OAM handling features compatible with ITU-T I.610
- PPP, Multi-Link (ML-PPP), Multi-Class (MC-PPP) and PPP mux in accordance with the following RFCs: 1661, 1662, 1990, 2686 and 3153
- IP termination support for IPv4 and IPv6 packets including TOS, TTL and header checksum processing
- L2 Ethernet switching using MAC address or IEEE 802.1P/Q VLAN tags
- Support for ATM (AAL2/AAL5) to Ethernet (IP) interworking
- Extensive support for ATM statistics and Ethernet RMON/MIB statistics.
- Support for 256 channels or HDLC/Transparent or 128 channels of SS#7

#### 2.1.1.2 Serial Interfaces

- Support for two UL2 / POS-PHY interfaces with 124 Multi-PHY addresses each.
- Support for two 1000Mbps Ethernet interfaces using GMII or RGMII, TBI, RTBI.
- Support for up to eight 10/100Mbps Ethernet interfaces using MII or RMII
- Support for up to eight T1 / E1 / J1 / E3 or DS-3 serial interfaces
- Support for dual UART, I²C and SPI interfaces.

System scalability is also made available through the number of UCCs and MCCs. The initial implementation offers eight UCCs and one MCC, however as a result of the system-on-a-chip design methodology used for the QUICC Engine, these numbers can be scaled to support an optimized mix of communications channels. The flexible architecture of the QUICC Engine allows customers to customize their own application protocol and filtering requirements, allowing Freescale to add more RISC engines and/or UCCs on future family derivatives.

## 2.2 Development Environment

Development tools, hardware platforms, software building blocks and application-specific software solutions are available from Freescale and our Freescale Alliance Program, including third party protocol and signaling stack suppliers, real time operating systems support and a variety of applications software support. All of this builds upon the existing industry standard PowerQUICC family support program.

### 2.2.1 Software Development Tools

To simplify and accelerate the development process, Freescale will provide a user-friendly, integrated development environment (IDE), which includes a compiler, instruction set simulator and debugger for the e300 PowerPC core.

### 2.2.2 Application Development System (ADS)

Freescale provides an ADS board as a reference platform and programming development environment for the MPC8360E with a complete Linux Board Support Package. The ADS board will support on-board DDR SDRAM memory, a PCI interface, and a debug port and can be configured with optional daughter cards supporting protocols such as OC-3 or OC-12 ATM, 8xT1/E1 and Ethernet (10/100/1000Base T).

Also available is a complete development system based around the AdvancedTCA (ATCA) form factor chassis with a choice of AMC cards that can be operate stand alone, or as modular inserts into the main processor baseboard. This allows maximum flexibility for prototyping wireless network interface, control and base band applications using Freescale silicon solutions.

### 2.2.3 Modular Software Building Blocks

The QUICC Engine will be supported by a complete set of configurable device API drivers and initialization software. Figure 3 shows the wealth of software protocols that the QUICC Engine with the e300 PowerPC™ core is able to provide.

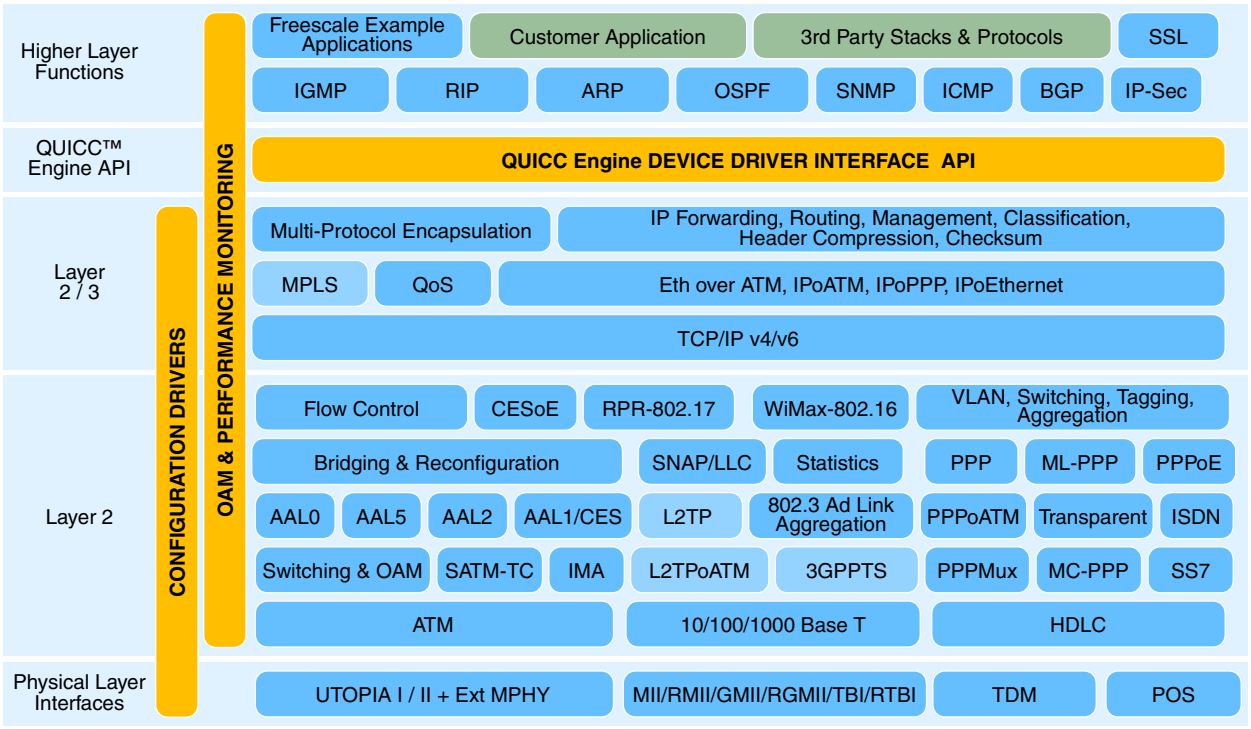


**Figure 3. Software Protocol Support for the QUICC Engine**

# 3 Application Example

Equipment manufacturers need a high degree of flexibility in their design, in parallel with increasing demands on fields such as power consumption, PCB real estate, design time and cost. Such combination of demands cannot be dealt with by implementations relying heavily on ASIC or FPGA technology.

Freescale proposes a software-defined solution based on our PowerPC TM, QUICC TM Engine and DSPs based on Starcore technology. As an implementation example, a line card with PHY and MAC based on these technologies is shown below in Figure 4.

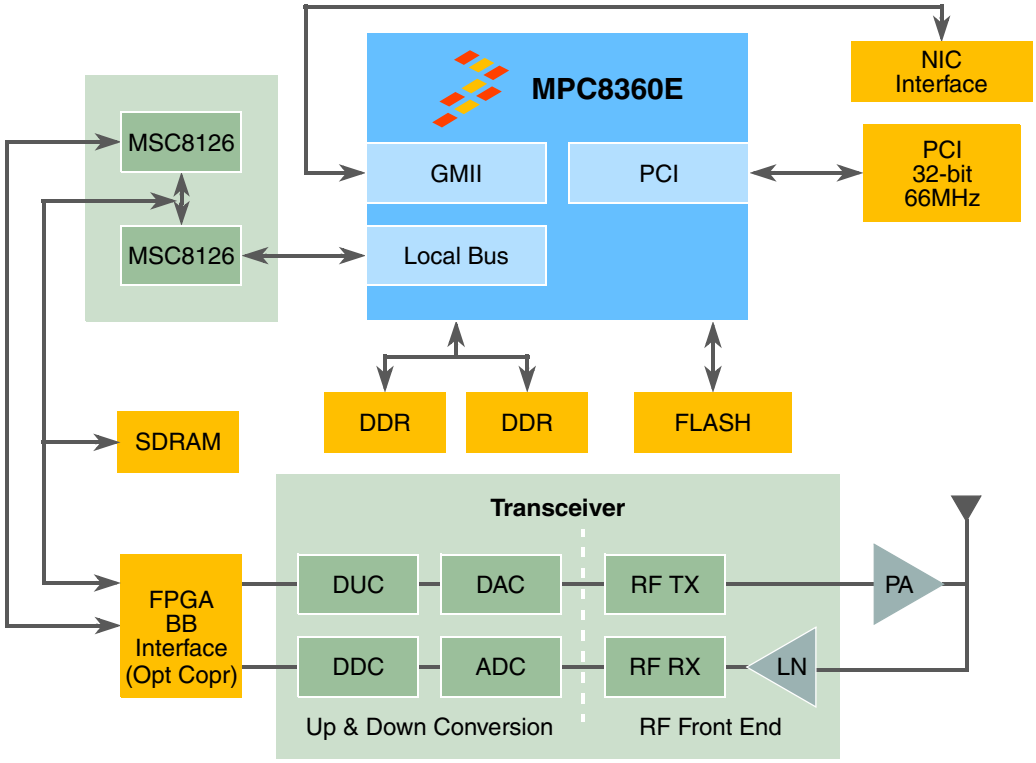


**Figure 4. 802.16 Line Card/Single Sector BS High-Level Architecture**

In this implementation, several line cards are connected through a single network interface card through Ethernet (multiple Fast Ethernet or a single Gigabit Ethernet link). A more detailed overview of the application of the MPC8360E in this approach is detailed in Figure 5 and Figure 6 for a line card and network interface card.

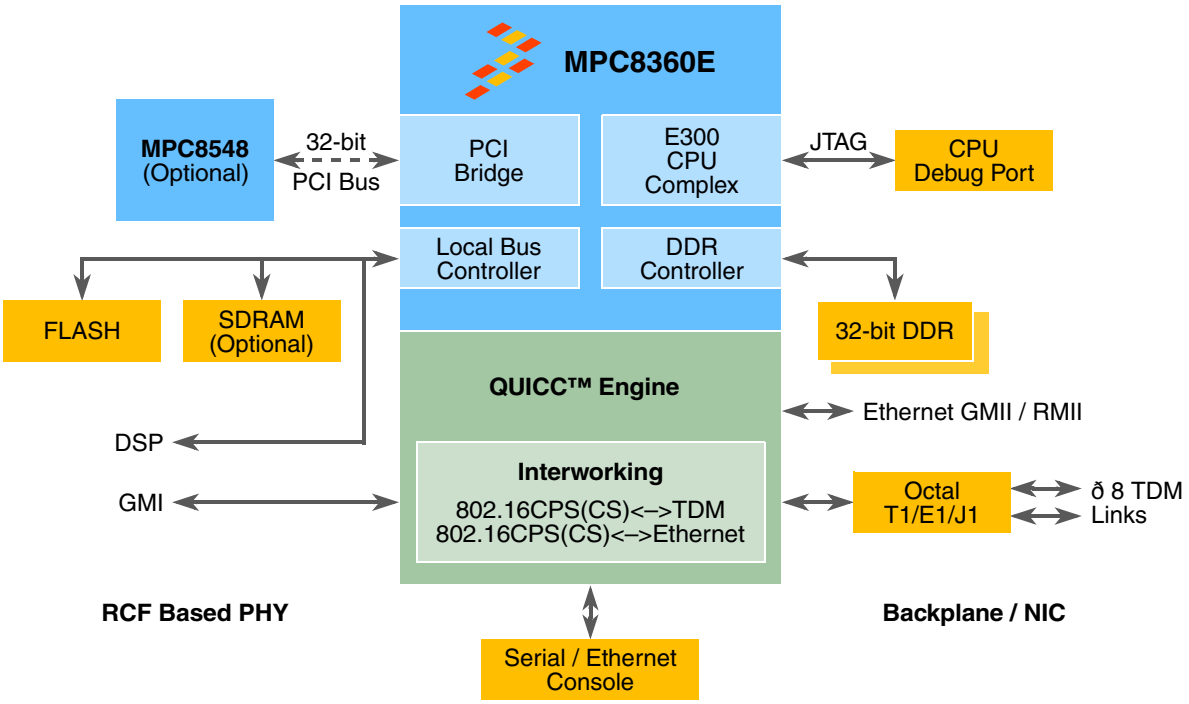


**Figure 5. Possible 802.16 Line Card or Single Sector BS Implementation Using MPC8360E**

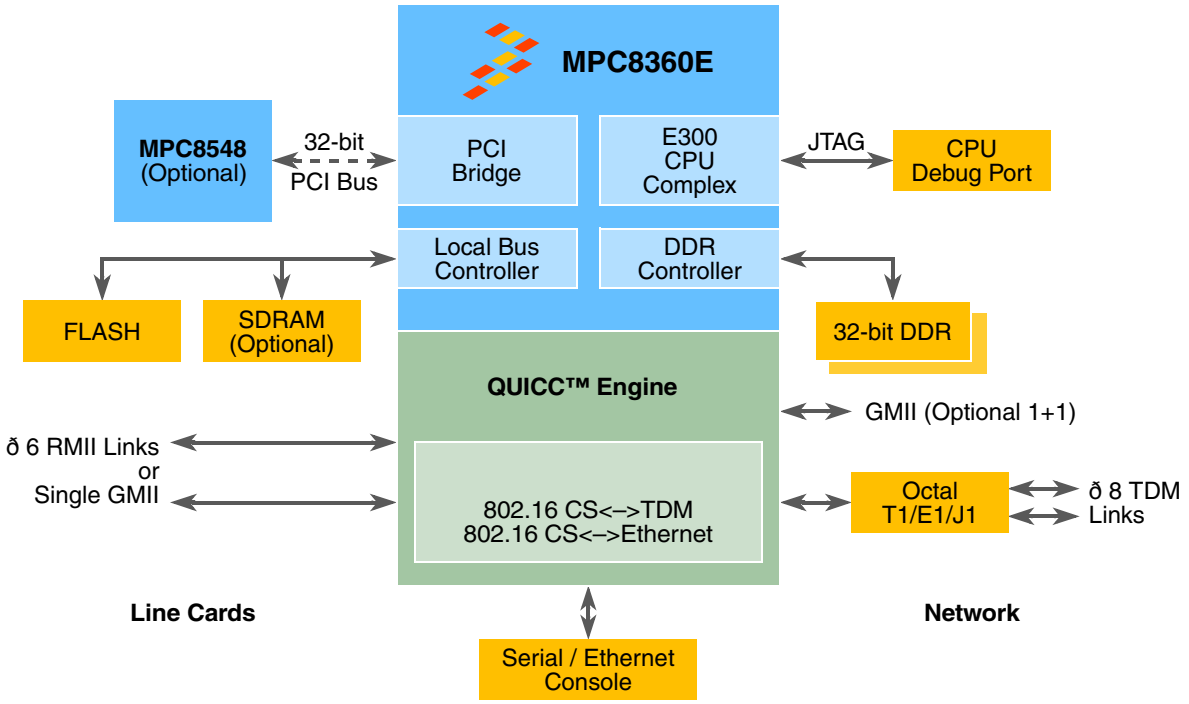


**Figure 6. Possible 802.16 Network Interface Card Implementation Using MPC8360E**

Optionally, the network interface can be TDM or any other standard protocol. The backplane carries Ethernet frames containing proprietary defined packets containing among others CID and IP payload.

In this system, the line card handles the MAC CS layer (classification, PHS, optionally uplink QoS), whereas the MAC CPS and control functionality are processed on the line cards.

For line card use, the QUICC Engine Typically handles the lower layer MAC, as where the upper MAC is implemented in software on the e300 core (although other partitioning is also feasible). The interfacing capabilities of the MPC8360E are used for interconnect to the PHY layer (for example, using Ethernet) on one side and to the network on the other (Ethernet), with an option to extend the raw processing power needed by connecting an MPC8548 through PCI. Also, legacy systems with a UTOPIA backplane or single sector base station implementations needing TDM interfacing is supported without adding extra hardware.

On the network interface card, connectivity is the main concern. The MPC8360E supports two Gigabit Ethernet connections for a 1:1 redundant network interface or back plane, or up to 8 RMII connections if a star-topology backplane is implemented. Of course, UTOPIA, TDM and other interfacing capabilities are fully supported. Support for classification of the downlink traffic arriving from the network interface, PHS (Payload Header Suppression), uplink classification (from CID) and optionally uplink QoS is implemented in software.

# 4 Software

Options in the standard and interpretations of PHS allows for different implementations of an 802.16 MAC layer. For this reason, flexibility—the option for vendor differentiation—is a major consideration when choosing the optimum MAC layer device. To keep design time low, a fully programmable ‘building block’ based software solution is best. This also allows for different parts of the system (such as frame building/de-mapping and the MAC CS layer) to be implemented on different devices if required.

Figure 7 shows an 802.16 MAC layer implementation built from software blocks. In the downlink direction, after classification and optional PHS, the SDUs are enqueued into per-CID queues, which are emptied by the fragmentation/packing block. This is done using input from the downlink scheduler algorithm. After saving the transmitted data including time-stamp information in a separate ARQ queue, the generated PDU is formatted (inclusion of CRC, HCS and encryption) and forwarded on to the frame builder. High-speed hardware based encryption for all supported algorithms and CRC blocks are needed in order to keep up with increasing throughput demands.

After frame de-mapping in the uplink, incoming PDUs are first checked for valid CRC and HCS before being hardware decrypted. The de-fragmentation/unpacking block separates out the individual fragments from the PDU, builds SDUs and updates the uplink ARQ status. After optional uplink QoS the SDUs are transmitted towards the network. Optionally, SDUs can be forwarded to a VoIP card for decoding to a TDM stream or transcoding. The uplink scheduler has to coordinate with the downlink scheduler, especially when implementing a TDD system.

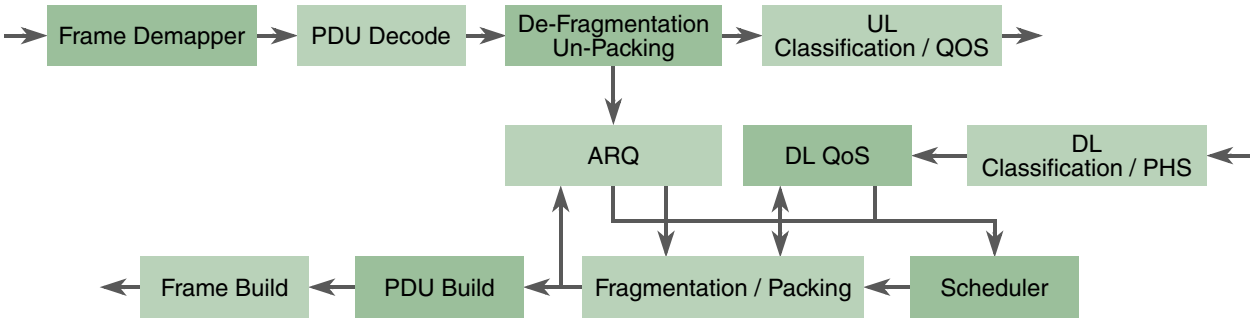


**Figure 7. Possible 802.16 CPS+CS MAC Layer Implementation in Software Blocks**

Two major building blocks of this system are the downlink and uplink schedulers. For ease of implementation, these could be implemented as a high-priority task in the e300 core, or for better throughput they could be placed inside the QUICC Engine. In either case, care must be taken to give access to all information needed for scheduling decisions such as queue depth in bytes (for both ARQ and normal traffic), channel configuration (e.g. modulation, block size) and service agreements.

For sub-optimized implementations or the case that more computational intensive processing is needed, a second processor such as an MPC8548 can be connected through the PCI bus to increase the CPU performance even more, as is shown in Figure 5.

Standards development forecast an increased throughput need in the foreseeable future. Therefore, it is important to implement a system which not only delivers sufficient throughput in the short term but also provides enough headroom for future generations and is scalable towards more advanced applications. Examples of such applications could be co-location with other 802.16 base stations, and 2G, 3G or 802.11 networks. Such systems demand not only hardware headroom but also a broad range of supported protocol stacks, including ATM (AAL2, AAL5), VLAN, RTP, PPP, ML/MC-PPP, PPPMux, IP header compression, routing, IP-Sec and QoS.

# 5 Summary

The PowerQUICC II Pro MPC8360E with the new QUICC Engine is a significant step forward in performance, integration and cost effectiveness for a wide variety of application. For flexible, high performance, wireless network interface cards, the MPC8360E offers a comprehensive feature set that enables cost effective solutions with an unrivalled level of versatility to evolve as both standards and the system requirements change.

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