MTUDSLAM8360EWP
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Using the PowerQUICC™ II Pro MPC8360E to Build a Multi-Tenant Unit Pizza-DSLAM

The connected world has begun to transition from traditional dial-up to high-speed broadband, primarily through the use of one of many DSL services. DSL services use the copper wiring of existing telephony cabling to transfer both voice and data, so the distance from the local exchange to the deployed end-user equipment directly affects the maximum achievable DSL data rate. This is of concern for network equipment manufacturers for several reasons:

- Physical installation costs associated with providing customers with access to the local loop exchange are significant
- The level of service that can be supplied to the end customer is highly dependant on distance to the exchange
- Management costs involved in controlling the services made available to multiple single-lines or users can be significant

These market trends are driving network equipment manufacturers to look to alternative, low-cost solutions that offer advanced broadband data and voice services to end customers.

Deploying DSL or broadband services to Multi-Tenant-Units (MTUs) offers network equipment manufacturers an attractive, cost-effective alternative that avoids the distance limitations and deployment costs related with DSL services and access to the local exchange. MTU solutions allow the ‘last mile’ from the local exchange to the street cabinet and the ‘last drop’ from the street

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cabinet to the end-user equipment to be controlled entirely by the service provider, as shown in Figure 1.

MTUs provide a high concentration of commercial or residential users. The cheapest deployment solution for the service provider is to re-use existing wiring such as Ethernet or DSL in conjunction with an access concentrator or DSLAM (DSL Access Multiplexer). Providers can then run fiber from their Central Office (CO) out to a small DSLAM located within an MTU and give building tenants the services and data rates they require. These small MTU DSLAMs are often called Pizza-DSLAMs due to their small, thin, box-like dimensions.

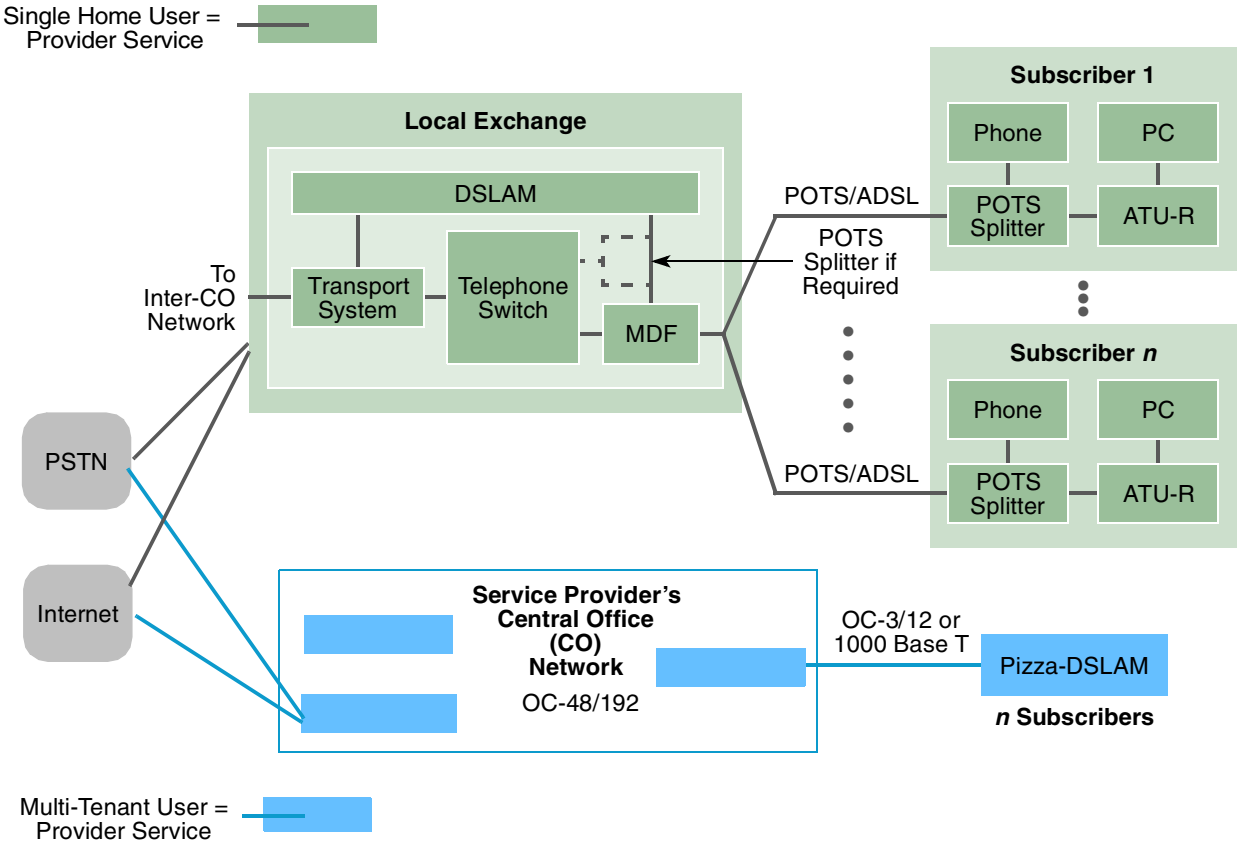

Figure 1. MTU Pizza-DSLAM—Bypassing the Local Loop

1 Design Challenges

Although direct cost is often the most critical factor in a design, a rapid return on investment (ROI) is of paramount concern for service providers. This is directly related to the processing capabilities of the end Pizza-DSLAM design. For example, high system throughput and the number of supported ports allow a faster ROI as more tenants are connected from one DSLAM and can be charged more for premium rate services. Typically, 48 ports or more are currently required with total aggregated throughput rates in excess of 1Gbps.

Because many older buildings do not have distributed LAN networks established, Pizza-DSLAMs must be capable of supporting cable-based technologies such as xDSL, as well as modern packet based technologies. A Pizza-DSLAM that can handle both ATM and Ethernet traffic means that wider range of services can be supported. This type of design also dictates a requirement for ATM-Ethernet interworking.

The Pizza-DSLAM must be capable of terminating a tenant's ATM-based xDSL lines and encapsulating the data into packets before forwarding them across the service provider's Gigabit Ethernet backbone. Using ATM as the

transport technology, MTU connections can easily migrate to higher data rates, such as OC-3/STM-1 or OC-12/STM-4, allowing future throughput enhancements and services for connected tenants. The support of different ATM Adaptation Layers (AAL1, AAL2 and AAL5) allows a range of triple-play services to be supported.

Because all connected MTU users share the same common Pizza-DSLAM, protecting the privacy of each subscriber's data becomes a highly critical issue. This requires that the end Pizza-DSLAM solution is capable of supporting Virtual LANs (VLAN) using the 802.1Q standard—allowing complete subnet separation and isolation for each connected tenant. Preventing users from accessing the databases of other tenants is another design requirement and this can be achieved using MPLS VPN as well as port filtering techniques such as IP/MAC filtering and IP access control.

Using Pizza-DSLAMs to connect multiple users together presents further design challenges. Most service providers have service level agreements, which guarantee a specific Quality of Service (QoS) with options for further service upgrades. Furthermore, streaming applications such as video, multi-media games and Voice over IP (VoIP) require a guaranteed bandwidth. Pizza-DSLAM designs must therefore have the ability to provide multi-level QoS, guaranteed bandwidth levels and the ability to bill per network usage.

Traditional design challenges are relevant to Pizza-DSLAM solutions. Silicon suppliers must ensure that their end-system communications processor can support a wide range of applications protocols and communication functions and also must have the capability to deliver scaleable system solutions in the future, while keeping system cost and power consumption to a minimum. In addition, the need to provide high levels of support in the form of applications protocols and software drivers, development systems, and third party tools solutions is mandatory.

2 Freescale Semiconductor Solutions

In the competitive DSLAM market, highly integrated, cost-effective and scalable system solutions are required. With these system requirements in mind, Freescale is pleased to introduce the latest addition to its popular PowerQUICC family of microprocessors—the PowerQUICC II Pro MPC8360E.

The MPC8360E incorporates the e300, 603e core which includes 32 Kbytes of L1 instruction and data caches, 32-bit PCI bridge, four DMA channels, USB support, dual 32-bit DDR memory controller, a double precision floating point unit and on-board memory management units. A block diagram of the MPC8360E is shown in Figure 2.

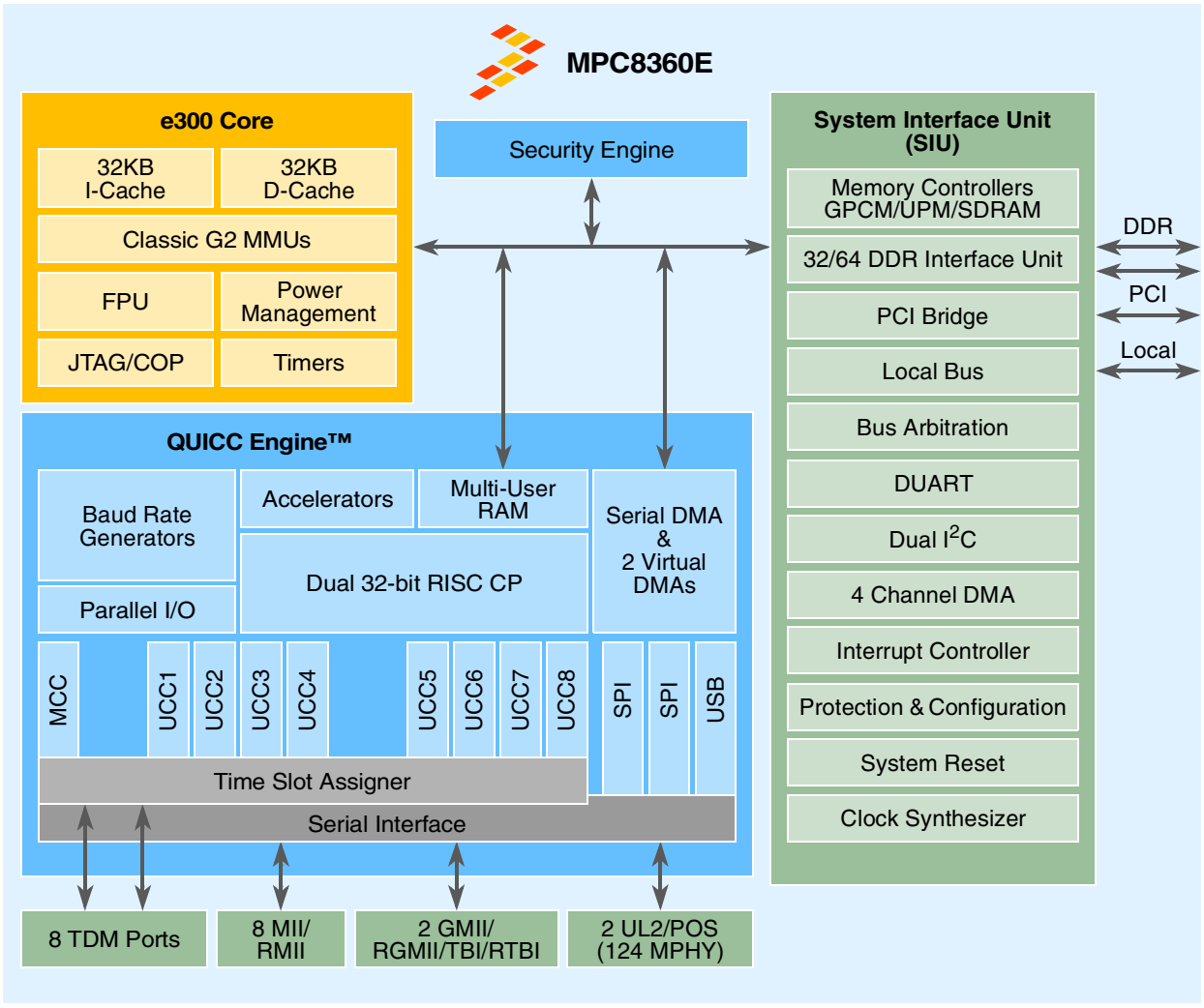

Figure 2. MPC8360E Block Diagram

A new communications complex—the QUICC™ Engine—forms the heart of the networking capability of the MPC8360E. The QUICC Engine contains several peripheral controllers and integrates two 32-bit RISC controllers. Each RISC controller can control multiple peripherals and work together to provide increased aggregated system bandwidth for higher throughput applications. Protocol support is provided by the main workhorses of the device—the unified communication controllers (UCCs) and multi-channel communication controller (MCC).

Each of the eight UCCs can support a variety of communication protocols: 10/100/1000 Mbps Ethernet through a Media-Independent Interface, ATM / POS PHY support up to OC-12 speeds, Serial ATM, Multi-PHY ATM, HDLC, UART, Multi-Link/Class PPP, BISYNC and 64 TDM channels. Each MCC is capable of supporting up to 256 TDM channels in either transparent or HDLC channel modes and multiplexing almost any combination of sub-groups into a single or multiple TDM stream. Inverse Multiplexing over ATM is supported and allows ATM traffic to be distributed across multiple E1/T1 circuits. This allows service providers to lease the exact bandwidth that subscriber's request.

In addition, the QUICC Engine can also support two UTOPIA level 2 or two POS interfaces, each interface capable of supporting 124 Multi-PHY, or up to two, 128 Multi-PHY interfaces using extended address mode. The QUICC Engine also features an integrated 8-port, L2 Ethernet switch which can provide 4 priority levels on each port,

VLAN functionality, IGMP snooping, network auto-negotiation function, store-and-forward switching and packet-error filtering. Enhanced interworking features within the QUICC Engine helps offload the main CPU. The QUICC Engine can provide ATM-to-ATM switching, Ethernet to ATM switching with L3 / L4 support and PPP interworking.

The MPC8360E's security engine allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. The security-processing accelerator provides hardware acceleration for the DES, 3DES, AES, SHA-1, MD-5, and ARC-4 algorithms. It includes a public key accelerator and an on-chip random number generator.

In summary, the MPC8360E provides DSLAM line-card vendors with a highly integrated, fully programmable communications processor that allows reuse of existing legacy PowerQUICC II and III software drivers and microcode packages. This helps ensure that a low cost system solution can be quickly developed and will offer flexibility to accommodate new standards and evolving system requirements.

2.1 The PowerQUICC II Pro MPC8360E

The PowerQUICC II Pro MPC8360E is a high performance, highly integrated communication processor solution that offers the following.

2.1.1 MPC8360E Features

- High-performance, low power (< 5W typical power dissipation), and cost-effective communications processor
- The MPC8360E QUICC Engine offers a future proof solution for next generation designs by supporting programmable protocol termination, network interface termination, and interworking features to meet evolving protocol standards
- Single platform architecture supports the convergence of IP packet networks and ATM networks, including interworking between these networks
- Simplified network interface card design with a cost-effective single chip data plane/control plane solution for ATM or IP packet processing (or both). This reduced component count, board power consumption and board real estate.
- Universal network interface card design for multiple applications, which lowers costs and reduces time-to-market
- Built-in proprietary, hardware accelerators that accelerate data plane traffic, such as interworking, and control plane packet snooping, such as IGMP, VLAN tagging, DHCP, and so on
- DDR memory controller—one 64-bit or 2x32-bit interfaces that split data and control plane traffic at up to 333 MHz
- e300 PowerPC core (enhanced version of 603e core with 32 Kbytes of Level 1 Instruction and 32 Kbytes of Level 1 Data caches)
- 32-bit PCI interface
- 32-bit Local Bus interface
- USB
- Integrated 8-port L2 Ethernet switch
  - 8 connection ports of 10/100 Mbps MII/RMII & one CPU internal port
  - Each port supports four priority levels
  - Priority levels used with VLAN tags or IP TOS field to implement QoS

  - QoS types of traffic, such as voice, video, and data
- A security engine provides termination or encrypted plane traffic
- High degree of software compatibility with previous-generation PowerQUICC processor-based designs for backward compatibility and easier software migration
- Seamless connection to PowerQUICC III family devices for increased control (CPU) application processing requirements

2.1.1.1 Protocols

- ATM SAR up to 622Mbps (OC-12) full duplex, with ATM traffic shaping (ATF TM4.1) for up to 64K ATM connections
- Support for ATM AAL1 structured and unstructured Circuit Emulation Service (CES 2.0)
- Support for IMA and ATM Transmission Convergence sub-layer
- ATM OAM handling features compatible with ITU-T I.610
- PPP, Multi-Link (ML-PPP), Multi-Class (MC-PPP) and PPP mux in accordance with the following RFCs: 1661, 1662, 1990, 2686 and 3153
- IP termination support for IPv4 and IPv6 packets including TOS, TTL and header checksum processing
- L2 Ethernet switching using MAC address or IEEE 802.1P/Q VLAN tags
- Support for ATM (AAL2/AAL5) to Ethernet (IP) interworking
- Extensive support for ATM statistics and Ethernet RMON/MIB statistics.
- Support for 256 channels or HDLC/Transparent or 128 channels of SS#7

2.1.1.2 Serial Interfaces

- Support for two UL2 / POS-PHY interfaces with 124 Multi-PHY addresses each.
- Support for two 1000Mbps Ethernet interfaces using GMII or RGMII, TBI, RTBI.
- Support for up to eight 10/100Mbps Ethernet interfaces using MII or RMII
- Support for up to eight T1 / E1 / J1 / E3 or DS-3 serial interfaces
- Support for dual UART, I²C and SPI interfaces.

System scalability is also made available through the number of UCCs and MCCs. The initial implementation offers eight UCCs and one MCC, however as a result of the system-on-a-chip design methodology used for the QUICC Engine, these numbers can be scaled to support an optimized mix of communications channels. The flexible architecture of the QUICC Engine allows customers to customize their own application protocol and filtering requirements, allowing Freescale to add more RISC engines and/or UCCs on future family derivatives.

2.2 Development Environment

Development tools, hardware platforms, software building blocks and application-specific software solutions are available from Freescale and our Freescale Alliance Program, including third party protocol and signaling stack suppliers, real time operating systems support and a variety of applications software support. All of this builds upon the existing industry standard PowerQUICC family support program.

2.2.1 Software Development Tools

To simplify and accelerate the development process, Freescale will provide a user-friendly, integrated development environment (IDE), which includes a compiler, instruction set simulator and debugger for the e300 PowerPC core.

2.2.2 Application Development System (ADS)

Freescale provides an ADS board as a reference platform and programming development environment for the MPC8360E with a complete Linux Board Support Package. The ADS board will support on-board DDR SDRAM memory, a PCI interface, and a debug port and can be configured with optional daughter cards supporting protocols such as OC-3 or OC-12 ATM, 8xT1/E1 and Ethernet (10/100/1000Base T).

Also available is a complete development system based around the AdvancedTCA (ATCA) form factor chassis with a choice of AMC cards that can be operate stand alone, or as modular inserts into the main processor baseboard. This allows maximum flexibility for prototyping wireless network interface, control and base band applications using Freescale silicon solutions.

2.2.3 Modular Software Building Blocks

The QUICC Engine will be supported by a complete set of configurable device API drivers and initialization software. Figure 3 shows the wealth of software protocols that the QUICC Engine with the e300 PowerPC™ core is able to provide.

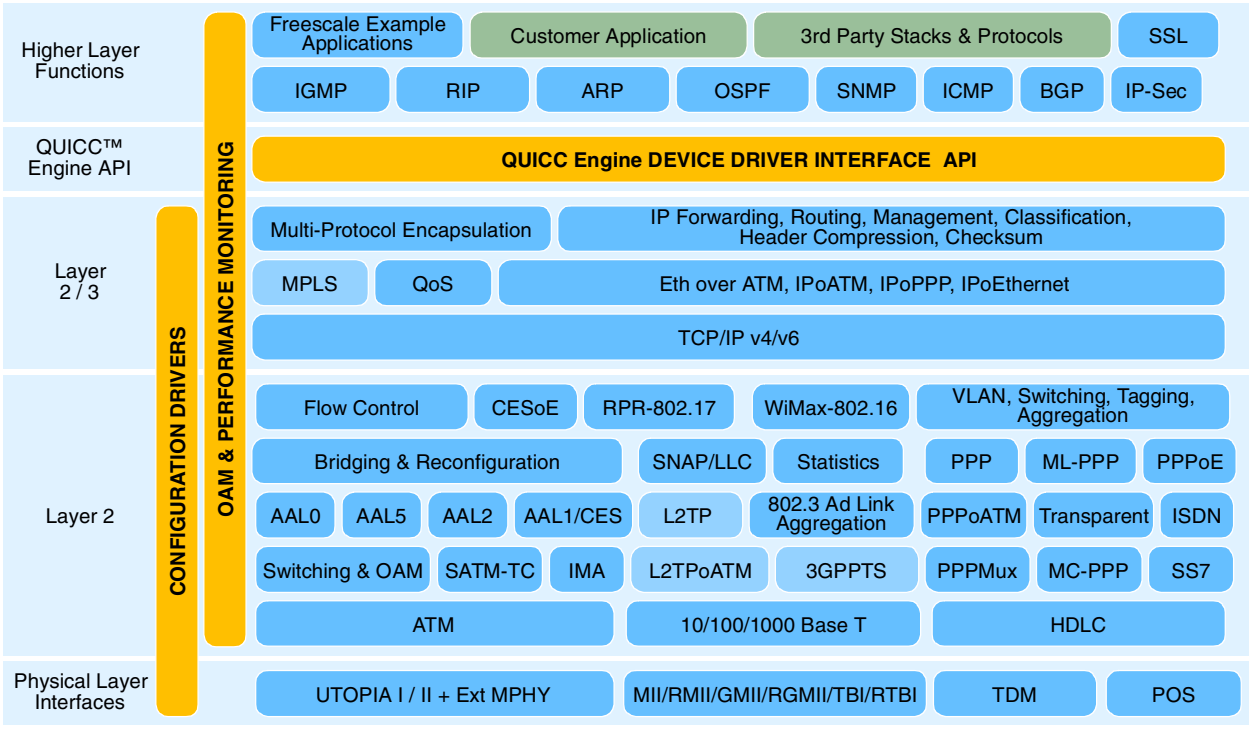

Figure 3. Software Protocol Support for the QUICC Engine

3 Pizza-DSLAM MTU Application Example

The internal features and protocols supported by the MPC8360E allow a wide range of different network solutions to be developed. Figure 4 illustrates how a typical MTU Pizza-DSLAM application can facilitate the convergence of packet and circuit switched networks.

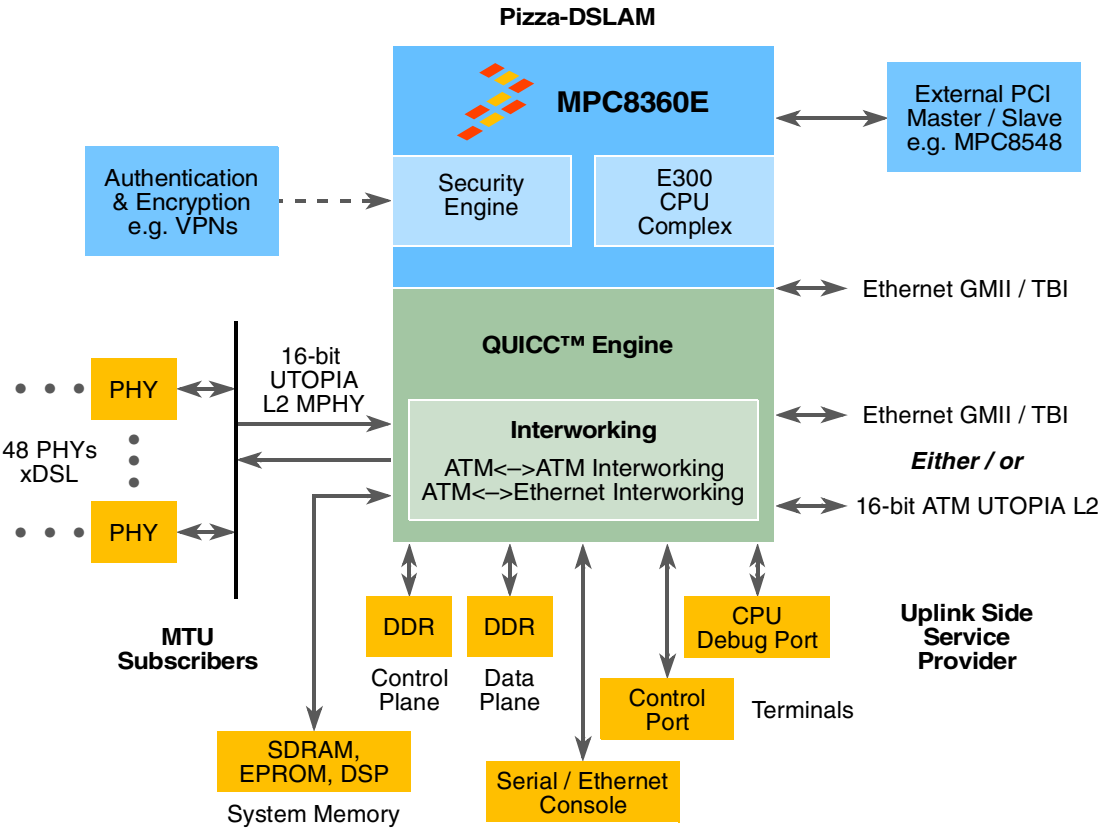

Figure 4. Freescale MPC8360E Pizza-DSLAM Example

As shown on the left hand side of the Figure 4, MTU subscribers connect to the DSLAM via DSL PHYs and the integrated UTOPIA interface on the MPC8360E.

If we consider that the application in Figure 4 is handling 48 ports of ADSL2 then each port will have a maximum data rate of 12Mbps downstream (for Annex A & B compliant equipment) and 1Mbps upstream (for Annex J compliant equipment). This generates an aggregate bandwidth of 624Mbps that must be handled through the uplink. Connection to the service provider's central office can be made using either two Gigabit Ethernet interfaces or an ATM interface depending on the type of switch fabric in the uplink network. Again, both Gigabit Ethernet MACs are fully integrated within the MPC8360E to minimize system footprint and simplify board layout.

In this type of application, the MPC8360E uses its internal interworking features to offload the e300 CPU. ATM-ATM interworking is used to transfer data from the ATM based DSL MTU subscriber inputs, through the RISC cores within the QUICC Engine and out through the other ATM UTOPIA on the uplink port. In the event that the uplink switch fabric is Ethernet-based then ATM-Ethernet interworking is provided by the MPC8360E.

The main system memory is provided by the DDR interface, which can either support one 64-bit or two 32-bit interfaces. This dual DDR architecture allows equipment providers to partition system parameters and data in an extremely efficient way. This helps ensure that data does not get blocked as the data plane can be completely

decoupled between the QUICC Engine/DDR memory and control plane transactions. The local bus can be used for SDRAM or on-board FLASH Eprom. The remaining unused UCCs can be configured as system terminals to allow some external I/O mechanism for debug and control. Finally, should the condition arise, the CPU can be debugged via the on-board JTAG interface.

4 Summary

The PowerQUICC II Pro MPC8360E with the new QUICC Engine is a significant step forward in performance, integration and cost effectiveness for a wide variety of applications. For flexible, high performance, multi-tenant user unit DSLAM the MPC8360E offers a comprehensive feature set that enables cost effective solutions with an unrivalled level of versatility to evolve as both standards and the system requirements change.

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