White Paper

MCM69C233WP/D
Rev. 2, 1/2003

MPC8260 PowerQUICC II™ to CAM Interfacing – MCM69C233

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The purpose of this document is to provide the designer a hardware method of interfacing the Motorola MPC8260 PowerQUICC II™ Integrated Communications Processor with the MCM69C233 Motorola Flexible Content Addressable Memory (CAM).

The following topics are addressed:

1 MPC8260 PowerQUICC II™

Motorola’s PowerQUICC II™ processor family is the next generation of Motorola’s leading PowerQUICC line of integrated communication processors. The MPC8260 integrates two main components, the embedded MPC603e G2 core and the Communications Processor Module (CPM). The CPM simultaneously supports three fast serial communications controllers (FCCs), two multichannel controllers (MCCs), four serial communications controllers (SCCs), two serial management controllers (SMCs), one serial peripheral interface (SPI), and one I2C interface.

2 Motorola Content Addressable Memories (CAMs)

The MCM69C233 is a flexible content addressable memory (CAM) that can contain 4096 entries of 64 bits. It is implemented with standard 4-transistor SRAM cells. The widths of the match field and the output field are programmable. At 66 MHz, the match time is designed to be less than or equal to 210 nanoseconds. As a result, the Motorola CAM is well suited for datacom applications such as Virtual Path Identifier/Virtual Circuit Identifier (VCI/VPI) translation in ATM switches up to OC12 (622 Mbps) data rates and Media Access Control (MAC) address lookup in Ethernet/Fast Ethernet bridges. The CAM is also well suited for fully associative disk drive cache and RAID applications. The match request rate of the MCM69C233 is user defined with a trade-off between the match request rate and the rate of new entries added to the CAM.

3 CAM Interface

The CAM consists of two independent ports: the control port and the match port. They have different functionality and control requirements. The MPC8260 local bus asserts one unique chip select for control port access and another for the match port. Because the MPC8260 is only able to assert one chip select per memory bank access, the MPC8260 accesses one CAM port at a time; the CAM control port and match port cannot be selected simultaneously. Also note on the MPC8260, some functions are multiplexed with other functions on the same pins. Particularly, on some pins, there are SDRAM signals that reside with signals that are used in the MPC8260/CAM interface. Therefore for this interface, SDRAM cannot be used on the local bus along with the CAM.

3.1 Control Port Interfacing Using the MPC8260 GPCM

The CAM control port is an asynchronous 16-bit read/write port. The control port signals consist of A2-A0 (Address), $\overline{\text{SEL}}$ (Select), $\overline{\text{IRQ}}$ (Interrupt), $\overline{\text{DTACK}}$ (Data Acknowledgement), $\overline{\text{WE}}$ (Write Enable), and $\overline{\text{RESET}}$.

The MPC8260 can reset the CAM in software, as the $\overline{\text{RESET}}$ input of the CAM is driven by the hardware reset of the MPC8260. For write transactions, the CAM address and data value should be valid, and the $\overline{\text{WE}}$ should be low when the $\overline{\text{SEL}}$ signal is asserted to begin a write cycle. Address, $\overline{\text{WE}}$, and $\overline{\text{SEL}}$ signal values should be held until the CAM asserts the $\overline{\text{DTACK}}$ signal to end the write cycle. Note however, that $\overline{\text{DTACK}}$ will not be used in this application and is pulled up with a 1kΩ resistor. The MPC8260 has an internal signal that will end the write transaction. See the Option Register setting in section 4.1 for further details. For read transactions, the address value should be valid and the $\overline{\text{WE}}$ signal should be high when $\overline{\text{SEL}}$ is asserted. Both signals (address, $\overline{\text{WE}}$, and $\overline{\text{SEL}}$) should hold their values until the CAM asserts the $\overline{\text{DTACK}}$ signal to end the read cycle. Again, as in the likewise manner of the write sequence, $\overline{\text{DTACK}}$ will not be used to end the read transaction.

This memory controller chip behavior can be accomplished via the MPC8260 Memory Controller's General Purpose Chip Select Machine (GPCM). The GPCM allows flexible interfacing between the MPC8260, SRAM, EPROM, flash EPROM, ROM devices and external peripherals. The table below lists the interface signals of the GPCM.

Table 1. GPCM Interface Signals

60x Bus	Local Bus	Comments
$\overline{\text{CS}}$ [0-11]		Device select
$\overline{\text{WE}}$[0-7]	$\overline{\text{LWE}}$[0-3]	Write enables for write cycles
$\overline{\text{OE}}$	$\overline{\text{LOE}}$	Output enables for read cycles
$\overline{\text{PGTA}}$	$\overline{\text{LGTA}}$	Transaction Termination
BCTLx	LWR	Data Buffer Controls/Local Write-Read

From the table, GPCM signals can be generated either on the 60x bus or the local bus. For this document, the MPC8260/CAM control port interfacing will take place on the local bus. The Write enable ($\overline{\text{LWE}}$[0-3]) and the Transaction Termination signal ($\overline{\text{LGTA}}$) will not be used.

A device select from the MPC8260, $\overline{\text{CS}}$[1], functions as the CAM $\overline{\text{SEL}}$ while the $\overline{\text{LWR}}$ acts as the CAM $\overline{\text{WE}}$. The control port is only accessible through 16-bit accesses. Therefore, the CAM address lines A[2:0] will map to the MPC8260 address lines A[28:30] (Each byte of data within the MPC8260 addressing

scheme has a unique address. Since data transactions will occur on 16-bit intervals [two bytes], A[31] of the MPC8260 address will not be used). The CAM control port data bus (DQ[15:0]) will connect to the MPC8260's local data bus LCL_D[0-15]. The CAM also includes the $\overline{IRQ}$ signal that can optionally alert the user of certain conditions within the CAM. For this demonstration, $\overline{IRQ}$ is not used and is pulled up by means of a 1kΩ resistor.

3.2 Match Port Interfacing Using the MPC8260 UPM

The CAM match port is synchronous to the input clock (K). The match port is 32 bits wide with read/write capability. Accesses to the match port from the MPC8260 consist of a write transaction followed by a read. The write cycle drives match data into the CAM. This data is latched in when the CAM LH/$\overline{SM}$ (Latch High/Start Match) signal asserts. The completion of a match search is indicated with the CAM $\overline{MC}$ (Match Complete) asserting. If a match is found, $\overline{MS}$ (Match Successful) asserts. The MPC8260 performs a read cycle with data being driven by the CAM with the CAM output enable, $\overline{G}$.

The MPC8260 Memory Controller's User-Programmable Machine (UPM) will be mapped to the match port of the CAM. The UPM provides flexible interfaces to a wide array of memory devices. The heart of the UPM is the programmable internal-memory RAM array. Each 64-bit word, which is programmed by the user, specifies the signal values for a given clock cycle that are driven on the external memory pins. The table below lists the interface signals of the UPM:

Table 2. UPM Interface Signals

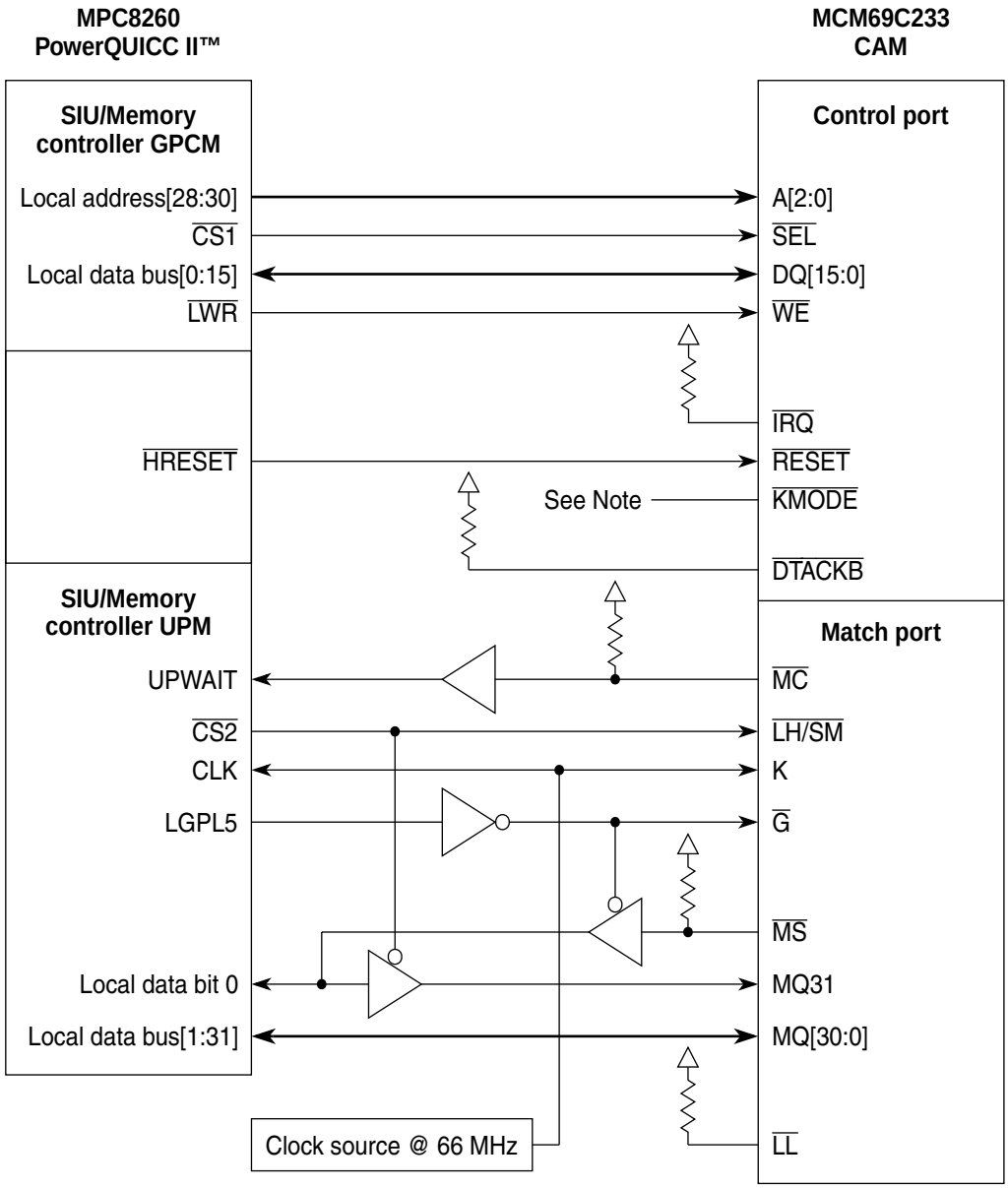
60x Bus	Local Bus	Comments
$\overline{CS}$[0-11]		Device select
PBS(0–7)	LBS(0–3)	Byte Select
PGPL_0	LGPL_0	General-purpose line 0
PGPL_1	LGPL_1	General-purpose line 1
PGPL_2	LGPL_2	General-purpose line 2
PGPL_3	LGPL_3	General-purpose line 3
PGPL_4/UPWAIT	LGPL_4/UPWAIT	General-purpose line 4/UPM WAIT
PGPL_5	LGPL_5	General-purpose line 5

From Table 2, UPM signals can be generated either on the 60x bus or the local bus. For this document, the MPC8260/CAM match port interfacing will take place on the local bus.

The UPM's $\overline{CS}$[2] and LGPL[5] signals are mapped to the CAM $\overline{LH/SM}$ and $\overline{G}$ signals, respectively. The UPM will be programmed to assert $\overline{CS}$[2] ($\overline{LH/SM}$) during write cycles and LGPL[5] ($\overline{G}$) during read cycles. The CAM $\overline{MC}$ signal (pulled up through a 1kΩ resistor) is mapped to the UPM LGPL_4/UPWAIT pin. During a write cycle on the CAM match port, $\overline{MC}$ deasserts and goes into a high state. This in turn, asserts the UPM UPWAIT signal (this is an active high signal). When UPWAIT is active, the current transaction is frozen until UPWAIT is deasserted (a low state); this occurs when the match algorithm completes and $\overline{MC}$ enters a low state. All match data written from the MPC8260 will be 32-bit operands; all return data from the CAM will be 32-bit operands. Thereby, the byte select signals (LBS[x]) will not be used. For applications such as Ethernet or ATM, the MPC8260 requires an indication if a match attempt was either successful or not successful. The MPC8260 checks the msb (LCL_D[0]) of the returned data. If the bit is cleared, the data is accepted. If the bit is set, the data is rejected. Therefore, the CAM $\overline{MS}$ signal (pulled high) will accommodate this requirement. The CAM $\overline{LL}$ (latch low) signal is needed if the match data

written to the CAM requires more than one 32-bit write transaction (for example, if the input match data were 48 bits wide, $\overline{LL}$ would latch in the lower 16 bits; then, $\overline{LHSM}$ would latch in the higher 32 bits). For purposes of this document, $\overline{LL}$ is pulled high and not used. The 32-bit CAM data bus, MQ[31:0], is mapped to the MPC8260 local data bus, LCL_D[0-31].

Figure 1 below gives an illustration of the MPC8260/CAM interface:



Note: Assert $\overline{KMODE}$ 1 clock cycle after $\overline{RESET}$ is deasserted.

Figure 1. MPC8260/CAM Interface

4 MPC8260 Register Programming

In order to utilize the MPC8260's GPCM and the UPM, two registers in the MPC8260 must be programmed: the base register and the option register. The base registers (BR0-BR11) hold information

such as the base address of the memory peripheral (the CAM), the memory attributes, and the selection of the machine handling the memory accesses. The option registers (OP0-OP11) define the size of the memory banks and other access attributes that are depending on the machine selected.

4.1 CAM Control Port Access

To select the GPCM to handle accesses to the CAM control port, the base and option registers (BR1 and OR1) should be programmed with the following attributes:

Table 3. Base Register (BR1)

Bits	Name	Description
0–16	BA	Sets the base address for the CAM's control port
17–18	-	Reserved, should be cleared
19–20	PS	Port Size- Since the CAM control port is 16 bits wide, these two bits should have a value of 10
21–22	DECC	Data error correction and checking- This feature will not be used. Thereby it is disabled with bit value 00
23	WP	Write Protect- Can be used for write protection within the address range of BR. For this application R/W capability is needed. This bit is set to 0
24–26	MS	Machine select- Since the GPCM on the local bus is used for the CAM control port, these bits are set to 001
27	EMEMC	External Memory Controller Enable- Allows overriding of the MS (bits 24-26). This feature will not be used, therefore set this bit to 0
28–29	ATOM	Atomic Operation- The ability to either perform a read after a write (set to 01) or a write after a read transaction (set to 10). For this application, this feature is not used on the control port. Set these bits to 00
30	DR	Data pipelining- This feature is not needed. Set this bit to 0
31	V	Valid bit- Activates the chip select. Set this bit to 1

Therefore, the value for BR1 = xxxx xxxx xxxx xxxx x001 0000 0010 0001 in this application.

Table 4. Option Register (OR1) GPCM Mode

Bits	Name	Description
0–16	AM	Address mask- Sets the size of the memory by selecting which bits will be used in address comparison. Set the memory size of the chip select to the 64 KB minimum by setting these bits to all ones
17–18	-	Reserved, should be cleared
19	BCTLD	Data buffer control disable- Disables assertion of BCTLx and $\overline{\text{LWR}}$. Since $\overline{\text{LWR}}$ is needed, set this bit to 0
20	CSNT	Chip select negation time- Determines when $\overline{\text{CS}}$/$\overline{\text{WE}}$ are negated during a write transaction. Set this bit to 0 for normal negation.
21–22	ACS	Address to chip select setup- Determines the timing when the chip select is asserted relative to address validation. For the control port, the assertion of the chip select will be one quarter of a clock after the address is valid. Thereby, set these bits to 10
23	-	Reserved, should be cleared

Table 4. Option Register (OR1) GPCM Mode (continued)

Bits	Name	Description
24–26	SCY	Cycle length in clocks- Determines the number of wait states inserted in the cycle during an access. This application will use five wait states (i.e., five additional clock cycles) Set these bits to 0101
27	SETA	External access termination- Write accesses will be terminated with the MPC8260 $\overline{\text{PSVAL}}$ assertion instead of an external signal (such as the CAM $\overline{\text{DTACK}}$). Therefore, set this bit to 0
28–29	TRLX	Timing relaxed- (Note: This bit is used in conjunction with bit 30) Determines if the timings of the generated signals will be normal or slowed. For the CAM control port, this feature is not needed. Set this bit to 0
30	ETHR	Extended hold time on read access- Along with bit 29, this indicates how many cycles are inserted between a read access from the current bank and the next access. Set this bit to 0. No additional cycles are needed
31	-	Reserved, should be cleared

OR1 = 1111 1111 1111 1111 1000 0100 0101 0000.

4.2 CAM Match Port Access

Let us now configure the registers for the match port. To select the UPM to handle accesses to the CAM match port, the base and option registers (BR2 and OR2) should be programmed with these attributes:

Table 5. Base Register (BR2)

Bits	Name	Description
0–16	BA	Sets the base address for the CAM match port
17–18	-	Reserved, should be cleared
19–20	PS	Port Size- Since the CAM control port is 32 bits wide, these two bits should have a value of 11
21–22	DECC	Data error correction and checking- This feature will not be used. Thereby it is disabled with bit value 00
23	WP	Write Protect- Can be used for write protection within the address range of BR. For this application R/W capability is needed. This bit is set to 0
24–26	MS	Machine select- Since the UPMA is used for the CAM match port, these bits are set to 100
27	EMEMC	External Memory Controller Enable- Allows overriding of the MS (bits 24-26). This feature will not be used, therefore set this bit to 0
28–29	ATOM	Atomic Operation- The ability to either perform a read after a write (set to 01) or a write after a read transaction (set to 10). For this application, a read after a write will be needed. Set these bits to 01
30	DR	Data pipelining- This feature is not needed. Set this bit to 0
31	V	Valid bit- Activates the chip select Set this bit to 1

From the above table, BR2 = yyyy yyyy yyyy yyyy y001 1000 1000 0101.

Table 6. Option Register (OR2) (UPM Mode)

Bits	Name	Description
0–16	AM	Address mask- Sets the size of the memory by selecting which bits will be used in address comparison. Set the memory size of the chip select to the 64 KB minimum by setting these bits to all ones
17–18	-	Reserved, should be cleared
19	BCTLD	Data buffer control disable- Disables assertion of BCTLx and LWR. This feature is not needed. Set this bit to 1
20–22	-	Reserved, should be cleared
23	BI	Burst Inhibit- Indicates if this bank supports bursting. The CAM does not support bursting. Set this bit to 1
24–28	-	Reserved, should be cleared
29-30	ETHR	Extended hold time on read access- This indicates how many cycles are inserted between a read access from the current bank and the next access. Set these bits to 00 for normal timing (no additional cycles will be added).
31	-	Reserved, should be cleared

OR2 = 1111 1111 1111 1111 1001 0001 0000 0000.

4.3 UPM RAM Array

The MPC8260 UPM signals are driven by the 64-bit words that are programmed into the internal memory RAM array. Each word in the array provides bits that allow a memory access to be controlled with a resolution of up to one quarter of the external bus clock period on the byte-select (BSx) and chip select (CSx) lines. These words also control the behavior of the general-purpose line (GPLx). In order to program these words in to the UPM RAM array, additional registers, the Machine A/B/C Mode register (MxMR) and the Memory Data register (MDR), must also be configured. The MxMR controls the execution of the UPM. The MDR contains data that is written to or read from the RAM array for WRITE or READ commands. Note that the MDR must be set up before issuing a write command to the UPM.

To write words into the UPM RAM array:

Table 7. Machine A Mode Register

Bits	Name	Description
0	BSEL	Bus select- Assigns banks using the UPM to the 60x or Local bus. Since the CAM is on the local bus, set this bit to 1
1	RFEN	Refresh enable- Allows refresh services. This will not be used, so set this bit to 0
2–3	OP	Command Opcode- To write words (to program) into the array, set these bits to 01. For normal operations, set these bits to 00
4	-	Reserved, should be cleared
5–7	AMx	Address Multiplex size- Address multiplexing is not used. Set these bits to 000

Table 7. Machine A Mode Register (continued)

Bits	Name	Description
8–9	DSx	Disable timer period- Ensures minimum time between accesses to the same bank controlled by the UPM. It is a way of guaranteeing that no interrupts will occur while a current UPM-controlled transaction is taking place. Only one cycle disable period is needed; so set these bits to 00Disable timer period- Ensures minimum time between accesses to the same bank controlled by the UPM. It is a way of guaranteeing that no interrupts will occur while a current UPM-controlled transaction is taking place. Only one cycle disable period is needed; so set these bits to 00
10–12	GOCLx	General 0 line control- Determines which address line can be output to the GPL0 pin. Set these bits to 000
13	GPL_x4 DIS	GPL_x4 (General Purpose Line 4) Disable- Determines if the UPWAIT/GTA/GPL_4 pin behaves as an output line controlled by bits in the UPM array. Set this bit to 1
14–17	RLFx	Read Loop Field- Set these bits to 0000
18–21	WLFx	Write Loop Field- Set these bits to 0000
22–25	TLFx	Refresh Loop Field- Set these bits to 0000
26–31	MAD	Machine address- Depending on the function performed (Write or Read), this is the address within the RAM array that performs a particular function

Therefore, the value for MxMR (for this application, MAMR):

MAMR = 1001 0000 0000 0100 0000 0000 00xx xxxx where “xx xxxx” is the Machine Address.

After the MAMR is set (with the OP field set to 01), RAM words need to be programmed into the RAM array. Only single-beat read and single-beat write patterns are used. Burst, refresh, and exception patterns are not used.

For the 66 MHz bus, the following UPM RAM words should be programmed:

Single-beat reads-

FFFFDC00
FFFFDC00
FFFFC805

Single-beat write-

0FFFC000
FFFFC005

Each time a word is written into the RAM array, the MAD (bits 26-31 of the MxMR) automatically increments. For the above UPM RAM single-beat read patterns, the MxMR will only need to be configured once with the MAD bits set to the address of the first single-beat read (0x00)—the subsequent patterns will be written in consecutive Single-beat read address locations. However, the MxMR will need to be reconfigured for the different MAD pertaining to the first single-beat write pattern (0x18).

4.4 CAM Register Configuration

There are three types of registers accessible through the CAM control port: the I/O registers, the operation register, and the results/condition code registers. Each register is 16 bits in length. Data is written into the I/O registers followed by a command code written into the operation register. The results/condition registers alert the user when certain conditions occur or the user may set interrupts when certain conditions occur.

Before basic operations of the CAM can begin, there are some start-up functions that must be performed. First the match width and output width must be determined by issuing the SET GLOBAL MASK REGISTER command. The input bits to be compared are defined by this register. The convention of this mask register is opposite that of typical mask registers; bits that are 0 are used for matching while bits that 1 are used for masking. Typically, bits that are used for matching are the higher-order bits of the 64-bit CAM table entries, while the output bits are the lower-order bits.

The mode of data entry is the next start-up function. The buffered-entry mode utilizes the entry queue while fast-entry mode bypasses the entry queue and enters data directly into the CAM table. If the fast-entry mode is used, the INITIALIZE TABLE command must be executed before matching operations can begin. In a typical application, the fast-entry mode is used at start-up to load initial data into the CAM table, followed by the INITIALIZE TABLE command. Then, the buffered-entry mode is used for normal operation.

After the start-up functions are completed, the CAM table can be loaded. Each 64-bit data entry is constructed by writing a 16-bit value into each of the four I/O registers and issuing the INSERT VALUE command. After the INITIALIZE TABLE command is executed (if required), normal matching can begin. The DELETE VALUE command can be used to remove data from the CAM table.

The flag register gives the status of various states of operation. If an error occurs, one of several error codes appears in the error code register. Although in this document the CAM interrupt ($\overline{IRQ}$) signal is not used, several conditions can be programmed into the interrupt register to assert the CAM $\overline{IRQ}$ signal.

4.5 Transaction Timing Diagrams

Figures 2 through 5 below are timing diagrams of the 8260/CAM interface at 66 MHz. Results were derived via Verilog simulation of the MPC8260 SWIFT Model - Solaris: Rev. B.0 Bus Function Model (available on Motorola's MPC8260 Product Summary website) and the MPC69C233 HDL CAM model. Write and read transaction via the CAM control and match port are shown.

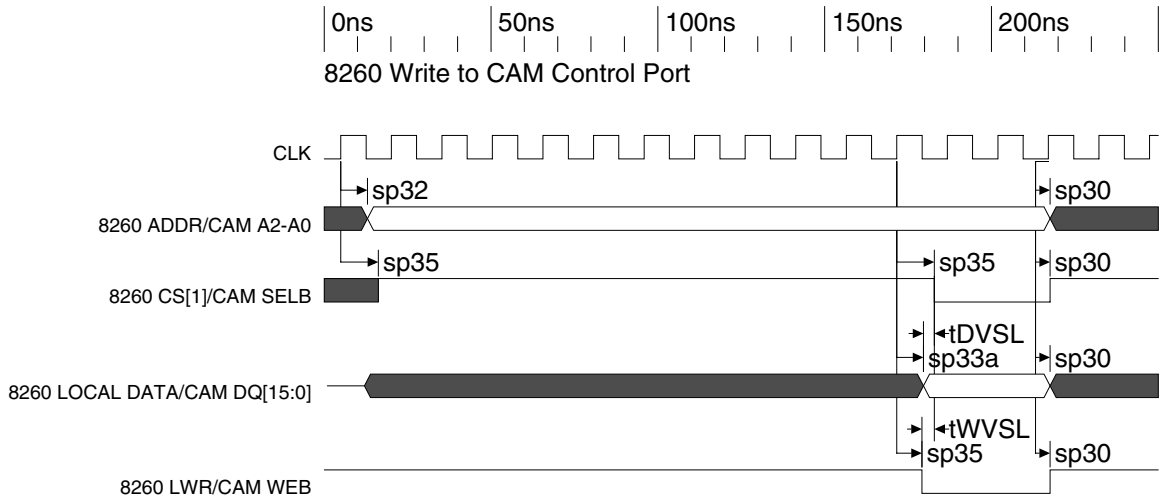


Figure 2. PowerQUICC II ™ Write Cycle (CAM Control Port Read)

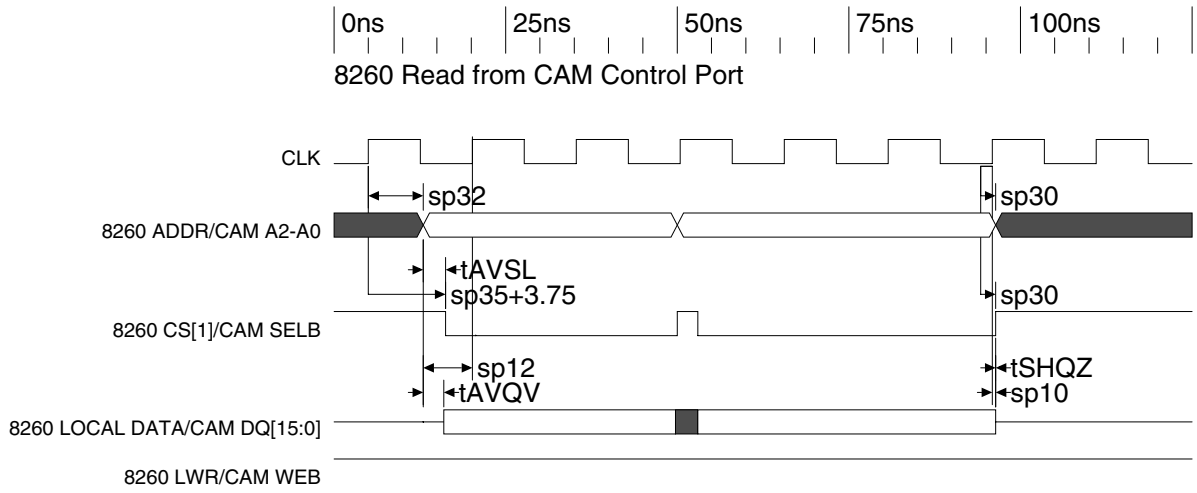


Figure 3. PowerQUICC II ™ Read Cycle (CAM Control Port Write)

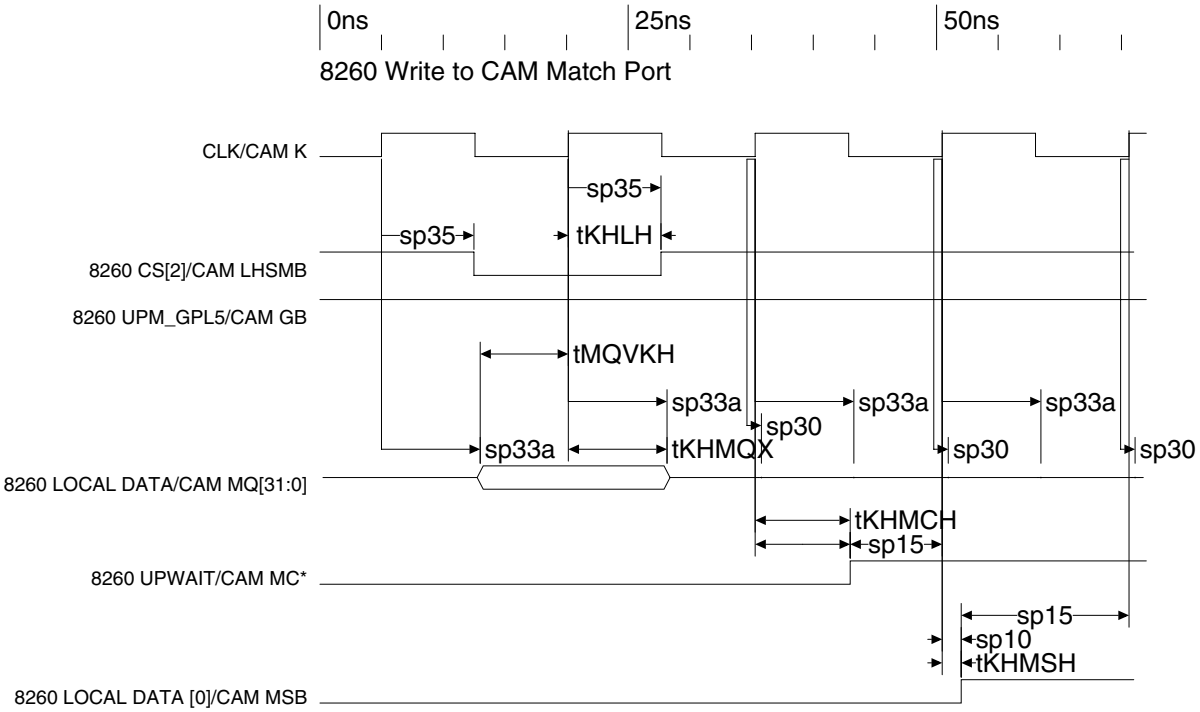


Figure 4. PowerQUICC II ™ Write Cycle (CAM Match Port Read)

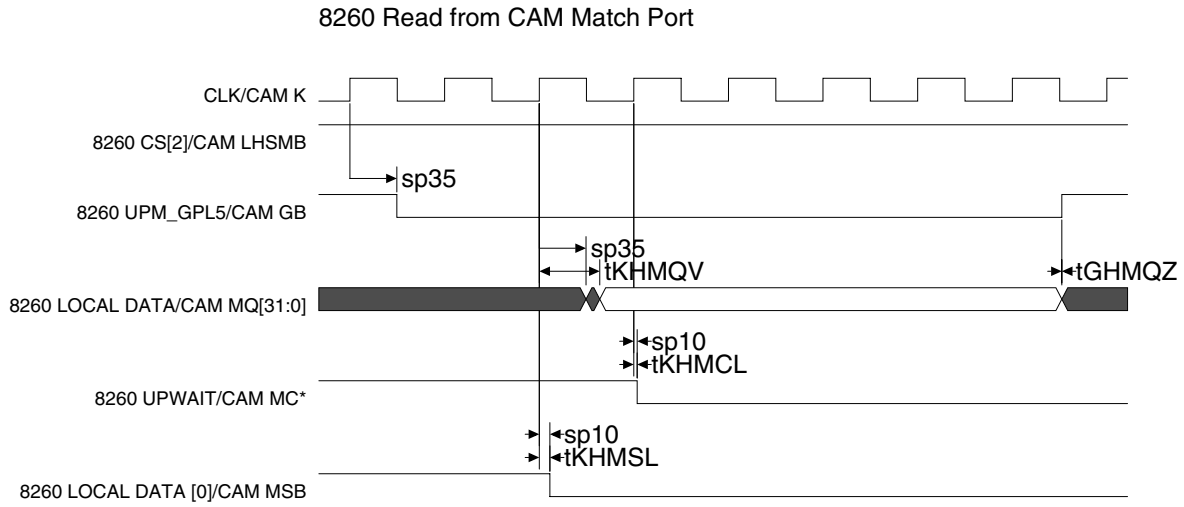


Figure 5. PowerQUICC II ™ Read Cycle (CAM Match Port Write)

5 References

MPC8260 PowerQUICC II™ User's Manual (**MPC8260UM/D Rev. 0 Chapter 10—Memory Controller** available on Motorola's MPC8260 Product Summary website)

MCM69C233 CAM data sheet (Available on Motorola's Content Addressable Memory [CAM] Product Summary website)

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