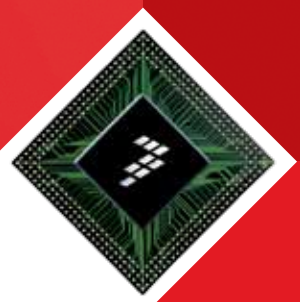

Integrated Flash Controller

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1 Introduction

The past few years have witnessed explosive growth in the flash memory market, driven by the use of wireless communication devices, networking and communication products, security systems and other types of electronic equipment (PDAs, digital cameras, MP3 audio players). In the next few years, system designs will demand even more non-volatile memories, either with high density and very high writing throughput for data storage applications or with fast random access for code execution. The flexibility and low cost of flash memory makes it a frequently utilized, well-consolidated and mature technology for most non-volatile memory applications.

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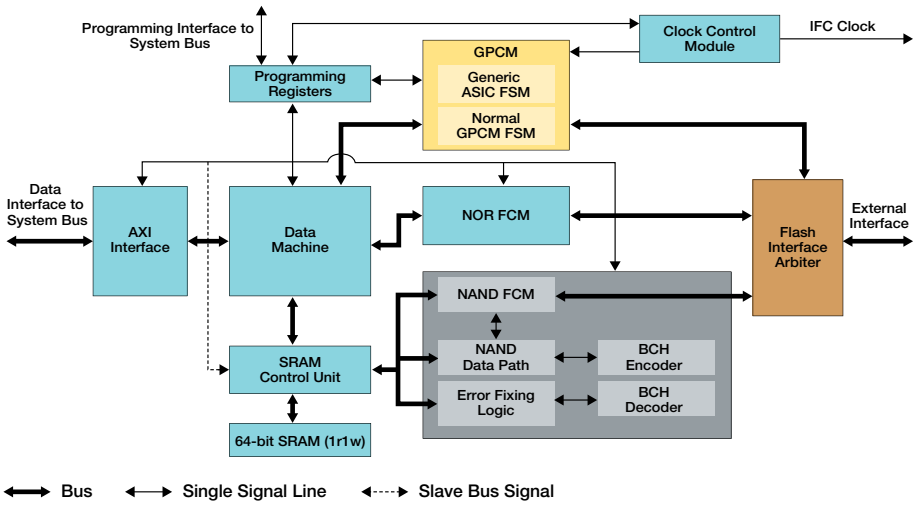

Today, almost every system design uses external memory, since embedded memories can be costly in terms of price and power consumption. As a result, implementing a memory controller that can manage multiple memory types is now an essential differentiator in the processor market.

The QorIQ P1010 and P1014 processors introduce the new integrated flash controller (IFC), an advanced version of the enhanced local bus controller which includes similar programming and signal interfaces with an extended feature set. The IFC provides access to multiple external memory types, such as NAND flash (SLC and MLC), NOR flash, EPROM, SRAM and other memories where address and data are shared on a bus. These memory controllers offer the system an alternate option and cover a wide range of applications, from networking and communications to consumer and automotive.

Drivers for an Integrated Flash Controller

- Market trend toward NAND with larger page sizes
- Increase in flash density with more ECC bits per page
- Command set enhancements
- Emergence of Open NAND Flash Interface (ONFI) standard
- High-speed NAND flash devices using source synchronous DDR mode

2 Overview

The IFC on the P1010 processor family contains one NAND, one NOR flash controller and one general-purpose chip-select machine (GPCM) controller. It can be programmed such that all four memory banks, each with addressable system memory of 4 GB, can work with NAND, NOR and a GPCM controller depending on the requirement. The IFC can be configured to interface to a NOR or NAND flash device on any bank. In addition, the IFC contains a GPCM that can be used as a synchronous interface to a variety of devices, including external PHYs, ASICs or FPGAs.

Four chip selects, with common address, data and control bus, are provided in IFC so that a maximum of four flash devices can be connected, but only one can be accessed at a given time. Pin muxing is done internally based on a selected controller (NAND, NOR or GPCM).

The NAND flash controller supports the ONFI 2.0 asynchronous interface and provides an 8- or 16-bit flash memory interface. The controller offers a Bose, Chaudhuri and Hocquenghem (BCH) algorithm for 4- and 8-bit error-correcting code (ECC) for optimized performance and reliability. In addition, the IFC supports boot from NAND flash devices, multiple page sizes (up to 4 KB) and multi-terabyte flash devices.

The NOR flash controller offers compatibility with asynchronous NOR flash (synchronous burst read not supported) and flexibility in timing control that allows interfacing with proprietary NOR devices. Boot from NOR flash devices is also available. Additionally, the GPCM offers the possibility to interface with a multitude of devices, including external PHYs, ASICs or FPGAs. The GPCM provides support for x8/16-bit devices, compatibility with general-purpose addressable devices (SRAM and ROM) and an external access termination signal (IFCTA).

QorIQ P1010/P1014 processors deliver unique product differentiators and can be configured to meet many system application needs. Freescale's innovative IFC technology is a key design component for the future of QorIQ processor platforms. It provides the flexibility needed for emerging applications that require interfacing with a variety external memories, as well as the ability to support large page mainstream flash memories.

Integrated Flash Controller Features

NAND Flash Features	NOR Flash Features	GPCM Features	GASIC Features

• x8/x16 NAND flash interface
• Support for ONFI-2.0 asynchronous interface (8/16-bit)
• BCH code for 4-bit and 8-bit error correction per sector
• ECC generation/checking optional
• Flexible timing control to allow interfacing with proprietary NAND devices
• SLC and MLC flash devices support with configurable page sizes of up to 4 KB
• Support for advanced NAND commands (cache, copy-back and multi-plane programming)
• Programmable command and data transfer sequences up to 15 steps
• Configurable block size constraint to multiples of 32 pages, up to 2048
• Interrupt for error handling and flash command completion event
• Internal SRAM of 16 KB
• Boot chip-select (CS0) available after system reset, with boot block size of 8 KB, for execute-in-place boot loading from NAND flash
• Flash devices with multiple terabytes of storage
	• Supports asynchronous NOR flash
	• Provides memory mapped interfacing to NOR
	• Supports address data multiplexed (ADM) NOR device
	• Flexible timing control allows interfacing with proprietary NOR devices (write enable controlled writes only)
	• Boot chip-select (CS0) available at system reset
	• Data bus width of 8/16 bits
		• Support for x8/16-bit devices
		• Compatible with general-purpose addressable devices (SRAM and ROM)
		• External clock is supported by programmable division ratios
		• Output enable signal
		• Write enable signal
		• Even/odd parity on data bus supported
		• External access termination signal (IFCTA)
			• Support for 16/8-bit devices where address and data sequences are shared on the same bus
			• The following address and data sequences are supported on I/O bus:
			  ○ 16-bit I/O: AADD
			  ○ 8-bit I/O: AAAADDDD
			• Configurable even/odd parity on address/data bus supported
			• Parity error detection supported

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