UM11802

RDGD3162I3PH5EVB three-phase inverter reference design

Rev. 3 — 27 August 2024 User manual

Document information

Information	Content
Keywords	GD3162, gate, driver, power, inverter, automotive
Abstract	The RDGD3162I3PH5EVB three-phase inverter is a functional hardware power inverter reference design, which can be used as a foundation to develop a complete ASIL D compliant high voltage, high-power traction motor inverter for electric vehicles.

1 Important notice

IMPORTANT NOTICE

For engineering development or evaluation purposes only

NXP provides the product under the following conditions:

This evaluation kit or reference design is for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY.

It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This evaluation kit or reference design may be used with any development system or other source of I/O signals by connecting it to the host MCU or computer board via off-the-shelf cables. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

The product provided may not be complete in terms of required design, marketing, and or manufacturing related protective considerations, including product safety measures typically found in the end device incorporating the product. Due to the open construction of the product, it is the responsibility of the user to take all appropriate precautions for electric discharge. To minimize risks associated with the customers' applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards. For any safety concerns, contact NXP sales and technical support services.

2 RDGD3162I3PH5EVB

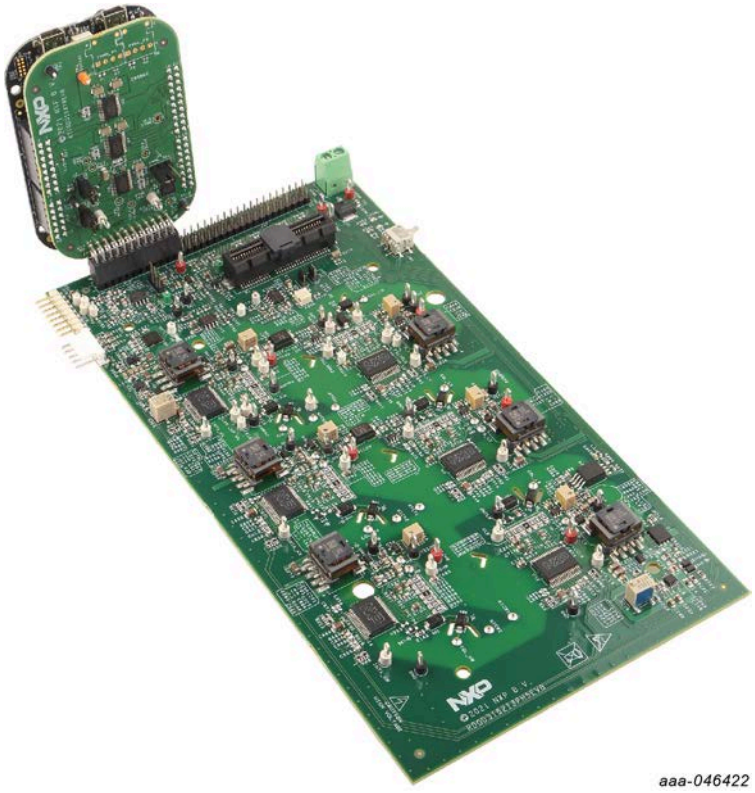


Figure 1. RDGD3162I3PH5EVB

3 Introduction

This document is the user guide for the RDGD3162I3PH5EVB reference design. This document is intended for the engineers involved in the evaluation, design, implementation, and validation of the GD3162 single-channel gate driver for insulated gate bipolar transistor (IGBT)/SiC.

The scope of this document is to provide the user with information to evaluate the GD3162 single channel gate driver for IGBT/SiC. This document covers connecting the hardware, installing the software and tools, configuring the environment and using the kit.

The RDGD3162I3PH5EVB is a fully functional three-phase inverter evaluation board populated with six GD3162 gate drivers with fault management and supporting circuitry. This board supports serial peripheral interface (SPI) daisy chain communication for programming and communication with three high-side gate drivers and three low-side gate drivers independently, or all six gate drivers at the same time.

This board has low-voltage isolation and high-voltage isolation with gate drive integrated galvanic signal isolation. Other supporting features on the board include desaturation short-circuit detection, IGBT/SiC temperature sensing, onboard isolated flyback supplies, DC link bus voltage monitoring, phase current sensing, DC link bus current sense, and motor resolver excitation/processing. See GD3162 data sheet for additional gate drive features.

4 Finding kit resources and information on the NXP website

NXP Semiconductors provides online resources for this reference design and its supported devices on http://www.nxp.com.

The information page for RDGD3162I3PH5EVB reference design is at http://www.nxp.com/RDGD3162I3PH5EVB. The information page provides overview information, documentation, software and tools, parametrics, ordering information and a **Getting Started** tab. The **Getting Started** tab provides quick reference information applicable to using the RDGD3162I3PH5EVB reference design, including the downloadable assets referenced in this document.

4.1 Collaborate in the NXP community

The NXP community is for sharing ideas and tips, ask and answer technical questions, and receive input on just about any embedded design topic.

The NXP community is at http://community.nxp.com.

5 Getting ready

Working with the RDGD3162I3PH5EVB requires kit contents and a Windows PC workstation with FlexGUI 2 software installed.

5.1 Kit contents

- Assembled and tested RDGD3162I3PH5EVB (three-phase inverter populated with 5.0 V compatible gate driver devices) board in an antistatic bag
- KITGD316xTREVB 3.3 V to 5.0 V translator with FRDM-KL25Z MCU board with micro-USB cable
- Quick start guide

5.2 Additional hardware

In addition to the kit contents, the following hardware is necessary or beneficial when working with this reference board.

- Microcontroller for SPI communication
- Compatible P6 IGBT or SiC metal-oxide-semiconductor field-effect transistor (MOSFET) module
- DC link capacitor compatible with HybridPACK Drive or P6 IGBT or SiC MOSFET module
- HV power supply with protection shield and hearing protection
- Current sensors for monitoring each phase current
- 12 V, 1.0 A DC power supply
- 4-channel oscilloscope with appropriate isolated probes

5.3 Windows PC workstation

This reference design requires a Windows PC workstation. Meeting these minimum specifications produces great results when working with this evaluation board.

- USB-enabled computer with Windows 10 or higher operating system

5.4 Software

Installing software is necessary to work with this reference design. All listed software is available on the information page at http://www.nxp.com/RDGD3162I3PH5EVB.

- FlexGUI 2 software for using with KITGD316xTREVB MCU/translator board
- S32S Design Studio IDE for power architecture
- Automotive Math and Motor Control Library (AMMCLib)
- FreeMASTER 2.0 runtime debugging tool
- Motor control application tuning (MCAT)
- Example code, GD3162 device driver notes, and GD31xx device driver reference

6 Getting to know the hardware

6.1 RDGD3162I3PH5EVB features

- Capability to perform double pulse and short-circuit tests on phase U using KITGD316xTREVB and FlexGUI 2; see phase U schematics and FlexGUI 2 pulse tab (Figure 29 and Figure 31)
- Evaluation board designed for and populated with GD3162 gate drivers and protection circuitry
- Capability to connect to HybridPACK Drive type SiC specific modules for full three-phase evaluation and development (see Figure 9 for specific module pin placement)
- Daisy chain SPI communication × 3 - 2 channel (three high-side gate drivers and three low-side gate drivers) or × 6 - 1 channel (all six gate drivers)
- Variable flyback VCC power supply with GND reference and variable negative VEE supply
- Easy access power, ground, and signal test points
- 2 × 32 peripheral component interconnect express (PCIe) socket for interfacing MCU control (MPC5775B/E-EVB, MPC5777C-DEVB, or MPC57744P); see Figure 32 and Figure 33
- Optional connection for DC bus voltage and current monitoring
- Phase current feedback connections
- Resolver signal connector

6.2 Kit featured components

6.2.1 Voltage domains, GD3162 pinout, logic header, and IGBT pinout

Low-voltage domain is an externally supplied 12 V DC (VPWR) primary supply for non-isolated circuits, typically supplied by vehicle battery. A 5 V regulator supplies VDD to GD3162 gate drive devices. The low-voltage domain includes the interface between the MCU and GD3162 control registers and logic control.

Low-side driver and high-side driver domains are isolated high-voltage driver control domains for SiC MOSFET or IGBT single phase connections and control circuits. Pins on the bottom of the board are designed to connect easily to a compatible three-phase SiC MOSFET or IGBT module.

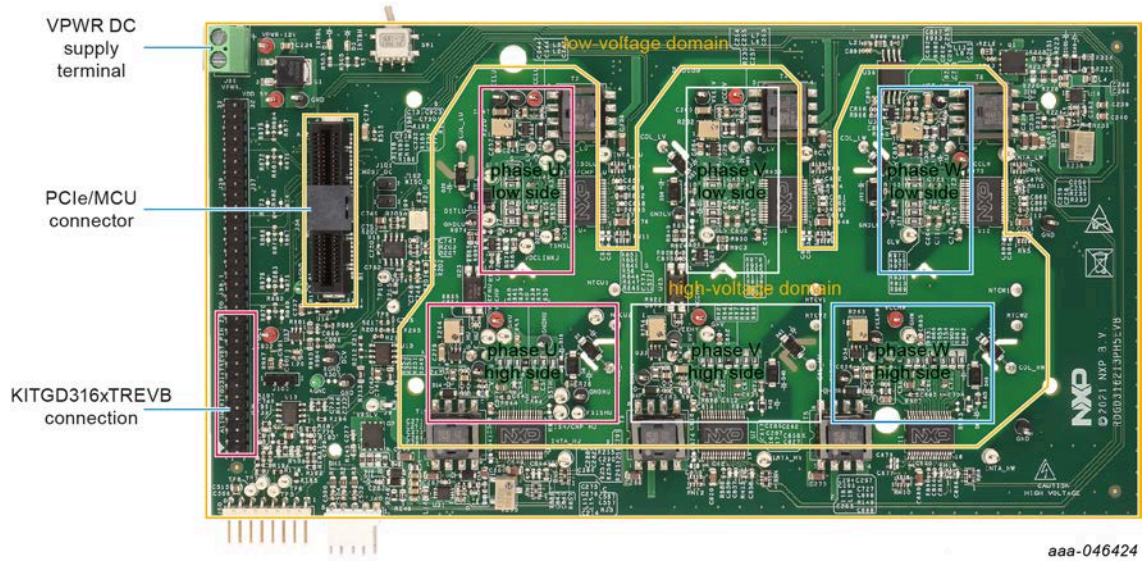


Figure 2. RDGD3162I3PH5EVB three-phase inverter board voltage domains and interfaces

6.2.2 GD3162 pinout and MCU interface pinout

See GD3162 advanced IGBT/SiC gate driver data sheet for specific information about pinout, pin descriptions, specifications, and operating modes. VSUP/VPWR DC supply terminal is a low-voltage input connection for supplying power to the low-voltage non-isolated die and related circuitry. Typically supplied by vehicle battery +12 V DC.

MCU connector is a 2 × 32-pin PCIe interface connector for use with either MPC5775B/E-EVB or MPC5744P or MPC5777C 32-bit MCU board or any other MCU of preference. An MCU is needed for SPI communication and control of advanced IGBT/SiC gate drive devices (GD3162).

KITGD316xTREVB included with the kit can be attached to this board at the bottom of the dual row connector. All gate drivers can be accessed via SPI control using FlexGUI 2 software.

Note: *Double pulse and short-circuit tests can be conducted on phase U only. See FlexGUI 2 pulse tab Figure 29 and Figure 31.*

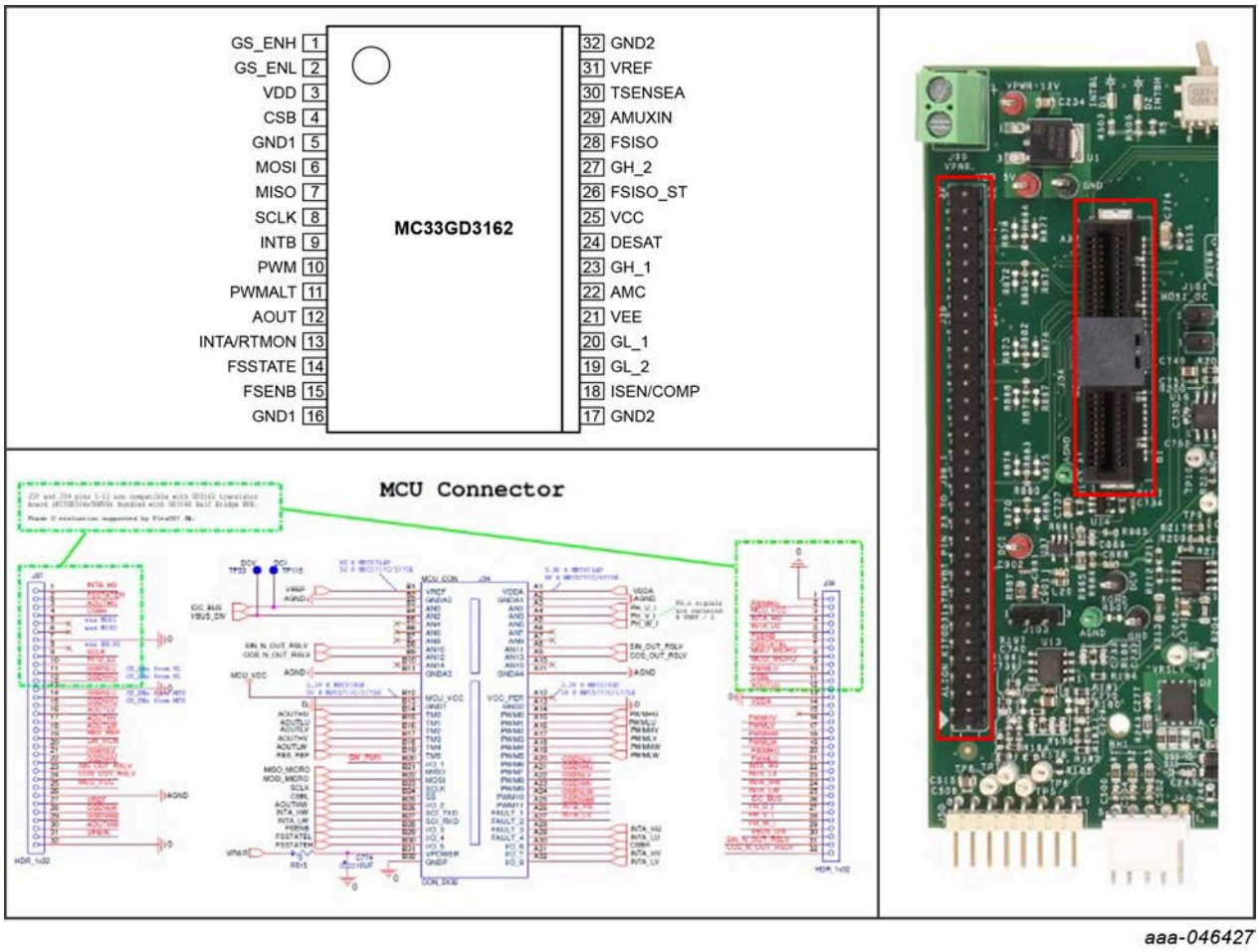


Figure 3. Gate driver pinout and board interface connection PCIe 2 × 32

Table 1. PCIe connector pin definitions

Pin	Name	Function
A1	VDDA	voltage reference resolver circuit
A2	GNDA1	analog ground
A3	PH_U_I	current feedback phase U
A4	PH_V_I	current feedback phase V
A5	PH_W_I	current feedback phase W
A6	n.c.	not connected
A7	n.c.	not connected
A8	SIN_OUT_RSLV	sine resolver signal
A9	COS_OUT_RSLV	cosine resolver signal
A10	n.c.	not connected
A11	GNDA4	analog ground
A12	VCC_PER	5.0 V MCU not connected

Table 1. PCIe connector pin definitions...*continued*

Pin	Name	Function
A13	GND2	ground
A14	PWMHU	pulse width modulation (PWM) high-side phase U
A15	PWMLU	pulse width modulation low-side phase U
A16	PWMHV	pulse width modulation high-side phase V
A17	PWMLV	pulse width modulation low-side phase V
A18	PWMHW	pulse width modulation high-side phase W
A19	PWMLW	pulse width modulation low-side phase W
A20	GSENLU	GD3162 gate strength enable low-side phase U
A21	GSENHU	GD3162 gate strength enable high-side phase U
A22	GSENLV	GD3162 gate strength enable low-side phase V
A23	GSENHV	GD3162 gate strength enable high-side phase V
A24	GSENLW	GD3162 gate strength enable low-side phase W
A25	GSENHW	GD3162 gate strength enable high-side phase W
A26	INTB_HS	GD3162 fault reporting for high-side gate drive devices
A27	INTB_LS	GD3162 fault reporting for low-side gate drive devices
A28	INTA_HU	GD3162 fault reporting and real-time monitoring high-side phase U
A29	INTA_LU	GD3162 fault reporting and real-time monitoring low-side phase U
A30	CSBH	chip select bar to high gate drive devices
A31	INTA_HV	GD3162 fault reporting and real-time monitoring high-side phase V
A32	INTA_LV	GD3162 fault reporting and real-time monitoring low-side phase V
B1	VREF	voltage reference from MCU
B2	GNDA2	analog ground
B3	IDC_BUS	optional DC bus current measurement from DC bus current filter
B4	VBUS_DIV	optional DC bus voltage divider monitoring (not used by default)
B5	n.c.	not connected
B6	n.c.	not connected
B7	n.c.	not connected
B8	SIN_N_OUT_RSLV	sine resolver signal
B9	COS_N_OUT_RSLV	cosine resolver signal
B10	n.c.	not connected
B11	GNDA3	analog ground
B12	MCU_VCC	MCU VCC regulator voltage
B13	GND1	ground
B14	AOUTHU	GD3162 analog output signal high-side U phase
B15	AOUTLU	GD3162 analog output signal low-side U phase
B16	AOUTLV	GD3162 analog output signal low-side V phase

Table 1. PCIe connector pin definitions*...continued*

Pin	Name	Function
B17	AOUTHV	GD3162 analog output signal high-side V phase
B18	AOUTLW	GD3162 analog output signal low-side W phase
B19	RES_REF	resolver reference voltage
B20	SW_RUN	signal from onboard switch demo mode
B21	MISO_MICRO	SPI slave out signal
B22	MOSI_MICRO	SPI slave in signal
B23	SCLK	SPI clock
B24	CSBL	chip select bar to low-side gate drivers
B25	AOUTHW	GD3162 analog output signal high-side W phase
B26	INTA_HW	GD3162 fault reporting and real-time monitoring high-side phase W
B27	INTA_LW	GD3162 fault reporting and real-time monitoring low-side phase W
B28	FSENB	fail-safe state enable bar
B29	FSSTATEL	fail-safe state low-side
B30	FSSTATEH	fail-safe state high-side
B31	VPWR	VPWR/VSUP 12 V voltage supply (low-voltage domain)
B32	GNDP	ground connection (low-voltage domain)

6.2.3 Test points

All test points are clearly marked on the board. Figure 4 shows the location of various test points.

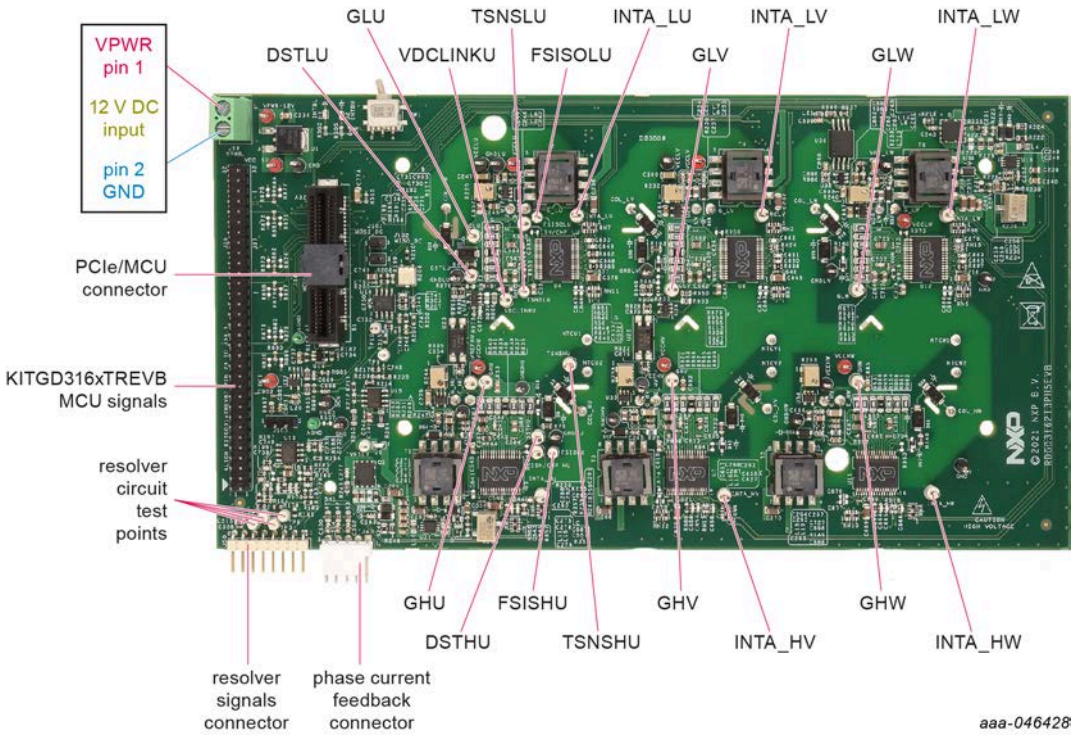


Figure 4. RDGD3162I3PH5EVB test points

Table 2. Test points

Test point name	Function
DSTHU	DESAT high-side U phase V_{CE} desaturation connected to DESAT pin circuitry
DSTHV	DESAT high-side V phase V_{CE} desaturation connected to DESAT pin circuitry
DSTHW	DESAT high-side W phase V_{CE} desaturation connected to DESAT pin circuitry
DSTLU	DESAT low-side U phase V_{CE} desaturation connected to DESAT pin circuitry
DSTLV	DESAT low-side V phase V_{CE} desaturation connected to DESAT pin circuitry
DSTLW	DESAT low-side W phase V_{CE} desaturation connected to DESAT pin circuitry
FSISHU	FSISO connection high-side U phase
FSISHV	FSISO connection high-side V phase
FSISLU	FSISO connection low-side U phase
FSISLV	FSISO connection low-side V phase
FSISLW	FSISO connection low-side W phase
GHU	gate high-side U phase, which is the charging pin of IGBT gate
GHV	gate high-side V phase, which is the charging pin of IGBT gate
GHW	gate high-side W phase, which is the charging pin of IGBT gate

Table 2. Test points*...continued*

Test point name	Function
GLU	gate low-side U phase, which is the charging pin of IGBT gate
GLV	gate low-side V phase, which is the charging pin of IGBT gate
GLW	gate low-side W phase, which is the charging pin of IGBT gate
INTA – UVW HS and LS	INTA interrupt/real-time reporting output signal test points from each gate driver
Resolver circuit	test points for internal signals of resolver circuit (see schematic for more information)
MCU signals	signal headers for analyzing all MCU signals (see schematic for signals)
TSNSHU	TSENSE high-side U phase connected to negative temperature coefficient (NTC) temperature sense
TSNSLU	TSENSE low-side U phase
VREFLU	5.0 V reference voltage test point low-side U phase
VREFHU	5.0 V reference voltage test point high-side U phase
VREFLV	5.0 V reference voltage test point low-side V phase
VREFHV	5.0 V reference voltage test point high-side V phase
VREFLW	5.0 V reference voltage test point low-side W phase
VREFHW	5.0 V reference voltage test point high-side W phase
VSUP	VSUP/VPWR test point low-voltage domain

6.2.4 Indicators

The RDGD3162I3PH5EVB contains LEDs as visual indicators on the board.

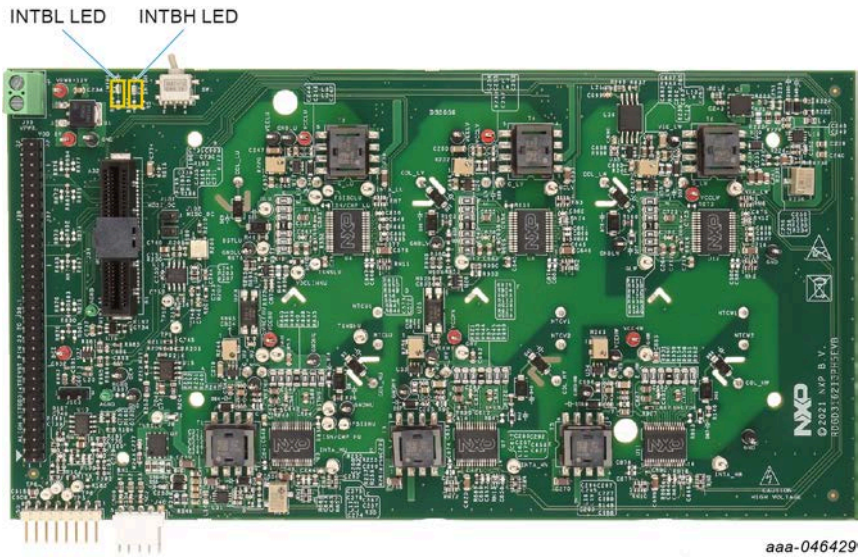


Figure 5. RDGD3162I3PH5EVB indicator locations

Table 3. RDGD3162I3PH5EVB indicator descriptions

Name	Description
INTBL LED	indicates that a GD3162 INTB fault interrupt has occurred on the low side
INTBH LED	indicates that a GD3162 INTB fault interrupt has occurred on the high side

6.2.5 Connectors and jumpers

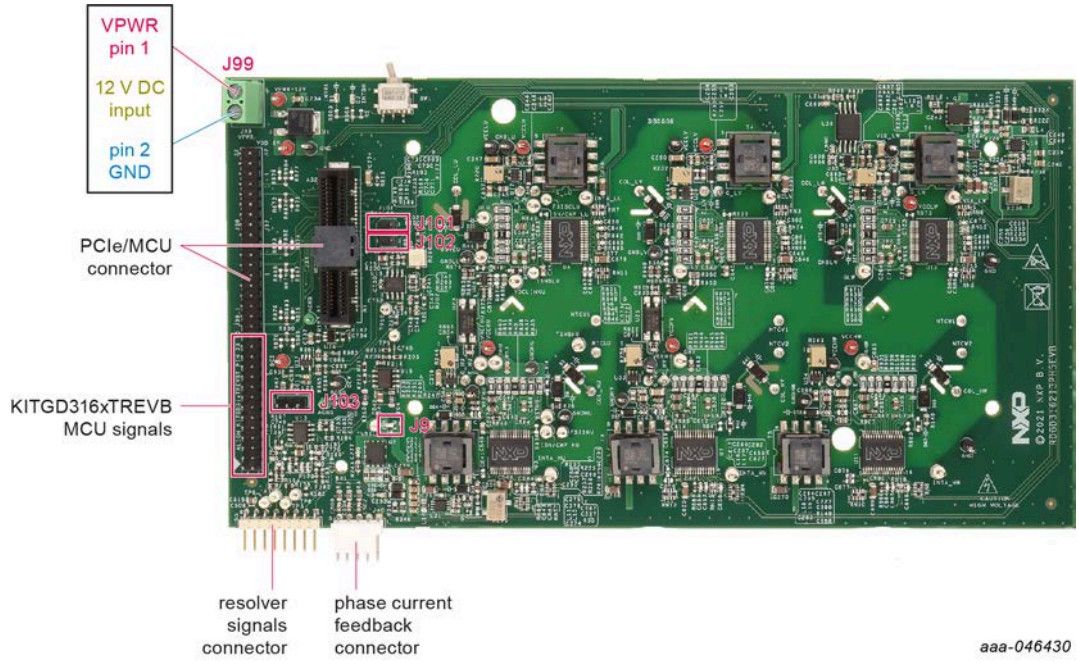


Figure 6. RDGD3162I3PH5EVB connector and jumper locations

Table 4. RDGD3162I3PH5EVB connector and jumper descriptions

Name	Description
J9	solder jumper 1-2 default - DC supply for VSUP to gate drivers supplied through J99 terminal connection jumper open VSUP supply to gate drivers isolated
J101	jumper 1-2 default master output slave input (MOSI) - normal mode three device daisy chain three device high side, three device low side (× 3 - 2 channel) jumper 2-3 MOSI - six device daisy chain all six gate drivers daisy chained together (× 6 - 1 channel)
J102	jumper 1-2 default master input slave output (MISO) - normal mode three device daisy chain three device high side, three device low side (× 3 - 2 channel) jumper 2-3 MISO - six device daisy chain all six gate drivers daisy chained together (× 6 - 1 channel)
J103	DC bus current measurement connection header
Phase current feedback connector	current feedback connections from U, V, and W phases
Resolver signals connector	resolver excitation signals (see schematic for more information)
MCU signals	two-row header of all MCU signals for debug and development (see schematic for details)
PCIe/MCU connector	2 × 32 PCIe connector for easy connection to MPC5777CDEVB or MPC5744P via PCIe cable (S32SDEV-CON18)
J99 VPWR terminal connector	used for external low-voltage power supply connection, typically 12 V V_{BAT}

6.2.6 Power supply test points

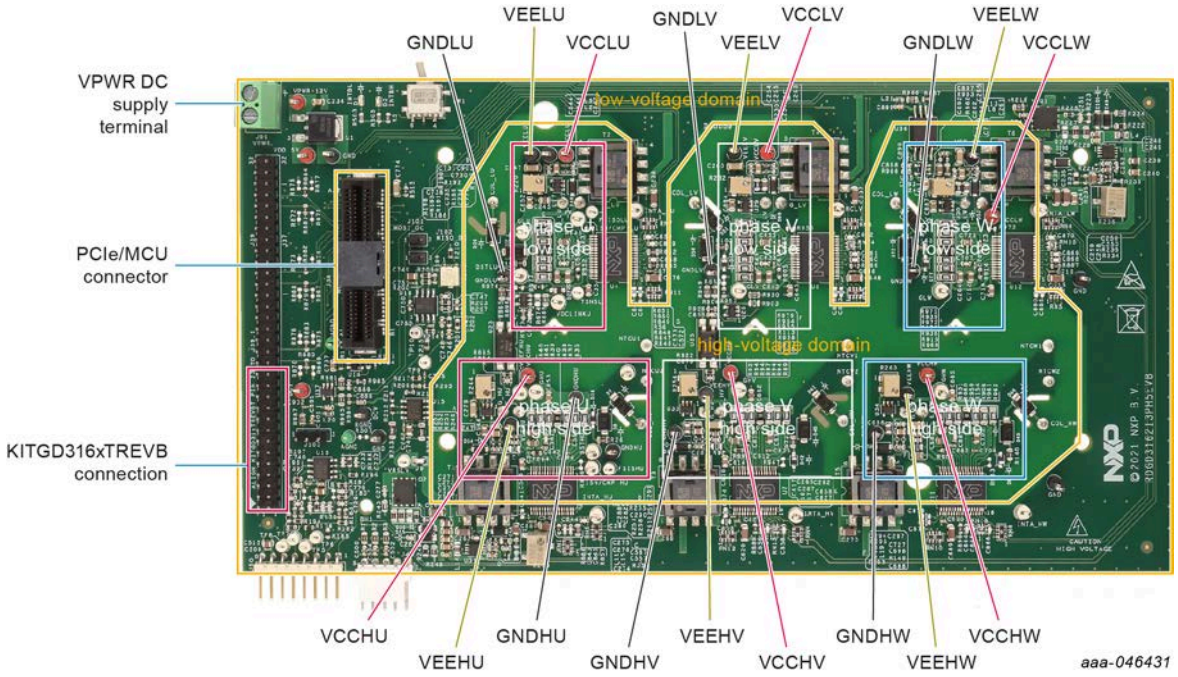


Figure 7. Power supply test point locations

Table 5. Power supply test point descriptions

Name	Function
VCCHU	high-side phase U VCC voltage test point isolated positive voltage supply (9.3 V to 25 V)
GNDHU	isolated ground high-side phase U
VEEHU	negative gate supply voltage high-side phase U
VCCHV	high-side phase V VCC voltage test point isolated positive voltage supply (9.3 V to 25 V)
GNDHV	isolated ground high-side phase V
VEEHV	negative gate supply voltage high-side phase V
VCCHW	high-side phase W VCC voltage test point isolated positive voltage supply (9.3 V to 25 V)
GNDHW	isolated ground high-side phase W
VEEHW	negative gate supply voltage high-side phase W
VCCLU	low-side phase U VCC voltage test point isolated positive voltage supply (9.3 V to 25 V)
GNDLU	isolated ground low-side phase U
VEELU	negative gate supply voltage low-side phase U
VCCLV	low-side phase V VCC voltage test point isolated positive voltage supply (9.3 V to 25 V)

Table 5. Power supply test point descriptions...*continued*

Name	Function
GNDLV	isolated ground low-side phase V
VEELV	negative gate supply voltage low-side phase V
VCCLW	low-side phase W VCC voltage test point isolated positive voltage supply (9.3 V to 25 V)
GNDLW	isolated ground low-side phase W
VEELW	negative gate supply voltage low-side phase W
VPWR	+12 V DC VPWR low voltage positive supply connection
VPWR GND	VPWR low voltage supply ground connection (GND1)

6.2.7 Gate drive resistors

- RGH_1 - gate high resistor in series with the GH_1 pin at the output of the GD3162 high-side driver and IGBT/SiC gate that controls the strong turn on current for IGBT/SiC gate.
- RGH_2 - gate high resistor in series with the GH_2 pin at the output of the GD3162 high-side driver and IGBT/SiC gate that controls the weak turn on current for IGBT/SiC gate.
- RGL_1 - gate low resistor in series with the GL_1 pin at the output of the GD3162 low-side driver and IGBT/SiC gate that controls the strong turn off current for IGBT/SiC gate.
- RGL_2 - gate low resistor in series with the GL_2 pin at the output of the GD3162 low-side driver and IGBT/SiC gate that controls the weak turn off current for IGBT/SiC gate.
- RAMC - series resistor between IGBT/SiC gate and active Miller clamp (AMC) input pin of the GD3162 high-side/low-side driver for gate sensing and active Miller clamping.

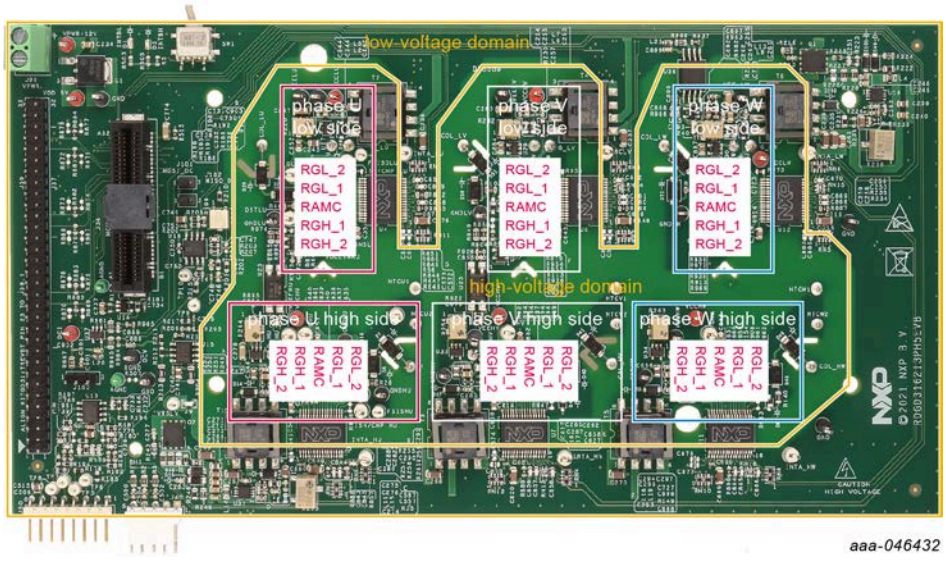


Figure 8. Gate drive resistors for each phase high side and low side

6.2.8 SiC module pin connections

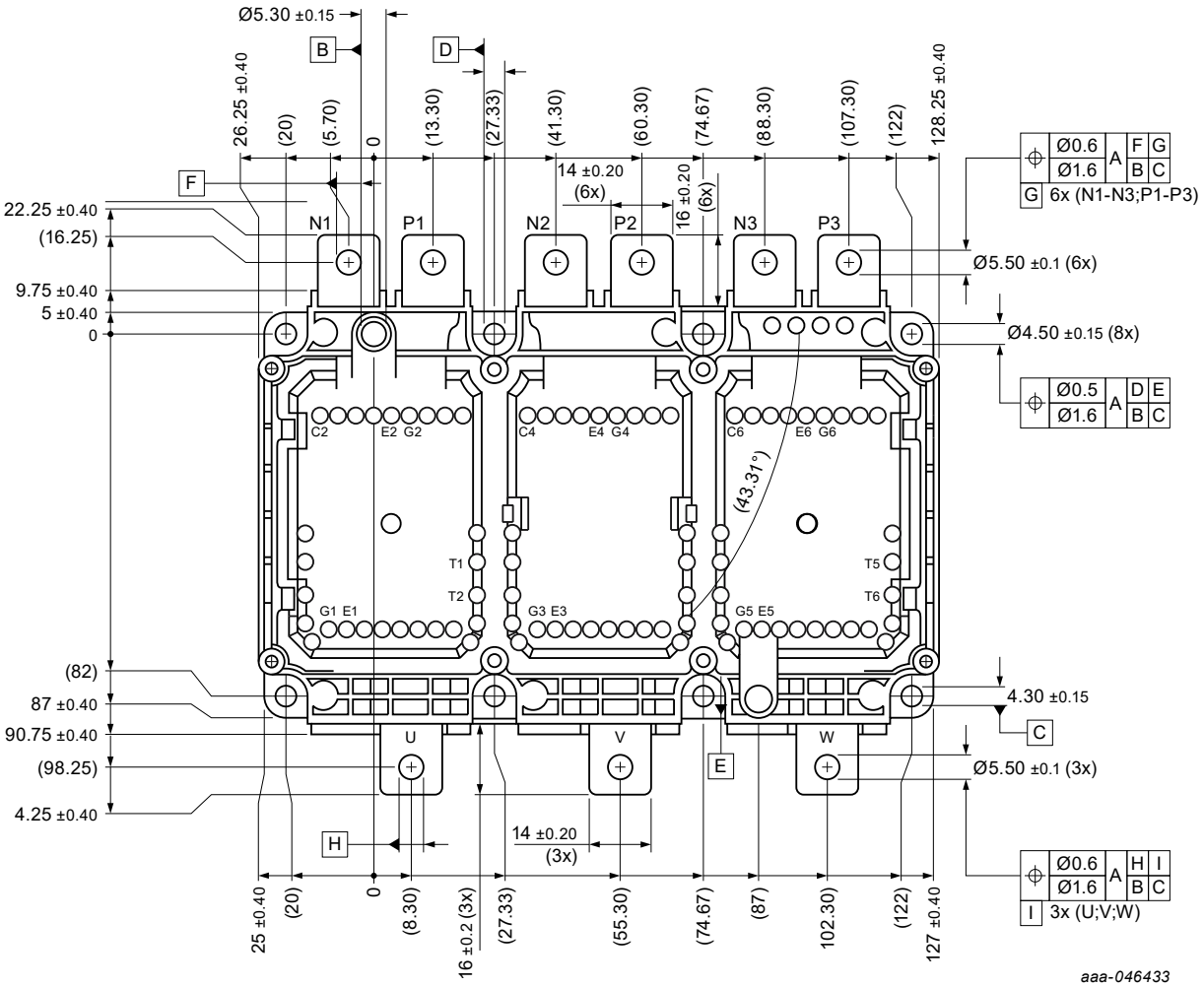


Figure 9. SiC module pin placement

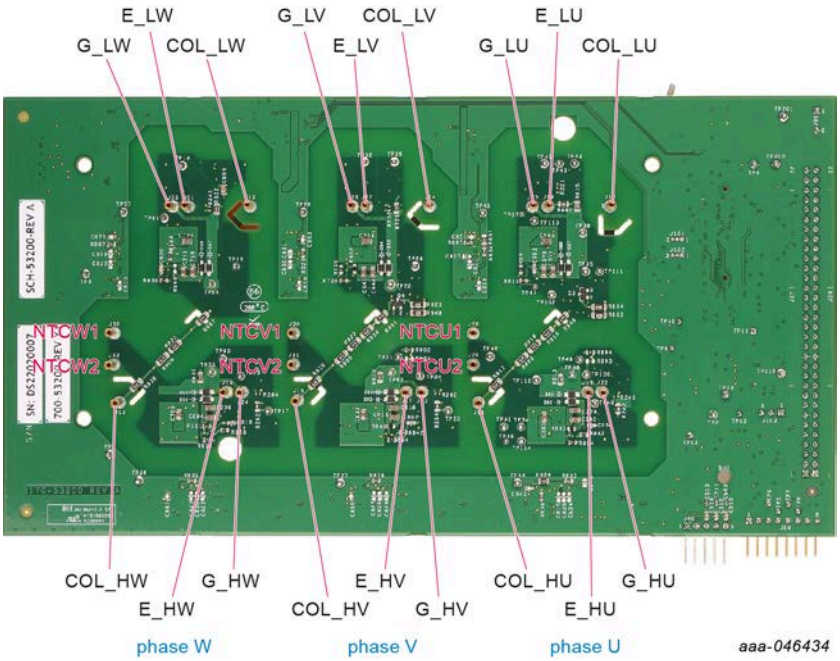


Figure 10. SiC module pin connections

Table 6. SiC module pin connections

Connection name	Pin description
G_HU	gate high-side U phase
E_HW	emitter/source connection high-side U phase
COL_HU	collector/drain connection high-side U phase
NTCU1	NTC temperature sensor connection U phase (high-side TSENSEA)
NTCU2	NTC temperature sensor connection U phase (high-side isolated ground)
G_LU	gate low-side U phase
COL_LU	collector/drain connection low-side U phase
E_LU	emitter/source connection low-side U phase
NTCV1	NTC temperature sensor connection V phase (high-side TSENSEA)
NTCV2	NTC temperature sensor connection V phase (high-side isolated ground)
G_HV	gate high-side V phase
COL_HV	collector/drain connection high-side V phase
E_HV	emitter/source connection high-side V phase
G_LV	gate low-side V phase
E_LV	emitter/source connection low-side V phase
COL_LV	collector/drain connection low-side V phase
NTCW1	NTC temperature sensor connection W phase (high-side TSENSEA)
NTCW2	NTC temperature sensor connection W phase (high-side isolated ground)

Table 6. SiC module pin connections...*continued*

Connection name	Pin description
G_HW	gate high-side W phase
E_HW	emitter/source connection high-side W phase
COL_HW	collector/drain connection high-side W phase
G_LW	gate low-side W phase
E_LW	emitter/source connection low-side W phase
COL_LW	collector/drain connection low-side W phase

6.3 Kinetis KL25Z Freedom board

The Freedom KL25Z is an ultra low-cost development platform for Kinetis L series MCU built on Arm Cortex-M0+ processor.

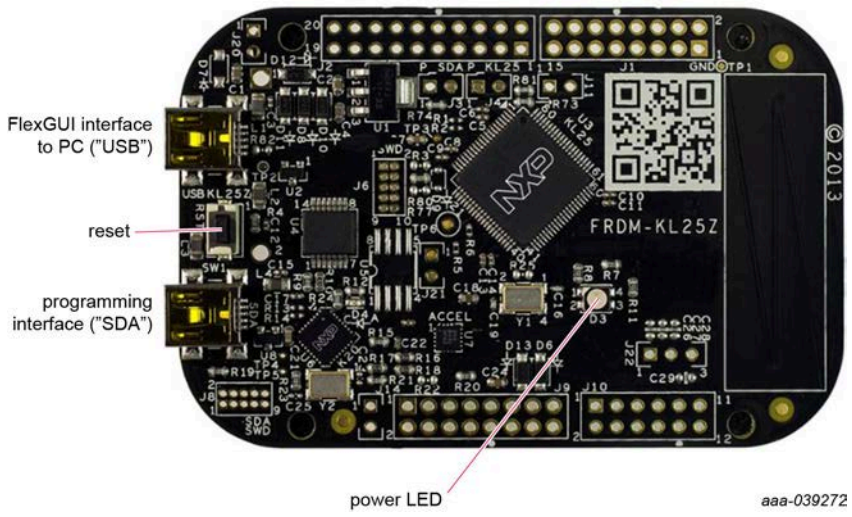


Figure 11. Freedom development platform

6.4 3.3 V to 5.0 V translator board

KITGD316xTREVB translator enables level shifting of signals from MCU 3.3 V to 5.0 V SPI communication.

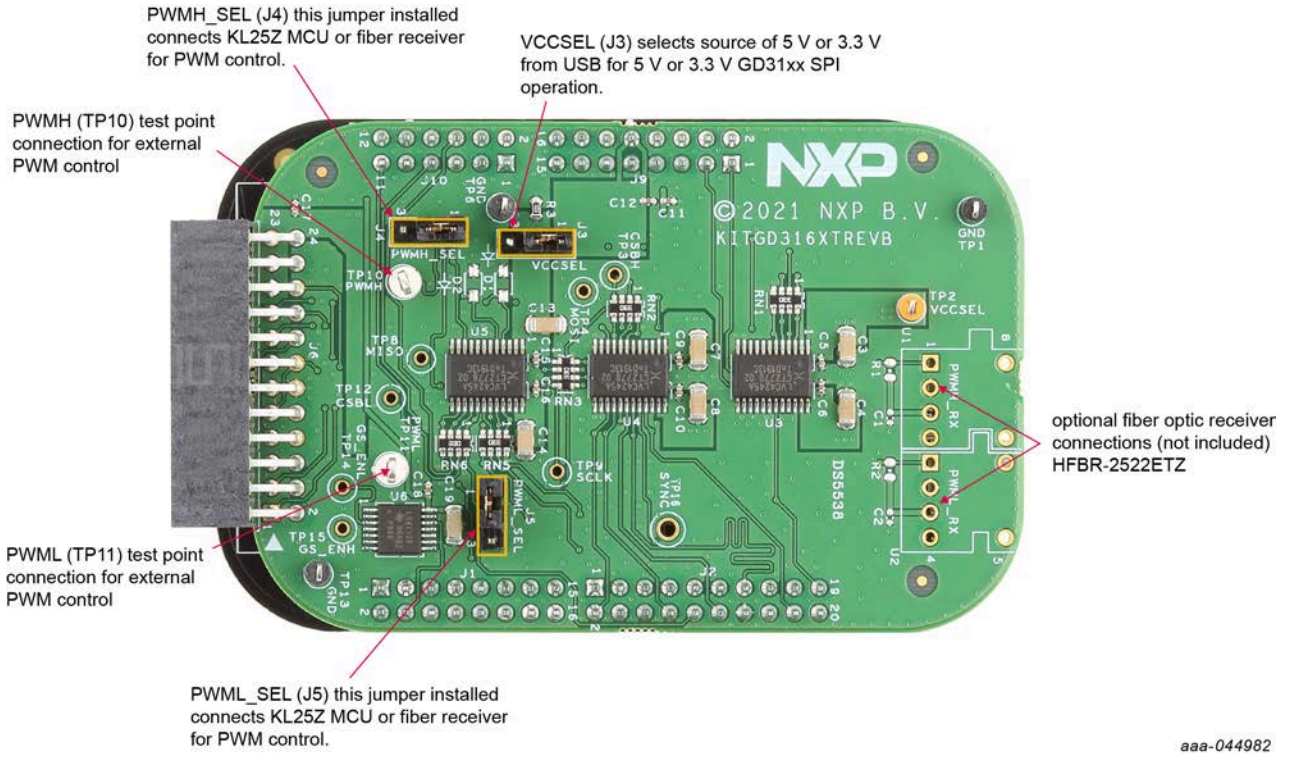


Figure 12. Translator board

Table 7. Translator board jumper definitions

Jumper	Position	Function
VCCSEL (J3)	1-2	selects 5.0 V for 5.0 V compatible gate drive
	2-3	selects 3.3 V for 3.3 V compatible gate drive
PWMH_SEL (J4)	1-2	selects PWM high-side control from KL25Z MCU
	2-3	selects PWM high-side control from fiber optic receiver inputs
PWML_SEL (J5)	1-2	selects PWM low-side control from KL25Z MCU
	2-3	selects PWM low-side control from fiber optic receiver inputs

7 Installing and configuring software and tools

Software for RDGD3162I3PH5EVB is distributed with the FlexGUI 2 for GD3162 tool (available on NXP.com). Necessary firmware comes preinstalled on the FRDM-KL25Z with the kit.

Even if you intend to test with other software or PWM, it is recommended to install this software as a backup or to help debugging.

7.1 Installing FlexGUI 2 for GD3162 on your computer

The latest version of FlexGUI 2 supports GD3162. It is designed to run on any Windows 10 or higher based operating system. To install the software, do the following:

1. Go to www.nxp.com/FlexGUI and click **Download**.
2. When the FlexGUI 2 software page appears, click **Download** and select the version associated with your PC operating system.
3. FlexGUI 2 wizard creates a shortcut, an NXP FlexGUI 2 icon appears on the desktop. By default, the FlexGUI 2 executable file is installed at **C:\NXP_GD3162_GUI-x.x.x.msi**.
   Installing the device drivers overwrites any previous FlexGUI 2 installation and replaces it with a current version containing the GD3162 drivers. However, configuration files from the previous version remain intact.

7.2 Configuring the FRDM-KL25Z microcode

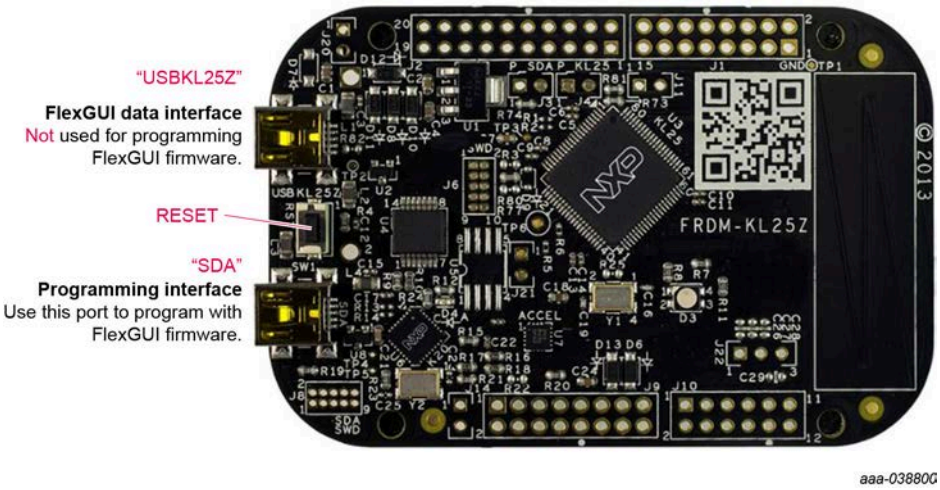


Figure 13. FRDM-KL25Z setup and interface

By default, the FRDM-KL25Z delivered with this kit is preprogrammed with the current and most up-to-date firmware available for the kit.

A way to check quickly that the microcode is programmed and the board is functioning properly, is to plug the KL25Z into the computer, open FlexGUI 2 for GD3162, and verify that the software version at the bottom is 6.4 or later (see Figure 13).

If a loss of functionality following a board reset, reprogramming, or a corrupted data issue, the microcode is rewritten per the following steps:

1. To clear the memory and place the board in bootloader mode, hold down the reset button while plugging a USB cable into the **OpenSDA** USB port.
2. Verify that the board appears as a BOOTLOADER device and continue with step 3. If the board appears as KL25Z, go to step 6.
3. Download the **Firmware Apps**.zip archive from the PEmicro OpenSDA webpage (http://www.pemicro.com/opensda/). Validate your email address to access the files.
4. Find the most recent MDS-DEBUG-FRDM-KL25Z_Pemicro_v118.SDA and copy/drag-and-drop into the **BOOTLOADER** device.
5. Reboot the board by unplugging and replugging the connection to the **OpenSDA** port. Verify now that the device appears as a KL25Z device to continue.
6. Locate the most recent KL25Z firmware; which is distributed as part of the FlexGUI 2 for GD3162 package.
   a. From the FlexGUI 2 install directory or zip file, downloaded, find the firmware bin file "flexgui2_fw_kl25z_gd3162_vx.x.x.bin".
   b. This .bin file is a product/family-specific configuration file for FRDM-KL25Z containing the pin definitions, SPI/PWM generation code, and pin mapping assignments necessary to interface with the translator board as part of RDGD3162I3PH5EVB.
7. With the KL25Z still plugged through the **OpenSDA** port, copy/drag-and-drop the .bin file into the KL25Z device memory at PC drive FRDM-KL25Z (D:). Once done, disconnect the USB for OpenSDA port and plug into the other USB port, labeled **KL25Z**.
   a. The device does not appear as a distinct device to the computer while connected through the KL25Z USB port, which is normal.
8. The FRDM-KL25Z board is now fully set up to work with RDGD3162I3PH5EVB and the FlexGUI 2.
   a. There is no software stored or present on either the driver or translator boards, only on the FRDM-KL25Z MCU board.

All uploaded firmware is stored in nonvolatile memory until the reset button is hit on the FRDM-KL25Z. There is no need to repeat this process upon every power up, and there is no loss of data associated with a single unplug event.

7.3 Using the FlexGUI 2

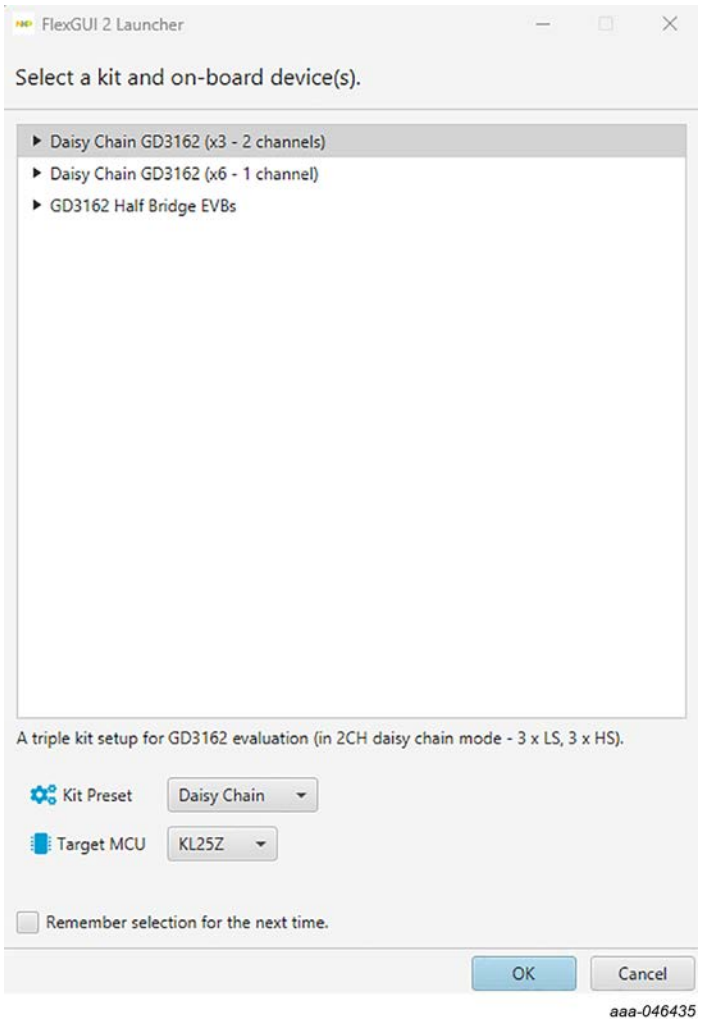
The FlexGUI 2 for GD3162 is available from http://www.nxp.com/FlexGUI as an evaluation tool demonstrating GD3162-specific functionality, configuration, and fault reporting. FlexGUI 2 also includes basic capacity for the RDGD3162I3PH5EVB to control an IGBT or SiC module, enabling double pulse or short-circuit testing.

SPI messages can be realized graphically or in hexadecimal format. CSB is selectable to daisy chain address. 3 low-side gate drivers and 3 high-side gate drivers simultaneously with (× 3 - 2 channel) selection or all 6 gate drivers with (× 6 - 1 channel). See Figure 14 for FlexGUI 2 for GD3162 internal register read and write access.

Starting FlexGUI 2 for GD3162

- FlexGUI 2 for GD3162 install program (C:\NXP_GD3162_GUI-x.x.x.msi)
- Download FlexGUI 2 and run the install program on your PC.
- When you start the application, Figure 14 allows you to select the target application board, feature set (standard or daisy chain), target MCU, and USB interface. Leave all settings as shown.

Once the kit is selected press Ok and select CONNECT FlexGUI 2 on following GUI page. Micro-USB cable must be attached from PC and KL25Z port on KL25Z board.



See Table 4 for required jumper configuration to enable (× 3 - 2 channel) or (× 6 - 1 channel) SPI daisy chain operation.

Figure 14. Kit selection

FlexGUI_2 connection

- Select FRDM-KL25Z COM port from the drop-down menu and select Connect to establish USB connection
  - If connection is not established, check USB cable connection between PC and KL25Z port and or scan again and select an alternate COM port for FRDM-KL25Z
  - If connection is not established, ensure that proper firmware is installed on FRDM-KL25Z MCU for FlexGUI 2 (refer to step 6 in Section 7.2)

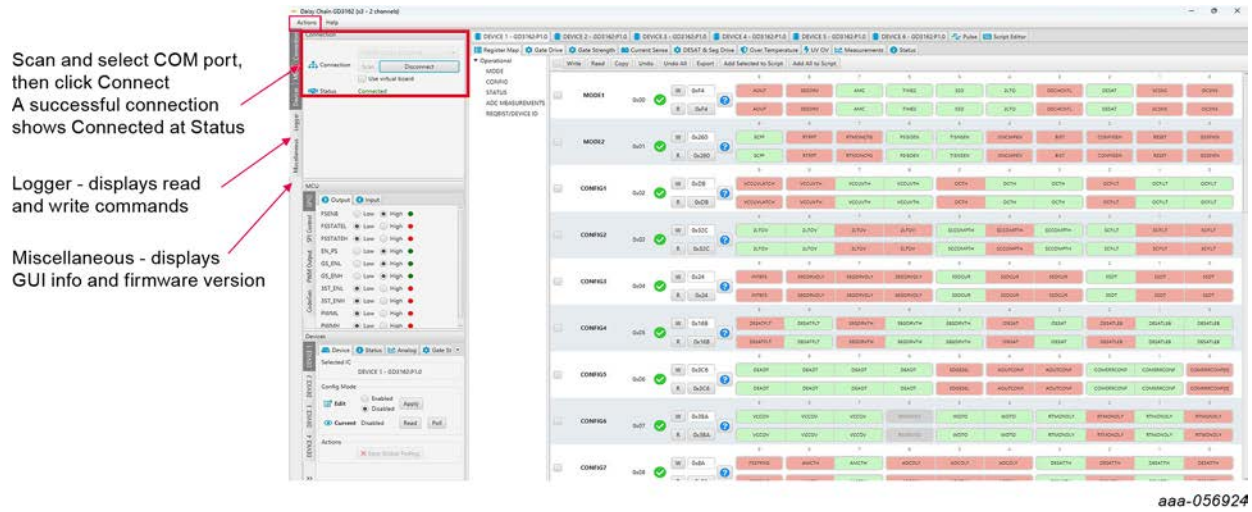
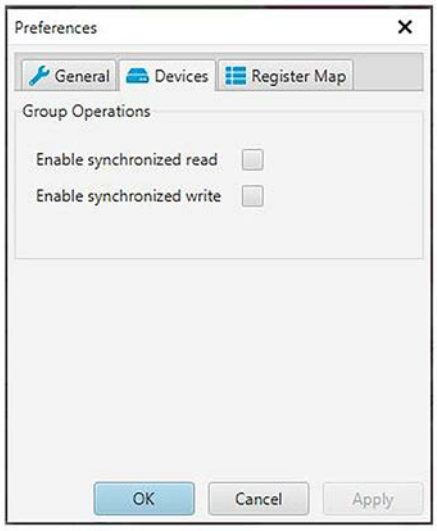


Figure 15. FlexGUI 2 connection

Set GUI actions and preferences

Access preferences from Actions menu at top left of GUI

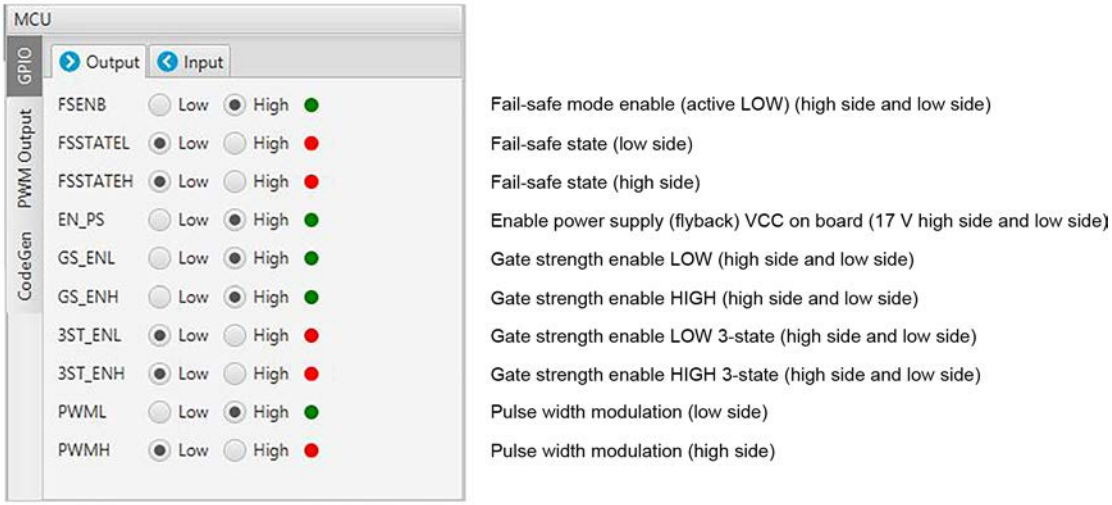


Enable synchronized read and write to set both HS and LS devices simultaneously with same settings if desired

Enable Use register init value and Enable read after write and Enable to set read value to write value if desired (recommended)

aaa-055040

Figure 16. Actions and preferences settings



Set logic level on gate drive and hardware inputs as desired.

aaa-055041

Figure 17. MCU GPIO output control

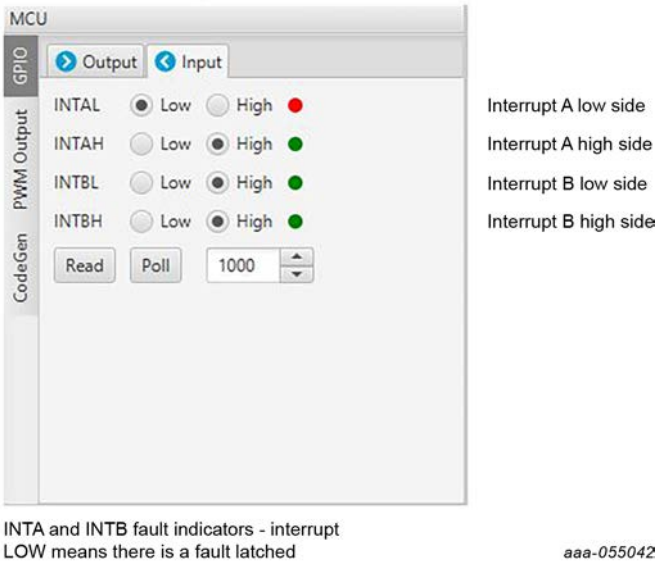


Figure 18. MCU GPIO input

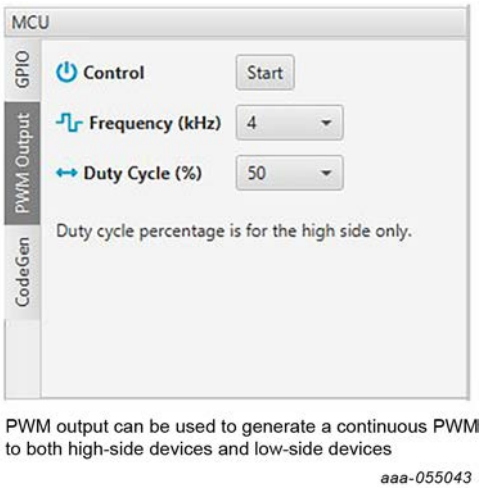


Figure 19. MCU PWM output

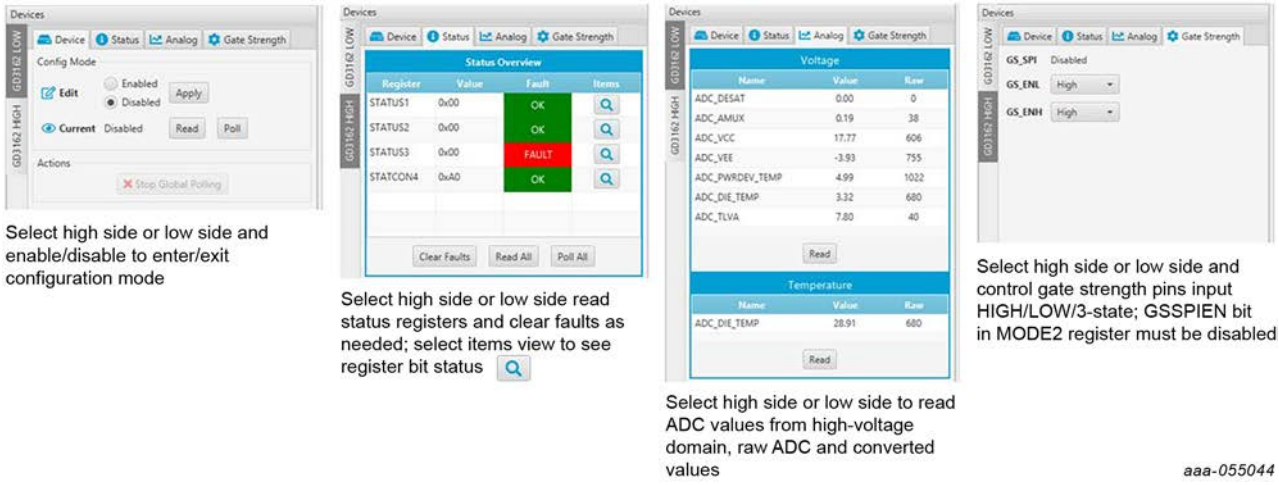


Figure 20. Devices

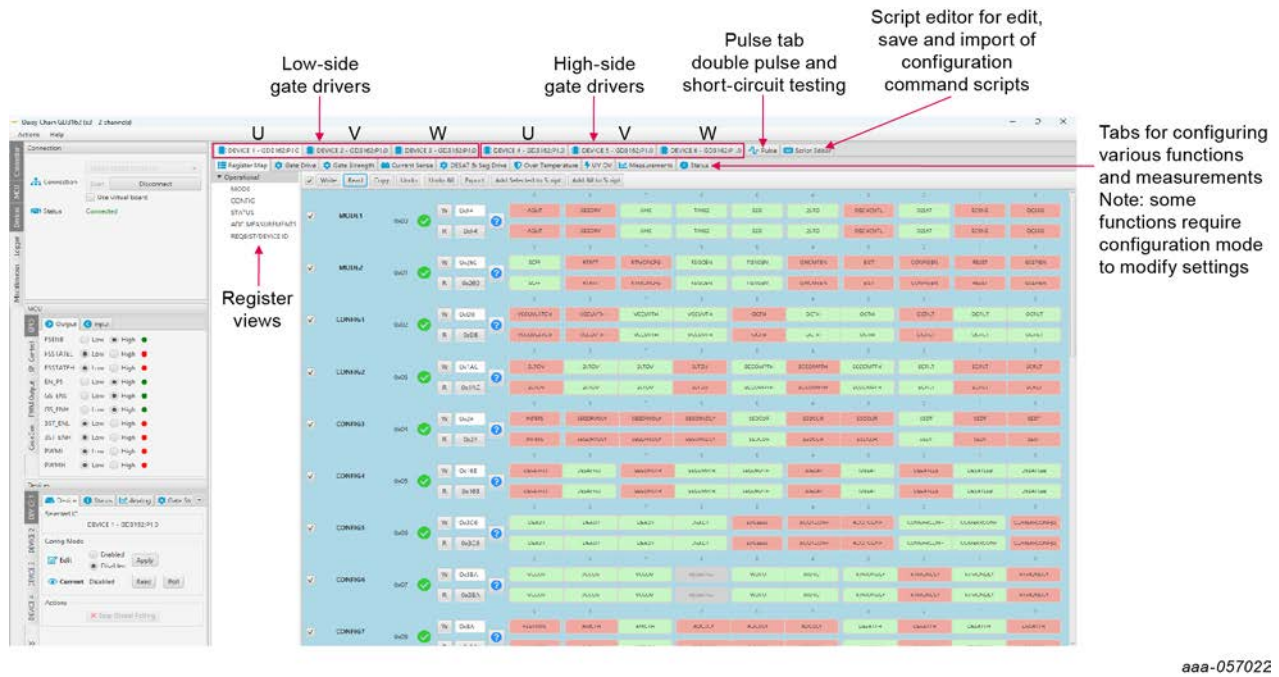


Figure 21. GUI tabs

- Registers are grouped according to function; independent lines to read and write the registers
- Individual registers can be read by clicking the R button and can be written by using the W button
- Copy button to copy the read values to the write line; can be set to copy automatically
- Global register controls perform the selected command on all registers with the checkbox selected
- Add to Script adds current and selected register values to a script in the script editor window

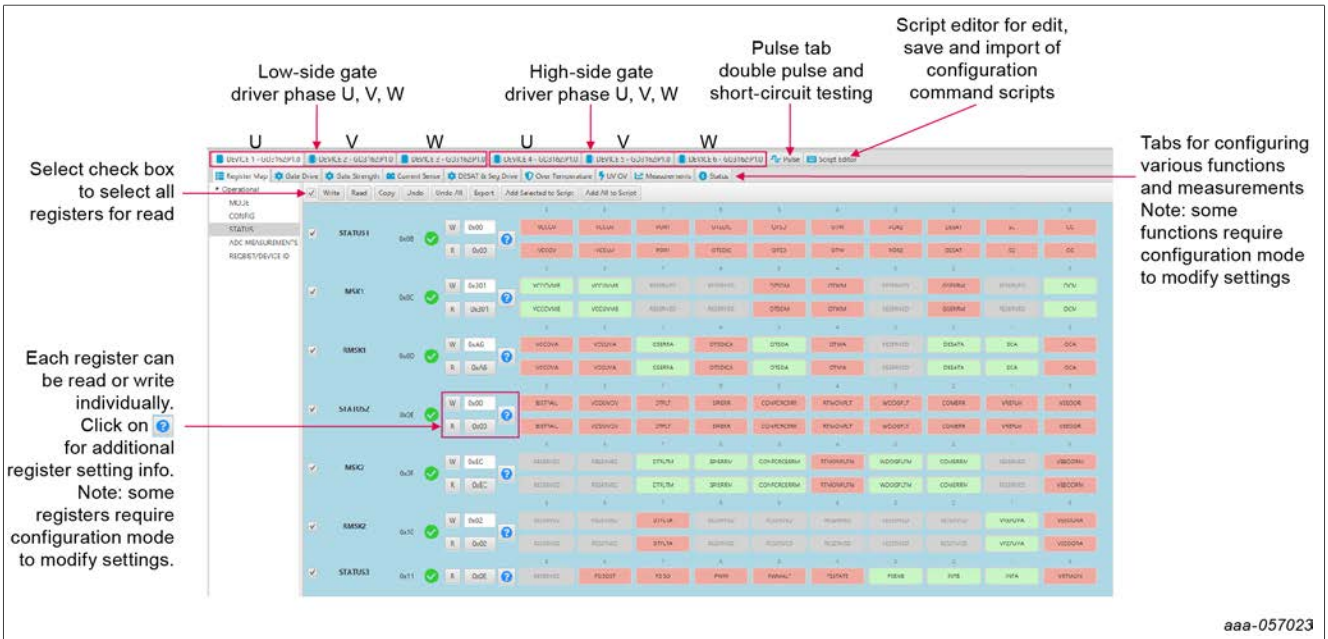
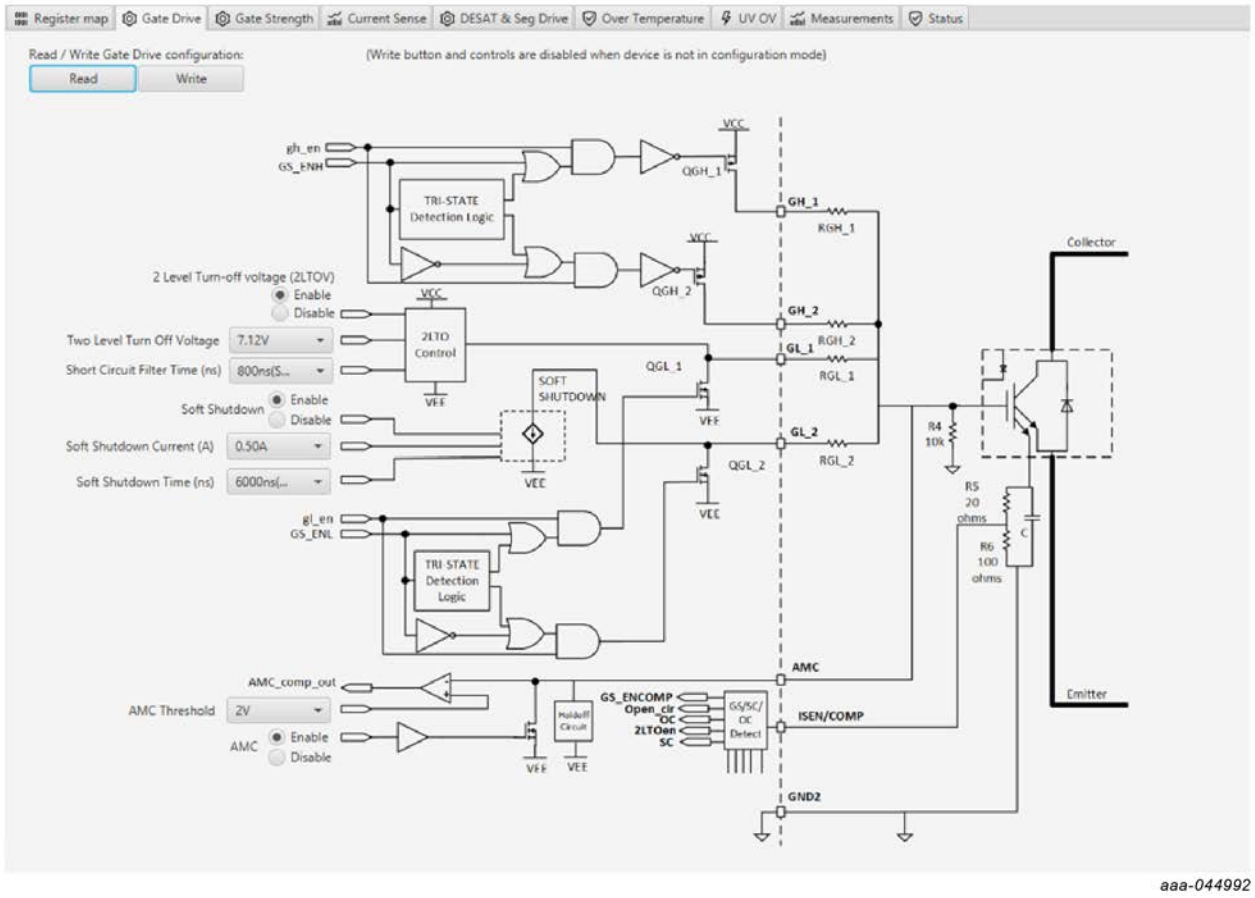


Figure 22. GUI tabs continued

Gate Drive tab

- Allows setting of parameters related to the gate drive; controls are disabled when not in config mode
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls.



aaa-044992

Figure 23. Gate drive tab

Current Sense tab

- Allows setting of parameters related to current sense
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls.

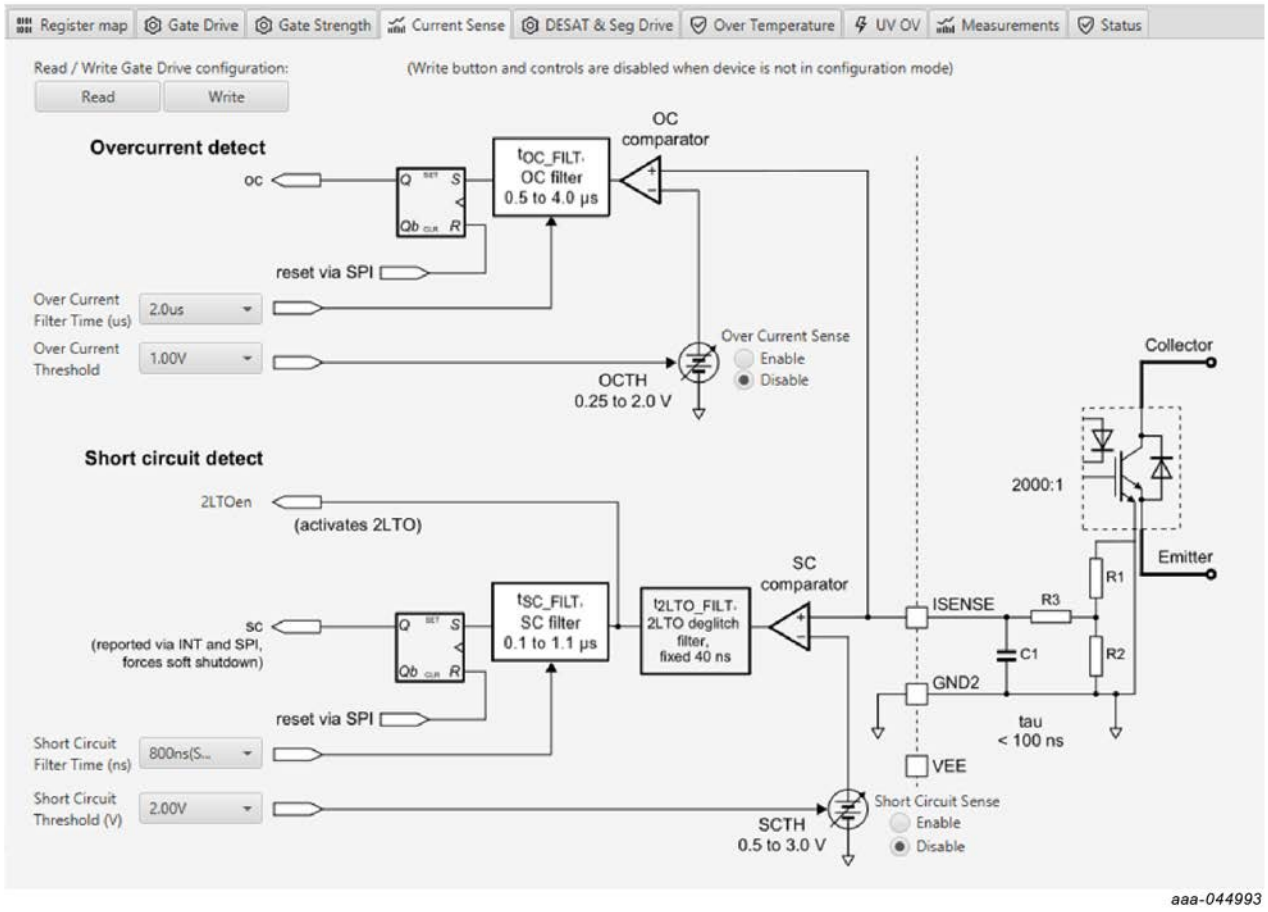


Figure 24. Current sense tab

DESAT & Seg Drive tab

- Allows setting of parameters related to desat and segmented drive
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls.

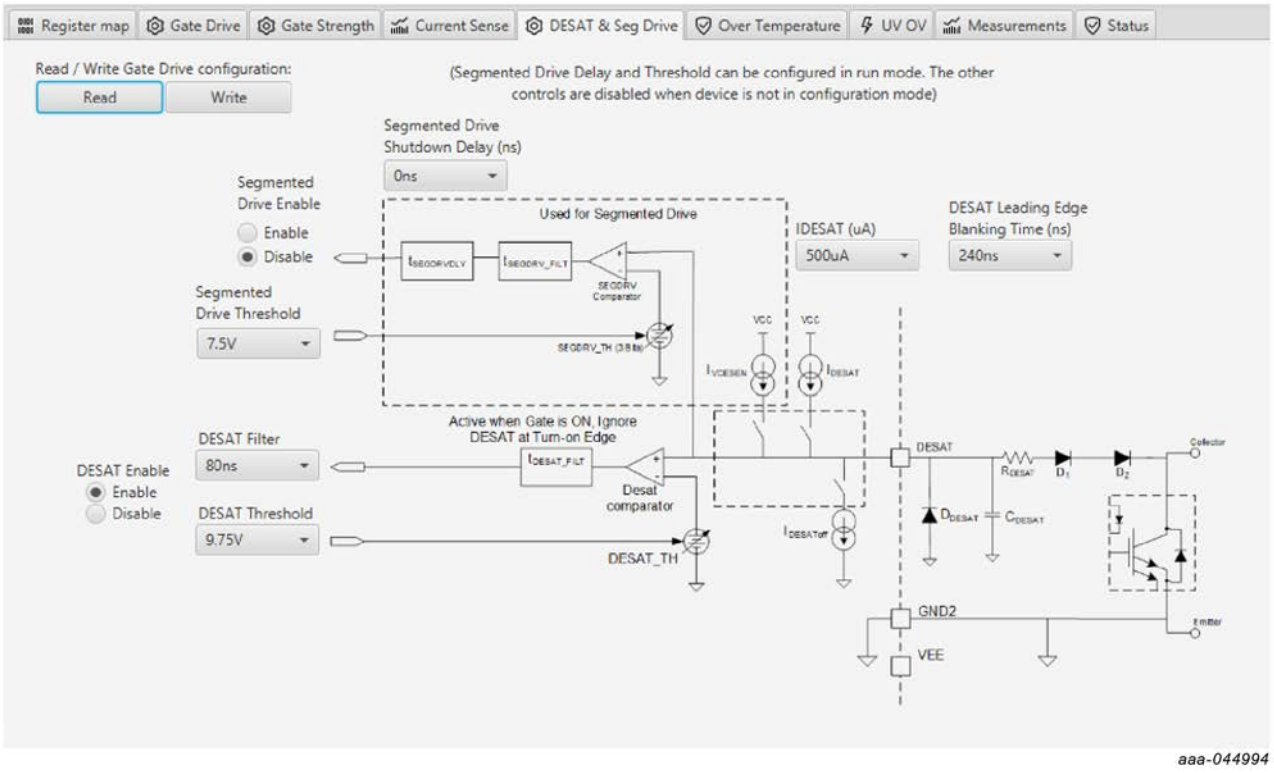


Figure 25. Desat and segmented drive tab

Overtemperature tab

- Allows setting of parameters related to overtemperature and overtemperature warning thresholds
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls.

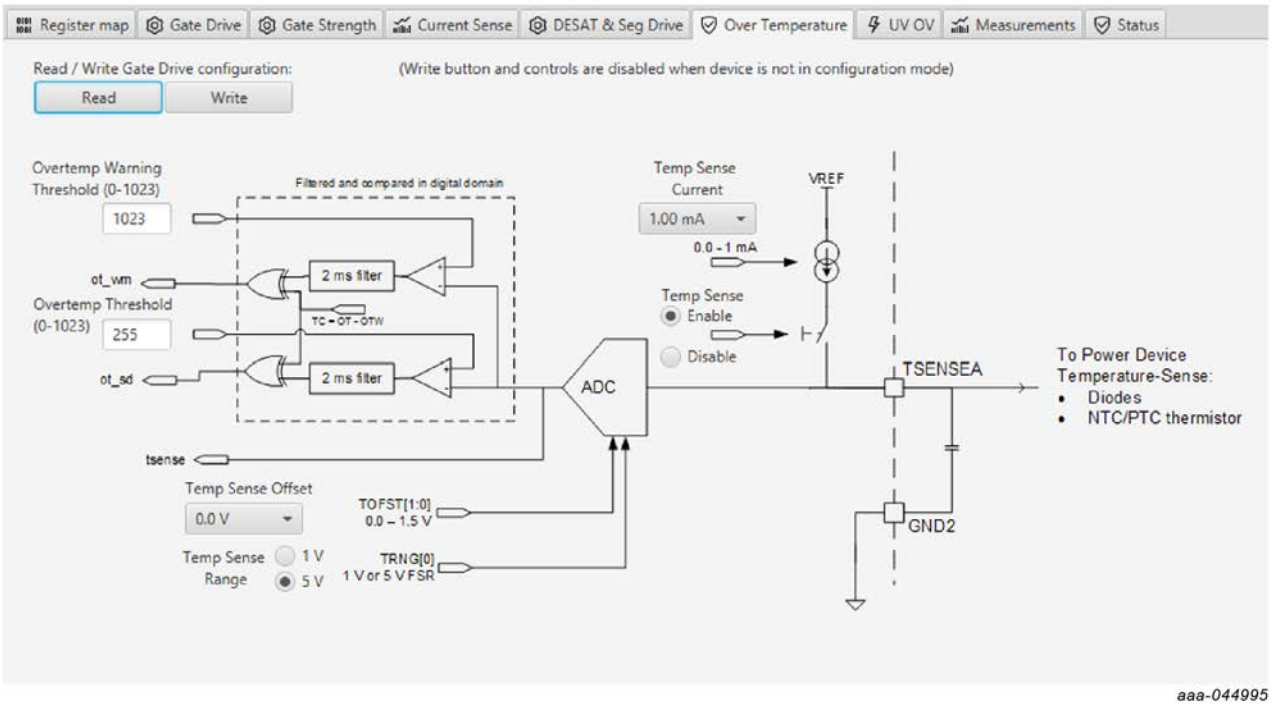


Figure 26. Overtemperature tab

Undervoltage and overvoltage threshold tab

- Allows setting of parameters related to undervoltage and overvoltage threshold
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls.

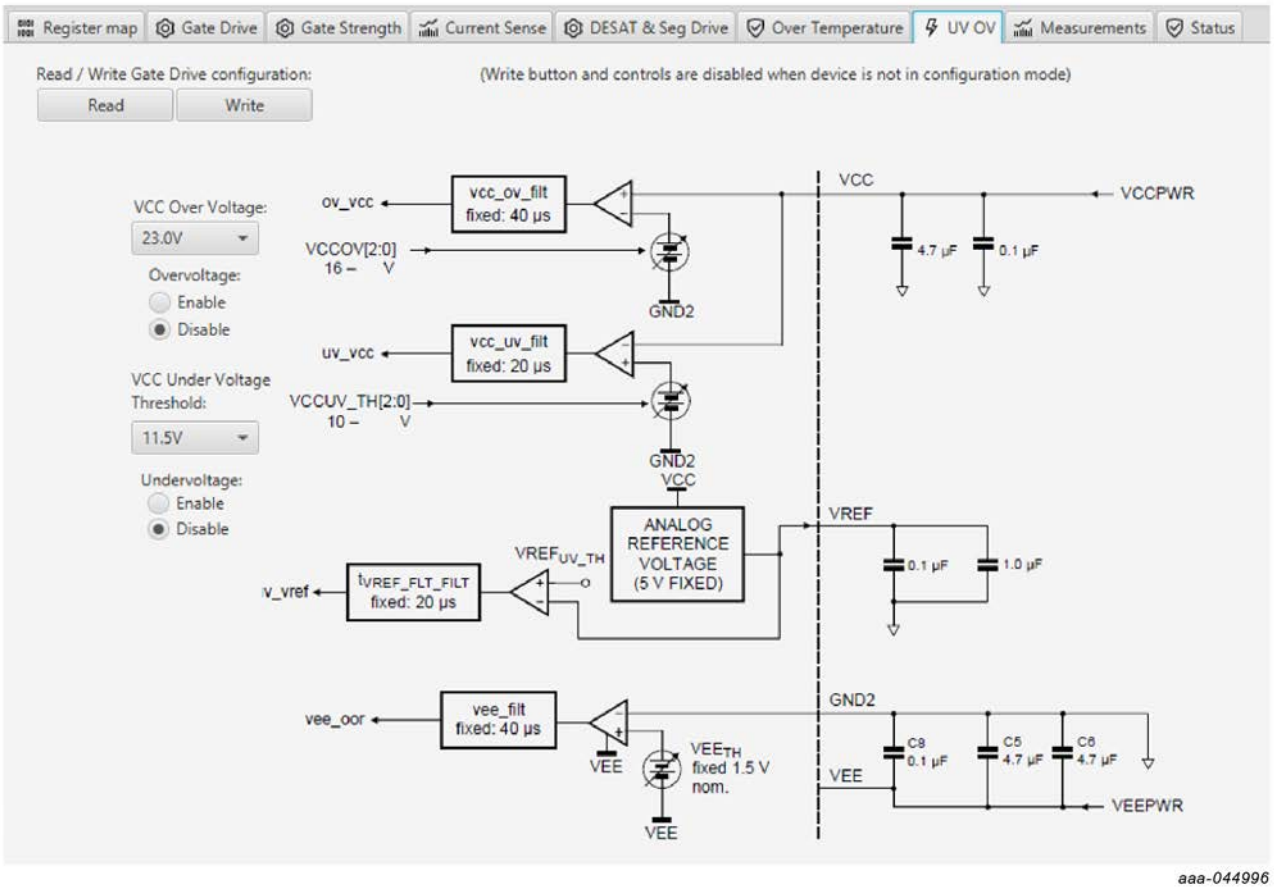


Figure 27. Undervoltage and overvoltage threshold tab

Measurements tab

- Allows monitoring and graphing of ADC and temperature values

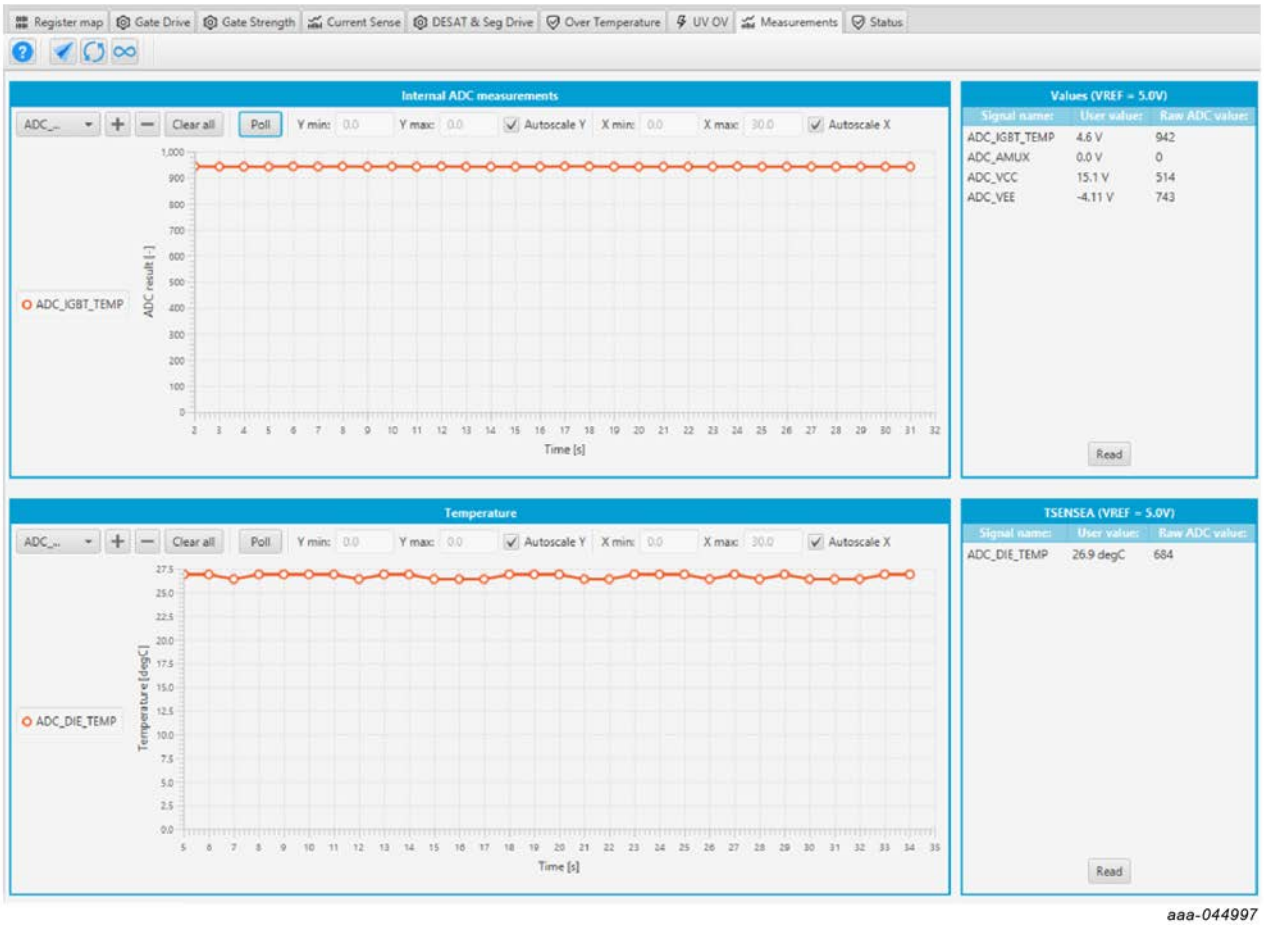


Figure 28. Measurements tab

Pulse tab

- Used for double pulse, short circuit, and PWM testing
- Select desired t1, t2, and t3 timings for each test type; select enable then generate pulses

Note: *Phase U can be configured for performing double pulse and short-circuit testing. To enable short-circuit testing, two resistors (R857, R862) must be pulled from PWMALT phase U signals to disable dead time control on phase U gate drivers.*

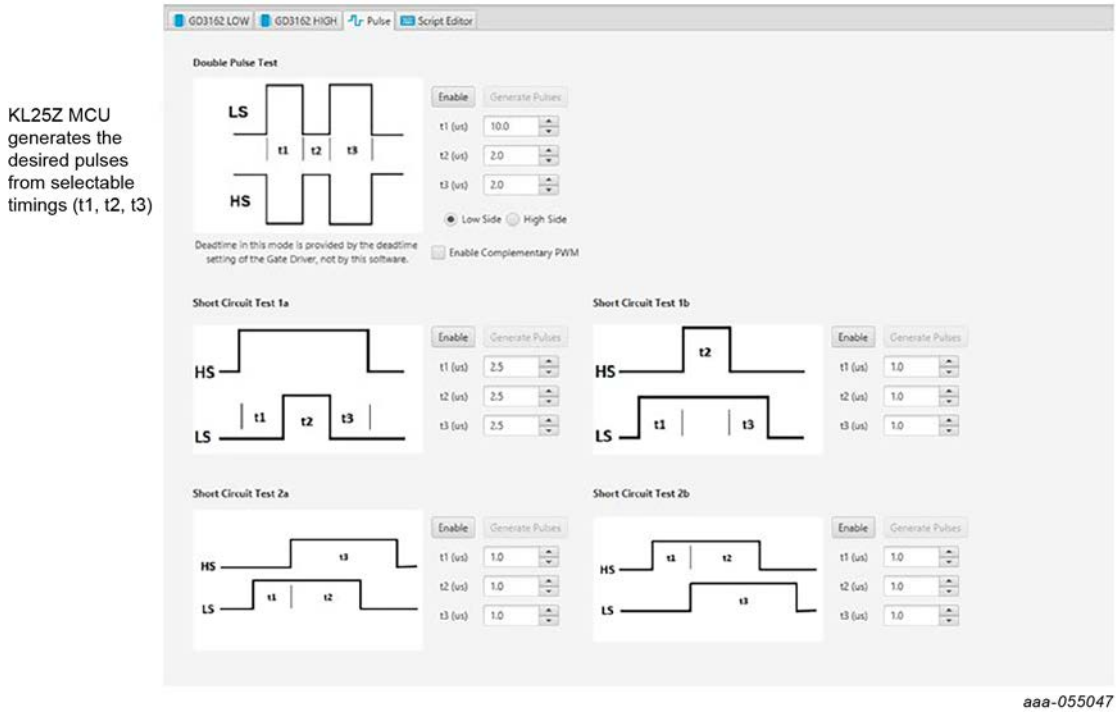


Figure 29. Pulse tab

Script editor tab

- Scripts can be used for setting up configurations on all devices and saved for reuse.

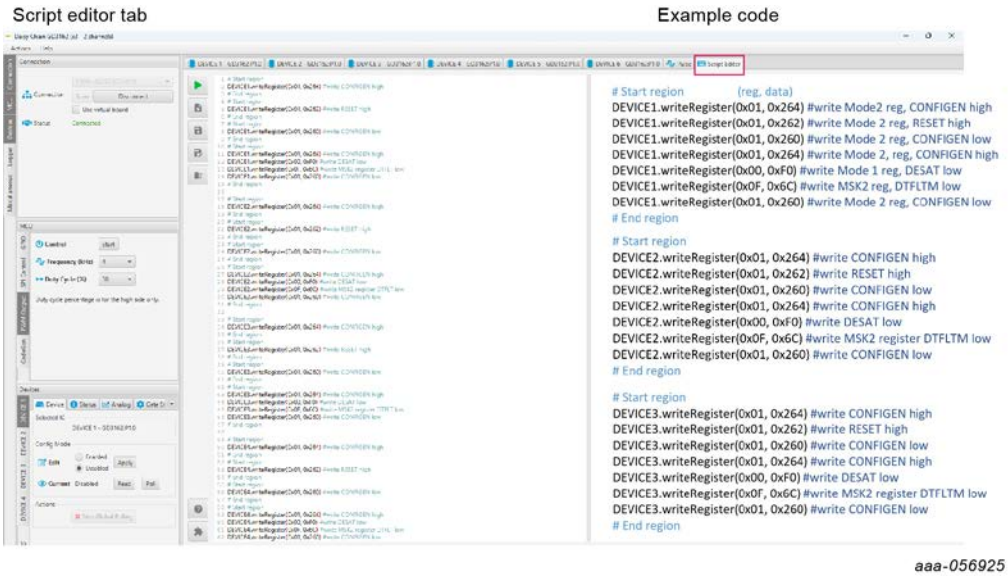


Figure 30. Script editor tab

7.4 Troubleshooting

Some common issues and troubleshooting procedures are detailed below. This is not an exhaustive list by any means, and additional debug may be needed:

Problem	Evaluation	Explanation	Corrective action(s)
Unable to establish COM port connection	Check USB cable is connected to KL25Z port on FRDM-KL25Z MCU	If the USB cable is not connected to PC USB and KL25Z port GUI will not be able to establish USB connection	Plug in USB cable to PC USB port and FRDM-KL25Z KL25Z port
	Incorrect firmware installed on FRDM-KL25Z MCU	If the incorrect firmware is installed on the FRDM-KL25Z MCU board GUI will not be able to establish USB connection	Go to step 5 in this user guide for installing FlexGUI 2 on your computer to locate firmware file in GUI download package and copy to FRDM-KL25Z through OpenSDA port on MCU board.
	Check the COM port setting on FlexGUI 2. The drop-down menu will show the various COM ports available.	Selecting the incorrect COM port in the COM port drop-down menu will not be able to establish USB connection.	Select an alternative COM in the COM port drop-down menu on FlexGUI 2.
No PWM output (no fault reported)	Check PWM jumper position on translator board	Incorrect PWM jumpers obstruct signal path but not report fault	Set PWMH_SEL (J4) and PWML_SEL (J5) jumpers properly, for desired control method: • 3.3 V to 5.0 V translator board reviewed in Section 6.4
	Check PWM control signal	Ensure that proper PWM signal is reaching GD3162	Monitor PWML (TP11) and PWMH (TP10) on translator board for commanded PWM state. Check position of jumpers J4 and J5 on translator board.
	Check FSENB status (see GD3162 pin 15, STATUS3)	PWM is disabled when FSENB = LOW	Set pin FSENB = HIGH (pin 15) to continue
	Check CONFIG_EN bit (MODE2)	PWM is disabled when CONFIG_EN is logic 1	Write CONFIG_EN = logic 0 to continue

Problem	Evaluation	Explanation	Corrective action(s)
No PWM output (fault reported)	Check VGE fault (VGE_FLT)	A short on IGBT or SiC module gate, or too low of VGEMON delay setting causes VGE fault, locking out PWM control of the gate.	Clear VGE_FLT bit (STATUS2) to continue. Increase VGEMON delay setting (CONFIG6). If safe operating condition can be guaranteed, set VGE_FLTM (MSK2) bit to logic 0, to mask fault.
	Check for short-circuit fault (SC) in STATUS1 register	SC is a severe fault that disables PWM. SC fault cannot be masked	Clear SC fault to continue. Consider adjusting SC fault settings on GD3162: • Adjust short-circuit threshold setting (CONFIG2) • Adjust short-circuit filter setting (CONFIG2)
PWM output is good, but with persistent fault reported	Check for dead time fault (DTFLT) in STATUS2 register	Dead time is enforced, but fault indicates that PWM controls signals are in violation	Clear DTFLT fault bit (STATUS2). Check PWMHSEL (J10) and PWMLSEL (J14) are configured to bypass dead time faults. Consider adjusting dead time settings on GD3162: • Change mandatory PWM dead time setting (CONFIG5) • Mask dead time fault (MSK2)
	Check for overcurrent (OC) fault in STATUS1 register	OC fault latches, but does not disable PWM. OC fault cannot be masked.	Clear OC fault bit (STATUS1). Adjust OC fault detection settings on GD3162: • Adjust overcurrent threshold setting (CONFIG1) • Adjust overcurrent filter setting (CONFIG1)
PWM or FSSTATE rising edge has longer delay than falling edge	Check translator output voltage versus GD3162 VDD voltage	Low translator output voltage (compared with correct VDD at GD3162) causes the high threshold at the GD3162 pin to be crossed later than commanded	Check translator output voltage selection (J3) is configured to the same level as the GD3162 VDD Check VCCSEL supply or translator outputs on the translator board for excessive loading or supply droop/pulldown
WDOG_FLT reported on startup	Check VSUP and VCC are powered	On initialization, watchdog fault is reported when one die is powered up before the other	Check VSUP and VCC both have power applied. Clear WDOG_FLT bit (STATUS2) to continue.
SPIERR reported on startup	Check KL25Z/translator connection	On initialization, SPIERR can occur when the SPI bus is open, or when GD3162 IC is powered up before the translator (which provides CSB).	Clear SPIERR fault to continue. Reinitialize power to GD3162 after translator is powered (over USB).
SPIERR reported after SPI message	Check bit length of message sent	There is SPIERR if SCLK does not see a n*24 multiple of cycles	Use 24-bit message length for SPI messages
	Check CRC	SPIERR faults if CRC provided in sent message is not good	Use FlexGUI to generate commands with valid CRC. The command can be copied in binary or hexadecimal and sent from another program.
	Check for sufficient dead time between SPI messages	SPIERR fault bit is set when the time between SPI messages (txfer_delay) received is too short. Minimum required delay time is 19 µs.	Check time between CSB rising edge (old message end) and CSB falling edge (new message start) during normal SPI read, and ensure transfer delay dead time check. SPIERR can also be cleared in BIST.
VCCREGUV reported on startup	Check VCCREG potential	Caused by low VCC	Clear VCCREGUV fault bit (STATUS1). Tune VCC-GNDISO potential with power supply set resistor (R37).

Problem	Evaluation	Explanation	Corrective action(s)
VREFUV reported on startup	Check HV domain is powered correctly	Related to slow rise time of VCC supply on HV domain, or failed VREF regulator	Clear VREFUV bit (STATUS2). Reset HV domain supply if fault bit does not clear.
	Check VCC for undervoltage condition	Low VCC is visible indirectly through other HV domain faults	Tune VCC-GNDISO using R37 feedback
VCCOV fault reported on startup	Check VEE level on suspect domain.	If VEE level is not at desired negative voltage it could cause excessive VCC level.	Check Zener diode in power supply circuit for proper value in setting VEE level. Clear VCCOV bit (STATUS1) to continue.
	Check VCC-GNDISO potential	PWM is disabled during a VCC overvoltage (20 V nom.)	Tune VCC-GNDISO potential to suitable level with power supply set resistor (R37). Clear VCCOV bit (STATUS1) to continue.
No PWM during short circuit test	Check PWMxSEL jumpers	Incorrect configuration of PWMALT pins prevent short-circuit test by enforcing dead time	Resistors R857, R862 must be unpopulated to disable dead time control for short circuit testing. See Pulse tab in Section 7.3.
Bad SPI data, appears to repeat previous response	Check VSUP/VDD for undervoltage condition	VDD_UV latches SPI buffer contents, preventing updated fault reporting.	Check voltage provided at VDD pin (pin 3). On each read, compare the address from the sent command and response (a difference indicates that the SPI response is latched due to inactive). Read multiple addresses to ensure a good comparison.
	Check EN_PS is set to HIGH in FlexGUI 2; see Figure 17	VCC/VEE can be enabled/disabled in software.	EN_PS in GPIO output tab on Flex GUI 2; see Figure 17
	Check VCC for undervoltage	Unpowered VCC prevents HV domain from updating data	Tune VCC-GNDISO using R37 feedback

8 Configuring the hardware

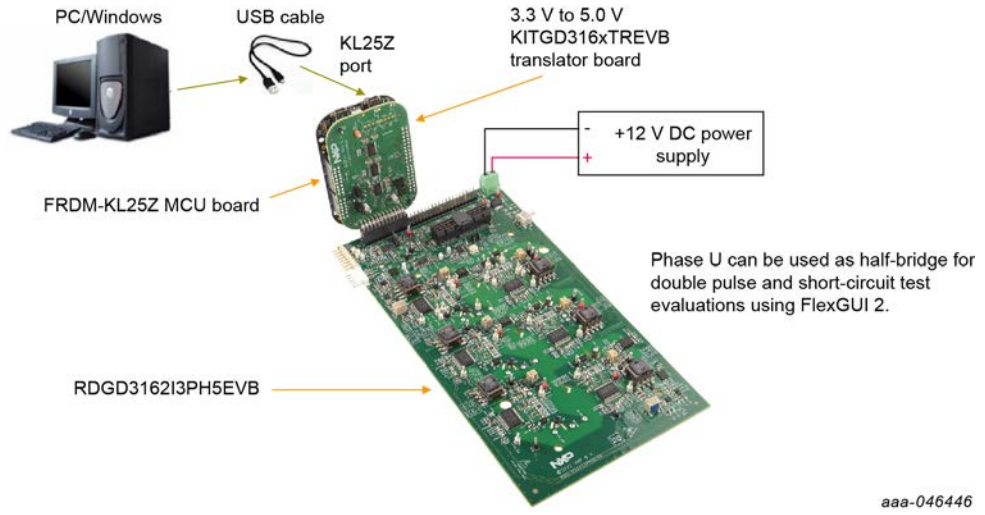
RDGD3162I3PH5EVB with KITGD316xTREVB attached as shown in Figure 31 using Windows based PC and FlexGUI 2 software.

Note: *Double pulse and short-circuit testing can be conducted on phase U only. See FlexGUI 2 Pulse tab Figure 29.*

Suggested equipment needed for test:

- Rogowski coil high-current probe
- High-voltage differential voltage probe
- High sample rate digital oscilloscope with probes
- DC link capacitor compatible with HybridPACK Drive module
- IGBT or SiC MOSFET HybridPACK Drive module
- Windows based PC
- High-voltage DC power supply for DC link voltage
- Low-voltage DC power supply for VPWR
  - +12 V DC gate drive board low-voltage domain
- Voltmeter for monitoring high-voltage DC link supply
- Load coil for double pulse testing (phase U only)

Note: *To enable short-circuit testing on phase U only, two resistors (R857, R862) must be pulled from PWMALT phase U signals to disable dead time control on phase U gate drivers.*



DC link capacitor and power module are not shown

Figure 31. Evaluation setup using KITGD316xTREVB and FlexGUI 2

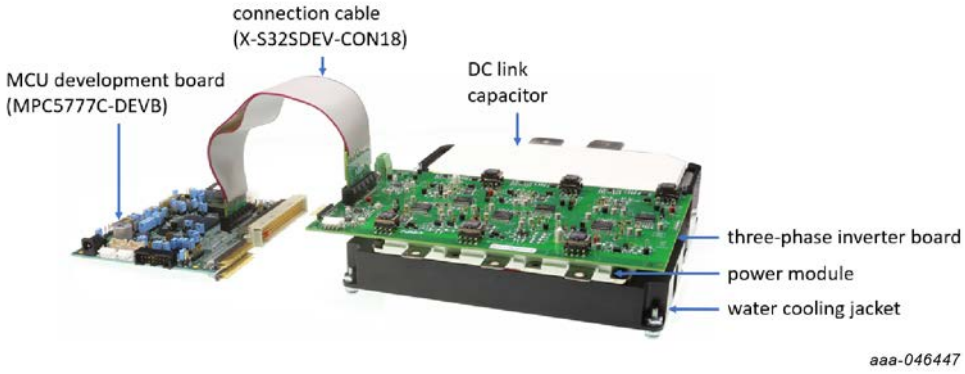


Figure 32. Evaluation setup using MPC5777C-DEVB MCU development kit

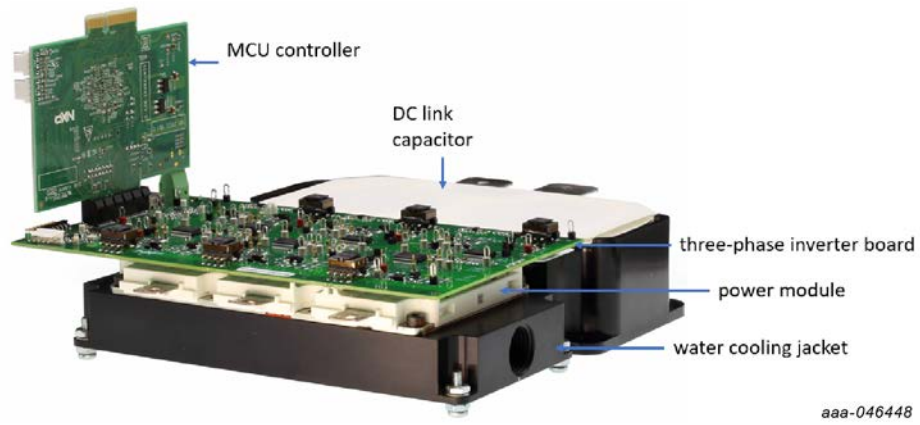


Figure 33. Evaluation setup using MPC5744P MCU development kit

9 Schematic, board layout, and bill of materials

The schematic, board layout, and bill of materials for the RDGD3162I3PH5EVB reference design are available at http://www.nxp.com/RDGD3162I3PH5EVB.

10 References

[1] RDGD3162I3PH5EVB detailed information on this board, including documentation, downloads, and software and tools http://www.nxp.com/RDGD3162I3PH5EVB

[2] GD3162 product information on advanced single-channel gate driver for IGBT/SiC http://www.nxp.com/GD3162

[3] MPC5777C ultra-reliable MCU for automotive and industrial engine management http://www.nxp.com/MPC5777C

[4] MPC5744P ultra-reliable MCU for automotive and industrial safety applications http://www.nxp.com/MPC574xP

[5] MPC5775B/E-EVB low-cost development board for battery management and inverter http://www.nxp.com/MPC5775B-E-EVB

11 Revision history

Table 8. Revision history

Document ID	Release date	Description
UM11802 v.3	27 August 2024	• Update for FlexGUI 2
UM11802 v.2	18 October 2023	• Table 6: changed emitter/drain to emitter/source and collector/source to collector/drain
UM11802 v.1	10 June 2022	• Initial version

Legal information

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at https://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

Suitability for use in automotive applications — This NXP product has been qualified for use in automotive applications. If this product is used by customer in the development of, or for incorporation into, products or services (a) used in safety critical applications or (b) in which failure could lead to death, personal injury, or severe physical or environmental damage (such products and services hereinafter referred to as "Critical Applications"), then customer makes the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. As such, customer assumes all risk related to use of any products in Critical Applications and NXP and its suppliers shall not be liable for any such use by customer. Accordingly, customer will indemnify and hold NXP harmless from any claims, liabilities, damages and associated costs and expenses (including attorneys' fees) that NXP may incur related to customer's incorporation of any product in a Critical Application.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer.

In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages.

Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

HTML publications — An HTML version, if available, of this document is provided as a courtesy. Definitive information is contained in the applicable document in PDF format. If there is a discrepancy between the HTML document and the PDF document, the PDF document has priority.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Kinetis — is a trademark of NXP B.V.

Tables

Figures

Contents