Rev. 1.1 — 5 September 2022

User manual

Document information

Information	Content
Keywords	Q100 eSwitch extreme switch
Abstract	This documentation describes how to install and use the Q100 Extreme Switch software driver.



Rev	Date	Description
v1.1	20220905	 Section 2.2: Corrected the following entry: 12 bits ADC: Current from 5.0 mA to 5.0 A with ± 6 % above 1 A Voltage from 0.5 to 65 V with ± 6.5 % above 5.0 V Temperature warning for each channel plus central die monitoring Revision history relocated
v.1.0	20190830	Initial version

1 Overview

This documentation describes how to install and use the Q100 Extreme Switch software driver (driver).

The Q100 Extreme Switch software driver encapsulates the functionality of the Q100 (MC33XS2410) device. The driver acts as an API layer between the microcontroller low-level drivers, e.g. SDK, and the user application, allowing you to perform the following:

- Setting and reading device registers (control and diagnostic bank)
- Initializing device with default or custom register values
- Controlling the OUTx channel by Direct Input or SPI signal, PWM or without PWM
- Reading fault, warning and channel status
- Measurements of voltage, current and temperature
- Enabling watchdog, transit to safe mode
- Setting PWM PI regulation

2 MCU compatibility

The driver implementation is generic; there is no dependency on a specific MCU. Virtually any MCU with the required peripherals should be able to use the driver.

2.1 Peripheral requirements

The driver needs the following MCU peripherals for its function:

- SPI Module is required for communication (MOSI_M, MISO_M, SCLK_M, CSB_M).
- **GPIO** is required for controlling RESET_B pin or optionally used for software controlled SPI chip select (CSB_M) instead of HW chip select.
- **Interrupt** pin is optionally required for use with the FAULT_B pin interrupt implementation is up to user.
- **Timer** is optionally required for generating external clock signal for Pulse-Width Modulation (PWM) of the Q100 device implementation is up to user

Depending on the user application, other resources may be required. See the provided example projects.

2.2 Supported devices

Q100 (MC33XS2410)

- Four fully-protected 100 m Ω / dual 50 m Ω (at 25 °C) high-side switches
- 4 x 1.8 A DC (Pd 2.5 W @ TJ 150 °C) or 2 x 3.6 A DC in parallel mode configuration
- · Floating power output architecture to drive all types of loads
- 16-bit SPI port communication 3.3 V / 5.0 V compatible with daisy chain capability
- Outputs controllable via SPI-bus or direct inputs
- Diagnostic status reported via SPI-bus
- Watchdog for invalid commands or inactive SPI, with programmable timeout
- Programmable interrupt generator that reports to FAULT pin or SPI-bus
- Four independent PWM modules programmable from 0.5 Hz to 2.0 kHz
- Protection for battery transient overvoltage and reversed polarity battery connection
- Configurable safe mode

- Standby mode with very low power consumption
- 10 mA open load detection in ON state
- Latch off with configurable auto retry
- Severe short-circuit and overload protection
- Programmable active current limit threshold to minimize short-circuit effect
- 12 bits ADC:
 - Current from 5.0 mA to 5.0 A with ± 6 % above 1 A
 - Voltage from 0.5 to 65 V with \pm 6.5 % above 5.0 V
 - Temperature warning for each channel plus central die monitoring
- Qualified in accordance with AEC Q100 grade 1
- Electrical transient disturbance immunity according of ISO 7637-2 and ISO 16750-2

2.3 Supported MCUs

The current implementation of the Q100 software driver is generic, such that any suitable 32 b microcontroller with SPI module and other necessary peripheries can be used. See <u>Section 2.1</u> for peripheral requirements.

Board name	MCU Board	Description
FRDM-XS2410EVB	FRDM-KL25Z	Q100 board with FRDM-KL25
FRDM-XS2410EVB	S32K144EVB-Q100	Q100 board with S32K144EVB

The driver was tested with an S32K144 MCU and S32K14x EAR SDK 0.8.6. Figure 1 shows a HW setup of S32K144EVB-Q100 and Q100 EVB.

The FRDM-XS2410EVB (Q100) evaluation board is directly compatible with the FRDM KL25Z board. See <u>Table 1</u> for used pin compatibility between FRDM-XS2410EVB (Q100) evaluation board and S32K144EVB-Q100 and FRDM KL25Z.

Table 1. Q100 EVB pin compatibility with S32K144EVB-Q100

Pin Function (Q100 EVB)	MOSI	MISO	CLK	CS	RST_B	FAULT_B	LHM	IN1	IN2	IN3	IN4
S32K144EVB-Q100	PTB4	PTB3	PTB2	PTB5	PTD13	PTB8	PTB9	PTC11	PTC10	PTB11	PTB10
FRDM KL25Z	PTD2	PTD3	PTD1	PTD0	PTA13	PTD4	PTA12	PTC9	PTC8	PTA5	PTA4

When other MCU boards or other Q100 EVB are used, refer to the provided user guides and schematics of the respective boards.



3 Q100 Extreme switch software driver

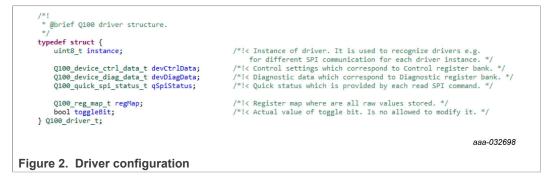
This section provides an overview of the functionality, settings and usage of the driver (configuration and functions). For additional information, see the *API Programmer's Guide* (included in the Q100 software driver zip file) and the comments embedded in the code.

The MSDI software driver consists of three files. The main functionality is contained in **Q100.c** and **Q100.h** whereas **Q100_regmap.h** contains register map of device. As the driver is not platform specific, several functions (marked as *external*in Q100.h) need to be implemented by the user.

3.1 Configuring the driver

The configuration structure shown in Figure 2 is the user interface available for configuring the driver and its behavior. The user must set appropriate Q100 device type and instance of the driver (in case more instances will be used) into the driver configuration structure ($Q100_driver_t$). The driver configuration structure is passed to all API functions of the driver as a parameter. Members qSpiStatus, regMap and toggleBit are initialized automatically in the $Q100_Init$ function.

As the driver is not platform specific, the user needs to implement several lowlevel functions. See <u>Section 3.2</u>. *Instance* member in *Q100_driver_t* structure is not modified by the driver itself. This member is passed to user-defined functions in order to differentiate between Q100 driver instances in case that more Q100 devices are connected to the MCU.



For a more detailed description of the user configuration structure, refer to the API programmer's guide.

3.2 Driver API

This Q100 software driver provides API that can be used for dynamic real-time configuration of a device in user code. For a summary of available functions, see <u>Table 2</u>. As the Q100 SW driver is platform independent, functions for SPI transfer and GPIO control need to be implemented by the user. There are helper functions that can be used for converting user-friendly float values into raw values. These values can be filled in the driver structure.

Table 2. Q100 software driver API

Table 2. Q100 software driver Al	-
Function	Description
External function	
Q100_SPI_Transfer	External defined function for SPI transfer.
SPI communications functions	
Q100_SpiWriteCtrl	Used for writing control registers via SPI
Q100_SpiReadCtrl	Used for reading control registers via SPI
Q100_SpiReadDiag	Used for reading diagnostic registers via SPI
APP control helpers configuration function	ons
Q100_UserCtrlPwmToRaw	Used for conversion user PWM (float) value to raw (uint8_t) value
Q100_RawCtrlPwmToUserVal	Used for conversion PWM raw (uint8_t) value to user (float)
Q100_UserCtrlCurrToRaw	Used for conversion user Current (float) value to raw (uint8_t) value
Q100_RawCtrlCurrToUserVal	Used for conversion Current raw (uint8_t) value to user (float) value
Q100_UserCtrlVoltToRaw	Used for conversion user Voltage (float) value to raw (uint8_t) value
Q100_RawCtrlVoltToUserVal	Used for conversion Voltage raw (uint8_t) value to user (float) value
Q100_UserCtrlTempToRaw	Used for conversion user Temperature (float) to raw (uint8_t) value
Q100_RawCtrlTempToUserVal	Used for conversion Temperature raw (uint8_t) to user (float) value
APP control configuration functions	
Q100_WriteGlobalControlSettings	Writes global control settings (reg: Q100_GLB_CTRL #00h \rightarrow Q100_READBACK #01h)
Q100_ReadGlobalControlSettings	Reads global control settings (reg: Q100_GLB_CTRL #00h → Q100_READBACK #01h)
Q100_WriteInputControlSettings	Writes input control settings (reg: Q100_OUT1_4_CTRL #02h \rightarrow Q100_IN_CTRL2 #04h)
Q100_ReadInputControlSettings	Reads input control settings (reg: Q100_OUT1_4_CTRL #02h → Q100_IN_CTRL2 #04h)
Q100_WritePwmSettings	Writes PWM control settings (reg: Q100_PWM_CTRL1 #05h → Q100_PWM_DC4 #0Fh)
Q100_ReadPwmSettings	Reads PWM control settings (reg: Q100_PWM_CTRL1 #05h → Q100_PWM_DC4 #0Fh)
Q100_WriteIrqWarningSettings	Writes interrupt and warnings configuration for SPI and FAULT_B pin (reg: Q100_EN_IRQ_SPI #10h \rightarrow Q100_EN_WARN_PIN #13h)
Q100_ReadIrqWarningSettings	Reads interrupt and warnings configuration for SPI and FAULT_B pin (reg: Q100_EN_IRQ_SPI #10h \rightarrow Q100_EN_WARN_PIN #13h)
Q100_WriteWatchdogSettings	Writes watchdog configuration (reg: Q100_WDT_REG #14h)
Q100_ReadWatchdogSettings	Reads watchdog configuration (reg: Q100_WDT_REG #14h)
Q100_WriteMeasurementsSettings	Writes measurements configuration (reg: Q100_M_SETUP #15h \rightarrow Q100_C_CTRL #16h)
Q100_ReadMeasurementsSettings	Reads measurements configuration (reg: Q100_M_SETUP #15h \rightarrow Q100_C_CTRL #16h)
Q100_WriteUnderOverCurrentSettings	Writes undercurrent and overcurrent configurations (reg: Q100_WC_CTRL #17h → Q100_UCW_OUT4 #1Fh)
Q100_ReadUnderOverCurrentSettings	Reads undercurrent and overcurrent configurations (reg: Q100_WC_CTRL #17h → Q100_UCW_OUT4 #1Fh)
Q100_WriteUnderOverVoltageSettings	Writes undervoltage and overvoltage configurations (reg: Q100_WV_CTRL #20h \rightarrow Q100_UVW_OUT4 #28h)
Q100_ReadUnderOverVoltageSettings	Reads undervoltage and overvoltage configurations (reg: Q100_WV_CTRL #20h \rightarrow Q100_UVW_OUT4 #28h)
Q100_WriteTemperatureSettings	Writes common temperature warning threshold (reg: Q100_TEMP_WT #29h)

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Table 2. Q100 software driver APIcontin	ued
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Function	Description
Q100_ReadTemperatureSettings	Reads common temperature warning threshold (reg: Q100_TEMP_WT #29h)
Q100_WriteVBATinOFFstateSettings	Writes short to VBAT in OFF state settings (reg: Q100_BV_STVB #2Ah → Q100_BT_STVB #2Bh)
Q100_ReadVBATinOFFstateSettings	Reads short to VBAT in OFF state settings (reg: Q100_BV_STVB #2Ah → Q100_BT_STVB #2Bh)
Q100_WriteOpenLoadSettings	Writes open load settings (reg: Q100_OPD_CTRL1 #2Ch → Q100_I_OLDx #31h)
Q100_ReadOpenLoadSettings	Reads open load settings (reg: Q100_OPD_CTRL1 #2Ch → Q100_I_OLDx #31h)
Q100_WriteActiveCurrentLimitSettings	Writes active current limit settings (reg: Q100_ACL_CTRL1 #32h → Q100_ACL_CTRL2 #33h)
Q100_ReadActiveCurrentLimitSettings	Reads active current limit settings (reg: Q100_ACL_CTRL1 #32h → Q100_ACL_CTRL2 #33h)
Q100_WriteSevereShortCircuitSettings	Writes severe short circuit settings (reg: Q100_SSC_CTRL #34h)
Q100_ReadSevereShortCircuitSettings	Reads severe short circuit settings (reg: Q100_SSC_CTRL #34h)
Q100_WriteOverloadProtectionSettings	Writes over load protection settings (reg: Q100_OLP_CTRL #35h → Q100_OCL_OUT4 #39h)
Q100_ReadOverloadProtectionSettings	Reads over load protection settings (reg: Q100_OLP_CTRL #35h \rightarrow Q100_OCL_OUT4 #39h)
Q100_WritePwmRegulationSettings	Writes Proportional-integral regulation compensation settings (reg: Q100_PI_CTRL1 #3Ah \rightarrow Q100_I_SET4 #3Fh)
Q100_ReadPwmRegulationSettings	Reads Proportional-integral regulation compensation settings (reg: Q100_PI_CTRL1 #3Ah \rightarrow Q100_I_SET4 #3Fh)
Q100_FillDataStructureBy	Gets settings for driver structure depend on parameter filledBy
Q100_Init	Initializes device by values stored in driver data structure
Runtime control functions	
Q100_EnableNonPwmOutput	Controls specified non-PWM output
Q100_EnablePwmOutput	Controls specified PWM output
Q100_SynchronizePwmOutputs	Synchronize all PWM outputs
APP diagnostic status functions	
Q100_ReadGlobalStatus	Reads global status from diagnostic register (Q100_GLB_STA #00h)
Q100_ReadInputOutputState	Reads input output state from diagnostic register (Q100_IN_OUT_STA #01h)
Q100_ReadChannelStatus	Reads channel status from diagnostic register (Q100_OUT1_STAx #02h \rightarrow #05h)
Q100_GetSpecificChannelStatus	Helps to find specific event in channel status register
Q100_ReadIrqStatus	Reads IRQ interrupt status from diagnostic register (Q100_ISR_IRQ #06h)
Q100_GetSpecificIrqStatus	Helps to find specific event in IRQ status register
Q100_ReadWarningStatus	Reads Warning interrupt status from diagnostic register (Q100_ISR_WARN #07h)
Q100_GetSpecificWarnStatus	Helps to find specific event in WARN status register
APP diagnostic helpers configuration fun	ctions
Q100_RawDiagCurrToUserVal	Helper conversion function from diagnostic raw Current (uint16_t) to user value (float)
Q100_RawDiagVoltToUserVal	Helper conversion function from diagnostic raw Voltage uint16_t) to user value (float)
Q100_RawDiagTempToUserVal	Helper conversion function from diagnostic raw Temperature (uint16_t) to user value (float)
Q100_RawDiagPiDutyToUserVal	Helper conversion function from diagnostic raw PI duty cycle (uint16_t) to user value (float)
Q100_RawDiagFBCurrToUserVal	Helper conversion function from diagnostic raw Feedback Current in Ton/2 (uint16_t) to user value (float)
APP diagnostic measurement functions	
Q100_ReadDiagnosticCurrent	Reads current from device diagnostic register
Q100_ReadDiagnosticVoltage	Reads voltage from device diagnostic register
Q100_ReadTemperature	Reads central temperatures from device diagnostic register
Q100_ReadPiPwmDutyCycle	Reads device duty cycle of proportional-integral controller
Q100_ReadFeedbackCurrentTon2	Reads device feedback current in Ton/2
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For a more detailed description of software driver API (function signatures, parameters) refer to the programmer's guide, included in the Q100 software driver zip file, or to the comments embedded in the Q100.h file.

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3.3 Required driver setup

In order to execute correctly, the Q100 software driver requires the following:

- 1. Fill in the driver configuration structure (Q100_driver_t).
- 2. Implement the external functions of **Q100/Q100.h**.

Moreover, the driver requires correctly pin-muxed pins and correctly initialized SPI periphery, which is handled by the external function *Q100_SPI_Transfer*.

- **SPI:** 16 bits/frame, MSB first, clock polarity: active high, clock phase: capture on the 2nd edge, active low chip select.
- SW controlled **CSB_M** chip select (if HW chip select is not possible): GPIO output pin, active low, initial value: high.
- SW controlled **RESET_B** pin, which is active in low, initial value high.

Additionally, some applications may require another set of correctly pin-muxed Q100 pins:

- FAULTB_M: Interrupt pin
- **INx:** Direct input pins for all channels

For more details refer to the provided example project.

3.4 Implementation notes

Q100 Extreme Switch SW driver is based on variables of *bool*, *uint8_t*, *uint16_t* and *float* types and requires standard *stdbool.h*, *stdint.h* and *stddef.h* libraries.

Each data received via MISO pin is parsed in order to get *QuickSpi* status flags. Fault or warning status flags are always saved into *qSpiStatus* member of the *Q100_driver_t* structure and can be read directly from the structure. There are three different SPI transfer functions, depending on R/W action on *Control register bank* and R *Diagnostic register bank*. Q100 driver automatically toggles the bit by each SPI transfer action. The user does not need to care about it.

4 Installing the software

This section describes installation of S32 Design Studio for ARM and shows how to use this SW driver with S32K144 and S32K14x SDK for application development. A process of adding the Q100 SW driver to an existing project in different IDEs or with use of different MCUs should be analogical. Most likely, the addition of a low-level SDK driver will vary.

4.1 Installing IDE

This procedure explains how to obtain and install the latest version of S32 Design Studio for ARM (2018.R1).

Note: The example in the driver package is intended for S32 Design Studio for ARM 2018.R1. If the selected IDE is already installed on the system, skip this section.

- Obtain the latest S32 Design Studio for ARM 2018.R1 installer file from the NXP website here: <u>www.nxp.com/S32DS</u>
- 2. Run the executable file and follow the instructions.

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4.2 Import an example project into IDE

The following steps show how to import an example from the downloaded zip file into S32 Design Studio for ARM.

1. In the S32 Design Studio menu bar, click **File** → **Import...** In the pop-up window, select **General** → **Existing Projects into Workspace** and click **Next**.

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ect eate new projects from an archive file or directory.		t Projects a directory to search for existing Eclip	se projects.	
elect an import source: ype filter text		ect root directory:	▼ 	Browse
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N 🏊 Run/Dehun		arch for nested projects opy projects into workspace		
	H	ide projects that already exist in the wo	orkspace	
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Ket Finish	Cancel	dd project to working sets		
45	Wor	king sets:	·	Select
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2. Click **Browse** and locate the folder where you unzipped the downloaded example files. Find the folder **S32DS_Examples** and select a project to import. Then click **OK**.

Browse For Folder		×
Select root directory of the proj	iects to import	
×	Examples Kinetis DS KL25 MCUXpresso KL25 S32 DS S32K144 Q100_direct_input Q100_freemaster_eSwitch Q100_irrq_warn Q100_pwm_control	~
<u>E</u> older: S32 DS S32K144 <u>M</u> ake New Folder	OK Cancel	
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3. With your project now loaded in the **Select root directory** box, click on the **Copy projects into workspace** checkbox. Then click **Finish**. The project is now in the S32 Design Studio workspace where you can build and run it.

NP Import	□ ×	Project Explorer 🙁 🗖 🗖
Import Projects Select a directory to search for existing Eclipse projects.		⊂ ⊊ ▽ ✓ <mark>⊘ Q100_direct_input: Debug</mark>
Select root directory: C:\PROJECTS\Q100\outputs\4. Execut Select archive file: Projects: Q100_direct_input (C:\PROJECTS\Q100\outputs\4. Executio Q100_freemaster_eSwitch (C:\PROJECTS\Q100\outputs\4. Executio) Q100_irq_warn (C:\PROJECTS\Q100\outputs\4. Executio) Q100_pwm_control (C:\PROJECTS\Q100\outputs\4. Executio) Q100_pwm_cot	Browse Browse Select All Deselect All Refresh	 > Signaries > Includes > Generated_Code > Project_Settings > SDK > SOK > Sources > Q100 > A Q100_regmap.h > Q100.c > A Q100.h > C main.c > M clude
Working sets Add project to working sets Working sets: Image: Set of the se	New Sglect	

4.3 Creating a new project with an MSDI software driver

If you choose not to use the example project, the following instructions describe how to create and set up a new project for S32K144 MCU that uses the MSDI SW driver.

To create a new project in S32 Design Studio for ARM, do the following:

1. In the S32 Design Studio menu bar, select File \rightarrow New \rightarrow S32DS Application Project.

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	New				Alt	+Shift+N>	C.	Makefile Project with Existing Code	
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	1 bcc.h [BC	C_S32K144_M	C33771_SPI_	Free]					
	2 bcc.c [BC	C_\$32K144_M	onitoring_Di	agn]					
	3 bcc.h [BC	C_S32K144_M	onitoring_D	iagn]					
	4 diagnostic	s.c [BCC_S32	K144_Monit	ori]					
	Exit								aaa-032702

2. When the S32DS Application Project box opens, enter a project name into the text box, choose S32K144 processor in the *Processors* tab, Standard S32DS toolchain for ARM in *ToolChain Selection* and click Next.

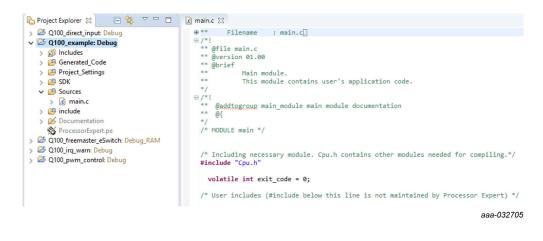
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3. Select NewLib Nano library, S32K144_SDK (version 0.8.6) SDK and click Finish.

S32DS Application Project						×
New S32DS Project for S32	(144					
Select required cores and para	meters for them.					
Project Name	Q100_example					
Core	Cortex-M4F					
Library	NewLib Nano					\sim
I/O Support	No I/O					~
FPU Support	Toolchain Default					~
Language	С					~
SDKs	S32K144_SDK_gcc					
Debugger	PE Micro GDB server					~
?		< <u>B</u> ack	Next >	<u>F</u> inish	Can	cel

4. The Project Explorer panel and a part of the **main.c** content after creation of new project is shown. This project includes only startup code and minimal driver set from S32K144 SDK.



4.3.1 Adding the Q100 eSwitch software driver to the project

This section describes how to add the Q100 software driver to the project.

1. Copy the content of **SDK_SW_Driver** to the **Sources** folder in your newly created project as shown.

🎦 Project Explorer 🐹 🛛 🖻 🔄 🗸
> 😂 Q100_direct_input: Debug
✓ [™] Q100_example: Debug
> 🔊 Includes
> 😕 Generated_Code
> 😕 Project_Settings
> 🔑 SDK
✓ 29 Sources
🗸 🔁 Q100
> h Q100_regmap.h
> 尾 Q100.c
> h Q100.h
> 尾 main.c
> 😂 include
> 📂 Documentation
💥 ProcessorExpert.pe
> 2 Q100_freemaster_eSwitch: Debug_RAM
> 😂 Q100_irq_warn: Debug
> 😂 Q100_pwm_control: Debug
aaa-032706

2. Include the *Q100.h* header file in **main.c** in order to get access to the Q100 software driver in the user code.

<pre>/* Including necessary module. Cpu.h contains other modules needed for compi #include "Cpu.h"</pre>	ling.*/
<pre>volatile int exit_code = 0;</pre>	
<pre>/* User includes (#include below this line is not maintained by Processor Ex #include "Q100/Q100.h"</pre>	pert) */
<pre>/*! \brief The main function for the project. \details The startup initialization sequence is the following:</pre>	aaa-032707

4.3.2 Setting up the project

Once the new project has been created and the Q100 software driver has been added into it, the project must be set up.

 In order to implement the platform specific (external) functions of the Q100 software driver, LPSPI and GPIO S32K14x SDK drivers are required. GPIO driver is already attached to the project. In order to generate the LPSPI driver into the project, click twice on the **Ipspi** component in **Components Library** window. If the **Components Library** window is hidden, open it by clicking **Processor Expert** → **Show Views**. When the Ipspi component is included in the PEx file, it is shown in the **Components** window.

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	All repositories	✓ Applicable to project ✓		 > Generator_Configurations > OSs
mponent	Component Repository	Description	^	Processors Processor
쭝 LinStack	SDK_S32K14x_09	S32 SDK Middleware for Local Interconnect Network Stack (LIN Stack)		V > Components
@ lpi2c	SDK_S32K14x_09	S32 SDK Peripheral Driver for Low Power Inter-Integrated Circuit (LPI2C)		> Referenced_Components
(D) Ipit	SDK_S32K14x_09	S32 SDK Peripheral Driver for Low Power Interrupt Timer (LPIT)		> 💮 pin_mux:PinSettings
🕝 lpspi	SDK S32K14x 09	S32 SDK Peripheral Driver for Low Power Serial Peripheral Interface (LPSPI)		> 🛐 clockMan1:clock manager
Component level: High Component level: High mpu_pal oc_pal osif pdb phy phy physettings	SDK_532K14x_09 SDK_532K14x_09 SDK_532K14x_09 SDK_532K14x_09 SDK_532K14x_09 SDK_532K14x_09 SDK_532K14x_09	face (IL-PPI) (IX Peripheral Driver for Low Power Timer (Iptm))) ∰ intMan 1anterrupt manager > @ IpspiCom13pspi
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2. In order to get the Q100 software driver to run on S32K144, the **PinSettings** component must be edited to configure the LPSPI and GPIO pins being used and the RESET_B signal. This entails making the correct MCU pin selections and then muxing them as needed. See <u>Section 2.3</u>. The following image is an example of LPSPI0 pin muxing. You should also set the correct GPIO pin directions and initial values in the **PinSettings** component.

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outing Functional Prope	erties Methods Se	ttings		
View Mode	Options			Generate Report
Collapsed OPins	Show Only Co	onfigurable Signals		HTML Report
ADC CAN CMP	EWM ELEXIO	FTM GPIO JTAG LPI2C LPS	PI = LPTMR = LPUART = Platform =	PowerAndGround RTC SWD TRGMUX
Signals		Pin/Signal Selection	Direction	Selected Pin/Signal Name
V LPSPI0				
Peripheral Chip Sel	ect 0	PTB5	Output	PTB5
Peripheral Chip Sel	ect 1	No pin routed	No pin routed	
Peripheral Chip Sel	ect 2	No pin routed	No pin routed	
Peripheral Chip Sel	ect 3	No pin routed	No pin routed	
Serial Clock		PTB2	Output	PTB2
Serial Data Input		PTB3	Input	PTB3
Serial Data Output		PTB4	Output	PTB4
✓ LPSPI1				
Peripheral Chip Sel	ect 0	No pin routed	No pin routed	
Peripheral Chip Sel	ect 1	No pin routed	No pin routed	
Peripheral Chip Sel	ect 2	No pin routed	No pin routed	
Peripheral Chip Sel	act 3	No pin routed	No pin routed	~

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- 3. In order to get the Q100 software driver to run on an S32K144, check the **clock_manager** component settings for the following:
 - The peripheral clock to LPSPI and PORT peripheries must be enabled AND
 - The frequency for theses peripheries must be in the allowed range

	clockMan1							
component version S	32K144_SDK01							
Clock Config Callba	acks Shared co	mponents Inherite	ed components					
Clock configurations	- 1	+ ^ v						
# Clock configu	ration							
0 clockMan1_In								
Details for selected r								
Clock configuration	n 0							
			PO) SIM) TCLK) Trad	re Clock Va	lues Summ	arv		
Settings SIRC FI	IRC RTC SOSC) SPLL) CLKOUT) LE	PO SIM TCLK Trad	ce Clock Va	lues Summ	ary		
	IRC RTC SOSC	SPLL CLKOUT L	PO SIM TCLK Trac	ce Clock Va	ilues Summ	ary		
Settings SIRC FI	IRC RTC SOSC		PO SIM TCLK Trac		lues Summ Divide	ary Frequency		
Settings SIRC Fi	IRC] RTC] SOSC						^	
Settings SIRC FI Peripheral Clocks Clock Name	IRC] RTC] SOSC	Interface Clock	Functional Clock			Frequency	A	
Settings SIRC FI Peripheral Clocks Clock Name FTM3_CLK	IRC] RTC] SOSC	Interface Clock	Functional Clock SIRCDIV1_CLK			Frequency 0-Hz		
Settings SIRC FJ Peripheral Clocks Clock Name FTM3_CLK LPI2C0_CLK	IRC] RTC] SOSC	Interface Clock SYS_CLK BUS_CLK	Functional Clock SIRCDIV1_CLK SIRCDIV2_CLK			Frequency 0 Hz 0 Hz	•	
Settings SIRC FI Peripheral Clocks Clock Name FTM3_CLK LPI2C0_CLK LPITO CLK	IRC RTC SOSC	Interface Clock SYS_CLK BUS_CLK BUS_CLK	Functional Clock SIRCDIV1_CLK SIRCDIV2_CLK SIRCDIV2_CLK			Frequency 0 Hz 0 Hz 0 Hz	•	
Settings SIRC FI Peripheral Clocks Clock Name FTM3_CLK LPI2C0_CLK LPITO CLK LPSPI0_CLK	IRC RTC SOSC	Interface Clock SYS_CLK BUS_CLK BUS_CLK BUS_CLK	Functional Clock SIRCDIV1_CLK SIRCDIV2_CLK SIRCDIV2_CLK SIRCDIV2_CLK			Frequency 0 Hz 0 Hz 0 Hz 8 MHz	Ē	
Settings SIRC FI Peripheral Clocks Clock Name FTM3_CLK LPI2C0_CLK LPITO CLK LPSPI0_CLK LPSPI1_CLK	IRC RTC SOSC	Interface Clock SYS_CLK BUS_CLK BUS_CLK BUS_CLK BUS_CLK	Functional Clock SIRCDIV1_CLK SIRCDIV2_CLK SIRCDIV2_CLK SIRCDIV2_CLK SIRCDIV2_CLK			Frequency 0-Hz 0-Hz 0-Hz 8 MHz 8 MHz	Ē	

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4. In the Components window, click the Generate Processor Expert Code icon to generate the component settings into the Generated_Code folder. In order to set the clock configuration and mux the pins according to the settings generated from the Processor Expert components, add the following lines to the beginning of the main() function:

CLOCK_SYS_Init(g_clockManConfigsArr, CLOCK_MANAGER_CONFIG_CNT, g clockManCallbacksArr, CLOCK MANAGER CALLBACK CNT);

CLOCK_SYS_UpdateConfiguration(0U, CLOCK_MANAGER_POLICY_FORCIBLE); PINS DRV Init(NUM OF CONFIGURED PINS, g pin mux InitConfigArr);

- 5. Create a variable of type Q100_driver_t that will be passed to all used functions. This variable stores Q100 software driver configuration and its internal data. This variable must be accessible during run time and should be declared either in the main() function or as a global variable.
- 6. Configure the Q100 as shown. You may change all individual items as needed.

	main(void)
{	<pre>lpspi_state_t lpspiState; lpuart_state_t lpUartState;</pre>
	/* Main driver structure where are all configurations stored. */ Q100_driver_t q100Drv; Q100 driver structure
	<pre>/*** Processor Expert internal initialization. DON'T REMOVE THIS CODE!!! ***/ #ifdef PEX_RTOS_INIT PEX_RTOS_INIT();</pre>
	/*** End of Processor Expert internal initialization. ***/
	<pre>/* Initialization of board. */ CLOCK_SYS_Init(g_clockManConfigsArr, CLOCK_MANAGER_CONFIG_CNT,</pre>
	PINS_DRV_Init(NUM_OF_CONFIGURED_PINS, g_pin_mux_InitConfigArr); SPI Initialization
	<pre>/* Initialization of SPI instance 0. In this example is only one device and SPI used. */ LPSPI_DRV_MasterInit(Q100_SPI_INSTACE, lpspiState , &lpspiCom1_MasterConfig0);</pre>
9	<pre>/* Next configure peripheral delay between active level of chip select signal and clock. * Next delay between CLK and de-active CS signal.*/ LPSPI_DRV_MasterSetDelay(Q100_SPI_INSTACE, 5, 5, 5);</pre>
9	<pre>/* Filling driver data structure by default values, disabled * transition to save mode if <u>watchdog</u> timeout event occur. */ Q100_FillDataStructureBy(Q100_INSTAMCE_0, &q100Drv, Q100_DEFAULT_SETTINGS, false);</pre>
	<pre>/* Reset device. */ Default structure configuration PINS_DRV_ClearPins(Q100_RSTB_PORT, (1 << Q100_RSTB_PIN)); OSIF_TimeDelay(1); /* Activate device. */ PINS_DRV_SetPins(Q100_RSTB_PORT, (1 << Q100_RSTB_PIN)); OSIF_TimeDelay(1); User drv config modification</pre>
L	<pre>q100Drv.devCtrlData.wtchdgConf.enable = false;</pre>
	<pre>q100Drv.devCtrlData.unOvVoltConf.overVoltage[Q100_CHANNEL_0] = Q100_UserCtrlVoltToRaw(15.5);</pre>
	<pre>/* Initialize device by configuration stored in driver structure. */ Q100_Init(&q100Drv);</pre>
	Initialization of Q100 device with driver data configurations

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- 7. Set up the LPSPI peripherals that will be used by the Q100 software driver. The easiest way is to set the LPSPI configuration in the **Ipspi** Processor Expert component. After clicking the **Generate Processor Expert Code** icon, the Ipspi configuration is generated in the Generated_Code folder. This configuration can be passed as a parameter of *LPSPI_DRV_MasterInit* SDK function in **main()**. In addition, it is recommended to set the Chip Select To Clock Delay (CSTCD) configuration and Delay Between Frames (DBF) configuration by LPSPI_DRV_MasterSetDelay when using the HW chip select.
- 8. The Q100 initialization function should be called. User must pass reference to driver configuration structure.

9. Except for the peripheral and Q100 initialization function, the external function (listed in Q100.h and <u>Table 2</u>) used by Q100 driver need to be implemented. See the *S32 DS S32K144* folder in the provided example project as a template of its implementation for S32K144.

4.3.3 Writing your application code

All of your application code must reside in the **Sources** folder in your project directory. You may modify the code in **main.c** but you must retain the original comments related to usage directions.

When the Q100 SW Driver and utilized peripherals are configured properly and external functions are implemented, you can use all of the prepared API functions to construct your own application.

See the *API Programmer's Guide* (included in the Q100 software driver zip file) for function signatures and required parameters. Also review the **Q100.h** headerfile, which contains prototypes and explanation for all available functions.

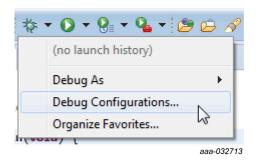
4.3.4 Compiling, downloading and debugging

To compile a project, click the compile icon in the toolbar.



The process for downloading an application on board in S32 Design Studio for ARM may differ according to used MCU board. If you have any question, please see S32 Design Studio for ARM user's guide. To download and debug on S32K144EVB-Q100 MCU board, do the following:

1. Click the arrow next to the debug icon in the toolbar and select **Debug Configurations...**.



- 2. In the **Debug Configurations** dialog box, select one of the existing configurations with a project name under **GDB PEMicro Interface Debugging**.
- 3. Make sure that the **C/C++ Application** contains a path to the .elf file of the project in the **Main** tab of the Debug Configuration window.
- 4. Pick up proper **debug interface** and **USB port** in the **Debugger** tab of Debug Configuration window.

5. Apply changes and then click **Debug**. S32 Design Studio for ARM will download and launch the program on board.

5 References

[1]	FRDM-XS2410EVB	Product Summary Page	http://www.nxp.com/FRDM-XS2410EVB
[2]	Q100 eSwitch software driver	Tool Summary Page	http://www.nxp.com/Q100-ESWITCH-DRIVER
[3]	S32 Design Studio IDE	Tool Summary Page	http://www.nxp.com/S32DS

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Q100 (MC33XS2410) Extreme switch software driver user guide

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