Three-phase PMSM Pump Reference Design Hardware User Guide

Rev. 0 — 26 July 2022

User guide

# 1 Introduction

This user guide describes three-phase Permanent Magnet Synchronous Motor (PMSM) pump reference design optimized for the HVP-MC3PH-LITE hardware equipped with Kinetis V series MCU. The aim of the reference design is help to customers develop motor-control solutions with safety features intended for controlled heating systems, electric circulation pumps, service water installation, and other devices used in industrial applications. The HVP-MC3PH-LITE reference design is targeted for the circular pump application sector, but it can be reused for general three-phase motor-control applications of up to 60 W with the AC supply from 110 V to 230 V. This reference design uses the NXP cost-optimized MCU MKV10Z32 with core M0+ and NXP high-voltage DC-DC converter TEA1721. In reference design there is implemented integrated 3-phase power module, inrush circuit, and single-shunt current sensing with or without an op amp. You can reuse the design reference manual, schematics, firmware, and manufacturing files to speed up the product design. Specific EMC filters of the AC input were not considered in this design, only the "Y" caps at the input stage.

The document consists of several parts. The first part describes the high-level hardware view. The following parts describe the particular schematic modules. The last parts focus on the control and debug interface.



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# 2 Hardware

The three-phase PMSM pump reference hardware is designed on a four-layer PCB. It consists of the power stage, control unit, and debug interface. The power stage contains the discrete input rectifier, integrated inverter power module, and power-supply block. The control unit contains the MCU and the analog sensing block. The debug interface is decoupled in a hierarchical view due to safety reasons. Use an external isolator for the debug interface. There is high voltage on the board, even when the power is off.



Figure 1. HVP3PH\_LITE block diagram

**CAUTION:** The board has high voltage, do not touch the board. For evaluation, flashing, and debugging of the application, use an external SWD isolator. It is recommended to use the J-Link JTAG isolator, which can be connected between the J-Link and any Arm board that uses the standard 10-pin JTAG-ARM connector to provide electrical isolation (1 kV DC).

### 2.1 Hierarchical block

The hierarchical block of the schematic page shows the real interconnection between blocks and all available inputs and outputs. The high-voltage AC input supports both 230 V / 110 V AC on J1. The serial-wire debug interface is available on J2. The 3.3-V supply for an external isolator is available on pin 1. Jumper J3 is intended for auxiliary purposes of 15 V or 3.3 V on J4. Consider the total board current consumption with the supplying isolator of the debug interface not to overload the 5-W high-voltage DC-DC converter. The three-phase motor can be connected to J5. The medium temp sensor (type PT1000) can be connected to J6. The medium temperature interface and the bias voltage were realized in the simplest form. J7 is an interface isolated by an optocoupler. The PWM input sets the optional speed setpoint of the pump. The signal expected on the input is a PWM with an amplitude of roughly 10 V. The PWM duty evaluation is polarity-dependent. At the A(1) pin, the positive duty cycle is measured. The following chapters describe each block and the details of the schematic.

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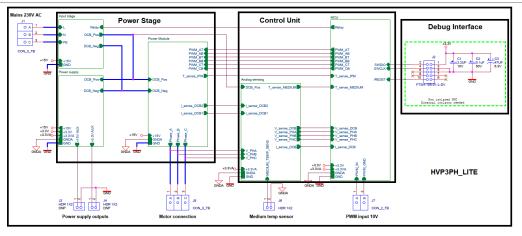
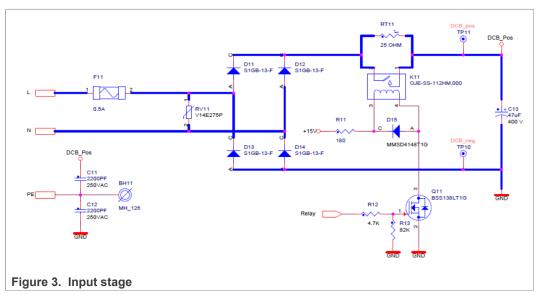


Figure 2. HVP3PH\_LITE block diagram

# 2.2 Input stage

This stage consist of input fuse F11, varistor overvoltage protection RV11, rectifier D11-D14, inrush protection circuit, and the main DC-Bus capacitor. Minimal EMI reduction is done using two Y caps (C11 and C12, 2200 pF) connected to the DC-Bus potential and the GND to protective earth or pump conducting chassis.



The input miniature slow fuse F11 (500 mA) is dimensioned in consideration of expected device operating current and inrush circuit capability.

The parameters of discrete rectifier with S1GB-13-F diodes are as follows:

- Vrrm is 400 V.
- lavg is 1 A.
- Surge peak is 30 A.

An inrush-limiting circuit is at the DC-Bus. A thermistor limits the inrush current to a safe level, which does not burn the input fuse. The K11 relay is controlled by the MCU. This relay is designed for 12 V operation. The R11 voltage drop helps to work on 15-V supply.

Relay contacts override the thermistor to prevent its overheating. The thermistor is ready for the following inrush action without any delay.

The parameters of the OJE-SS112HM relay are as follows:

- The current switching is 7.5 A.
- The voltage is 240 V AC.
- The V coil is rated at 12 V.
- The V coil operates at 9 V.

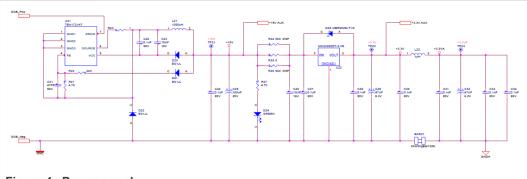
The main DC-bus capacitor (C13) value is chosen as a compromise between size and rectified voltage ripple. The voltage ripple can be compensated in the motor-control software.

**Attention:** There is high voltage on the board. Do not touch the board. The board is for evaluation purposes only. The DC-Bus capacitors are still charged when the device is not supplied.

### 2.3 Power supply

custom purposes.

This stage steps down the DC-Bus high voltage to 15 V and then to 3.3 V. The TEA1721 cost-optimised IC for 5-W applications is used as a converter from 325 V to 15 V. In our case, it is used in connection as a non-isolated DC-DC converter. The output voltage is set by the R21 and R22 dividers. This IC has many options. For details, see <a href="https://www.nxp.com/products/power-management/ac-dc-solutions/ac-dc-controllers-with-integrated-power-switch/hv-start-up-flyback-controller-with-integrated-mosfet-for-5-w-applications-fburst-430-hz:TEA1721AT and the TEA1721 application note demo board at <a href="https://www.nxp.com/products/power-management/ac-dc-solutions/ac-dc-controllers-with-integrated-power-switch/hv-start-up-flyback-controller-with-integrated-mosfet-for-5-w-applications-fburst-430-hz:TEA1721AT and the TEA1721 application note demo board at <a href="https://www.nxp.com/products/power-management/ac-dc-solutions/ac-dc-controllers-with-integrated-power-swith-integrated-power-solutions/ac-dc-controllers-with-integrated-power-swith-integrated-mosfet-for-5-w-applications-fburst-430-hz:TEA1721AT and the TEA1721 application note demo board at <a href="https://www.nxp.com/products/power-management/ac-dc-solutions/ac-dc-controllers-with-integrated-pc/tea1721-non-isolated-buck-boost-converter-demo-board:TEA1721ADB1060">https://www.nxp.com/products/power-management/ac-dc-solutions/ac-dc-controllers-with-integrated-pc/tea1721-non-isolated-buck-boost-converter-demo-board:TEA1721ADB1060</a>.



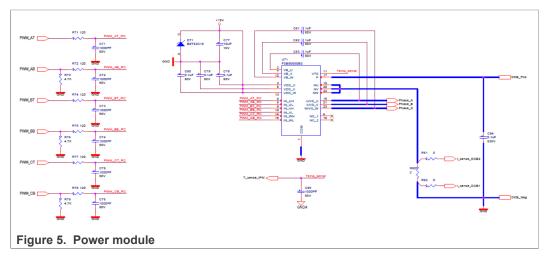
**Figure 4.** Power supply The 3.3-V regulator IC is of a classic linear type. A bigger case is capable to dissipate the power caused by a voltage drop. If the application works at a high ambient temperature, the R24, R25, and R26 input resistors help to and decrease the input voltage of the regulator and dissipate some power. In the default configuration, R24 and R26 are not populated and R25 is zero. A switching regulator could be considered here in a custom redesign. The analog and digital 3.3-V domains are decoupled by the L22 inductance and blocking capacitors on both sides. Both grounds are connected in the defined place by a shorting bar. The 15-V and 3.3-V domains are available as auxiliary on headers for

### 2.4 Power module

The selected FSB50650BS IPM (Integrated Power Module) fits the intended circular pump application. It is optimized for switching frequencies of over 10 kHz with built-in bootstrap diodes.

- Idrms is 1.8 A.
- Vdds is 500 V.

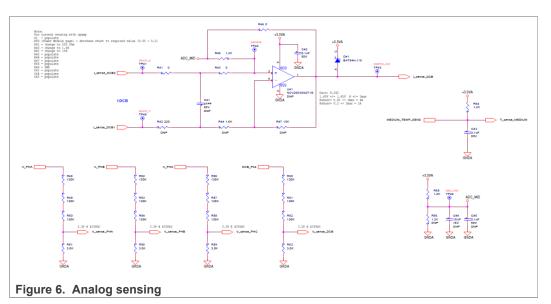
The power module temperature measurement protects the module in case of an overload and high ambient temperatures. The cost-optimised single shunt current sensing is realized in this design. The current reconstruction is described in the software design manual. In the default configuration, the value of the shunt resistor is designed to operate without an op amp. The PWM filters can smooth any glitches or HF disturbances. The pull-down resistors ensure that the low-side transistors are switched off when the PWM pins are not initialized. An additional high-voltage DC-Bus capacitor is intended to be close to the module pins.



### 2.5 Analog sensing

This reference design uses single-shunt current sensing. The default configuration uses a  $2-\Omega$  shunt value together with a passive bias circuit to operate without an op amp.





For operation without an op amp with a 2- $\Omega$  shunt value, the current scale is 1.65 A. The usable range is up to 500 mA not to burn the driver and the shunt resistor. With default components and op amp enablement, the current scale is 1 A for a 0.2- $\Omega$  shunt resistor and 4 A for a 0.05- $\Omega$  shunt resistor.

The midpoint of 1.65 is important for safety purposes. It is used for for both configurations (with/without an op amp). The voltage dividers for phase voltages and the DC-Bus voltage are identical with the scale of 433 V DC. The analog sensing block provides an optional input for the external temperature sensor (e.g. medium, water). The sensor interface and measurement is realized in the simplest form and designed for the PT1000 temperature sensor. In case of a different temperature sensing, redesign it accordingly.

### 2.6 MCU

A circular pump is a cost-sensitive design, so the MCU is selected accordingly.

The MCU parameters are as follows:

- 48-pin LQFP package
- Up to 75-MHz Arm Cortex-M0+ core

The memories and memory interfaces are as follows:

- 32 kB of program flash memory
- Up to 8 kB of RAM

The system peripherals are as follows:

- Nine low-power modes to provide power optimization based on application requirements
- 4-channel DMA controller
- SWD interface and micro trace buffer
- Bit Manipulation Engine (BME)
- External watchdog timer
- Advanced independent clocked watchdog
- Memory Mapped Divide and Square Root (MMDVSQ) module

The clocks are as follows:

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- 32 kHz to 40 kHz or 3 MHz to 32 MHz crystal oscillator
- Multipurpose Clock Generator (MCG) with frequency locked loop referencing either internal or external reference clocks

The security and integrity modules are as follows:

- 80-bit unique identification (ID) number per chip
- Hardware CRC module

The communication interfaces are as follows:

- One 16-bit SPI module
- One I2C module
- Two UART modules

The timers are as follows:

- One programmable delay block
- One 6-channel FlexTimer (FTM) for motor-control/general-purpose applications
- Two 2-channel FlexTimers (FTM) with quadrature decoder functionality
- 16-bit Low-Power Timer (LPTMR)

The operating characteristics are as follows:

- Voltage range: from 1.71 V to 3.6 V
- Flash write voltage range: from 1.71 V to 3.6 V
- Temperature range (ambient): from -40 °C to 105 °C

The analog modules are as follows:

- Two 16-bit SAR ADCs
- 12-bit DAC
- Analog Comparator (CMP) containing a 6-bit DAC and a programmable reference input

The human-machine interface is as follows:

• General-purpose I/O

The following pin mux table summarizes all pins of the MCU with dedicated function and signal descriptions.

Table	1.	Pin	mux	overview
Table			IIIUA	046141644

Pin number	Pin name	Function	Signal/connection
1	VDD1	VDD1	3.3 V
2	VSS1	VSS1	GND
3	PTE16	ADC0 SE1	vphb_rc
4	PTE17	ADC0 SE5	vphc_rc
5	PTE18	ADC0 SE6	vpha_rc
6	PTE19	GPIO in	GND
7	PTE20	FTM1 CH0	pwm_in_mcu
8	PTE21	FTM1 CH1	pwm_in_mcu
9	VDDA	VDDA	3.3 VA
10	VREFH	VREFH	3.3 VA
11	VREFL	VREFL	GNDA

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in number	Pin name	Function	Signal/connection
12	VSSA	VSSA	GNDA
13	PTE29	CMP IN5	ipm_temp_rc
14	PTE30	DAC0 OUT	TP119
15	PTE24	FTM0 CH0	PWM_AT
16	PTE25	GPIO out	Relay
17	PTA0	SWD CLK	SWCLK
18	PTA1	GPIO out	LED
19	PTA2	GPIO	TP117
20	PTA3	SWD DIO	SWDIO
21	PTA4	/NMI	3.3 V
22	VDD2	VDD2	3.3 V
23	VSS2	VSS2	GND
24	PTA18	GPIO in	GND
25	PTA19	GPIO in	GND
26	PTA20	/RESET	/RESET
27	PTB0	ADC0 ADC1 SE8	idcb_rc
28	PTB1	ADC0 ADC1 SE9	ipm_temp_rc
29	PTB2	ADC0 ADC1 SE10	vdcb_rc
30	PTB3	ADC1 SE2	medium_temp_rc
31	PTB16	GPIO in	GND
32	PTB17	GPIO in	GND
		GPIO out	
33	PTC0	CMP0 out	TP116
34	PTC1	GPIO in	GND
35	PTC2	GPIO in	GND
36	PTC3	GPIO in	GND
37	PTC4	FTM0 CH3	PWM_BB
38	PTC5	FTM0 CH2	PWM_BT
39	PTC6	CMP0 IN0	idcb_rc
40	PTC7	GPIO in	GND
41	PTD0	GPIO out	TP118
42	PTD1	ADC0 SE0	medium_temp_rc
43	PTD2	GPIO in	GND
44	PTD3	GPIO in	GND
45	PTD4	FTM0 CH4	PWM_CT
46	PTD5	FTM0 CH5	PWM_CB

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Table 1. Pin mux overviewcontinued	I
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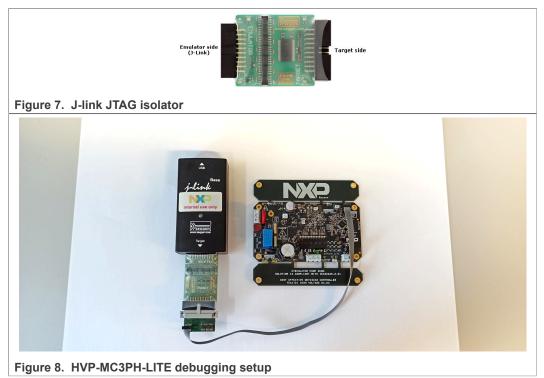
Pin n	umber	Pin name	Function	Signal/connection
4	17	PTD6	GPIO in	GND
4	18	PTD7	FTM0 CH1	PWM_AB

### 2.7 PWM input interface

The motor setpoint can be done using the FreeMASTER real-time debugger or a PWM duty on the PWM input. The expected PWM amplitude is roughly 10 V. The expected detectable frequency of the PWM is from 500 Hz to 2000 Hz. See the Three-phase PMSM Pump Reference Safety Software Design User Guide (document <u>PMSMSAFEUG</u>) for details.

### 2.8 SWD interface

This interface is realized by a miniature 10-pin header connector. The J-link (for example, J-link Base) interfaces are also supported. For flashing and debugging of this board, you must use an external isolator. The recommended solution is the J-Link JTAG isolator, which provides basic 1-kV isolation (<u>https://www.segger.com/products/debug-probes/j-link/accessories/isolators/j-link-jtag-isolator/</u>).



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#### Three-phase PMSM Pump Reference Design Hardware User Guide

# 3 Useful links

[1] Three-phase PMSM Pump Reference Safety Software Design User Guide (document <u>PMSMSAFEUG</u>)

[2] Sensorless PMSM Field-Oriented Control (document DRM148)

[3] MCUXpresso SDK for Motor Control

[4] MKV10Z32 MCU

- [5] TEA1721AT DC-DC converter
- [6] FSB50650BS integrated power module

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# **Revision history**

Revision history			
Revision number Date Substantive		Substantive changes	
0	26 July 2022	Initial release.	

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