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P2020RDB-PCA Specification

QorIQ Integrated Communications Processor

The reference design board (RDB) is a system featuring the P2020E QorIQ processor, which includes a built-in security accelerator. This low-cost, high-performance system solution consists of a printed circuit board (PCB) assembly, and a software board support package (BSP). This BSP enables the fastest possible time-to-market for development or integration of applications including printer engines, broadband gateways, no-new-wires home adapters/access points, and home automation boxes.

This document describes the hardware features of the board including specifications, block diagram, connectors, interfaces, and hardware straps. It also describes the board settings and physical connections needed to boot the RDB. Finally, it considers the software shipped with the platform.

When you finish reading this document, you should be familiar with:

- Board layout and its interfaces
- Board configuration options
- How to get started and boot the board

Contents

This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice.

1 Introduction

This document is applicable for PCBA Rev4.0 and PLD Rev4.2. The revision information is shown in the log file of board booting.

1.1 Acronyms and Abbreviations

Table 1 lists commonly used acronyms and abbreviations.

Table 1. Acronyms and Abbreviations

COP	Debug Port in Powerpc	**PHY**	Physical Layer Interface Device
DDR	Double Data Rate DRAM	**PLL**	Phase Lock Loop
LYNX	High Speed Serial Interface	**SERDES**	Serializer/Deserializer
PCIe	PCI Express®	**USB**	Universal Serial Bus

1.2 Reference Documents

The following documents are available on Freescale's intranet library.

- P2020E QorIQ Integrated Processor Family Reference Manual
- P2020E QorIQ Integrated Processor Hardware Specification

2 P2020RDB Hardware

This section covers the features, block diagram, specifications, and mechanical data of the RDB.

2.1 P2020E Features

The board features are as follows:

- P2020E running at1.2 GHz, platform 600 MHz and DDR3 800 MHz
- Memory subsystem:
  - 1 Gbyte unbuffered DDR3 SDRAM discrete devices (64-bit bus)
  - 16 Mbyte flash single-chip memory
  - 128 Mbyte NAND flash memory
  - 256 Kbit M24256 I2C EEPROM
  - 16 Mbyte SPI memory
  - SD connector to interface with the SD memory card
- Interfaces:
  - PCIe
    - x1 PCIe slot or x1 PCIe to dual SATA controller
    - x1 mini-PCIe slot
  - 10/100/1000 BaseT Ethernet ports:

    - eTSEC1, RGMII: four 10/100/1000 ports using Vitesse™ VSC7385 L2 switch
    - eTSEC2, SGMII: one 10/100/1000 port using Vitesse™ VSC8221
    - eTSEC3, RGMII: one 10/100/1000 port Atheros™ AR8021
  - USB 2.0 port:
    - ULPI PHY interface: SMSC USB3300 USB PHY and Genesys Logic's GL850A USB2.0 HUB Controller with 4 downstream ports
    - Two USB2.0 Type A receptacles
    - One USB2.0 signal to Mini PCIe slot
  - Dual RJ45 UART ports:
    - DUART interface: supports two UARTs up to 115200 bps for console display
- Board connectors:
  - Open frame power supply connector
  - JTAG/COP for debugging
- IEEE Std. 1588™ signals for test and measurement
- Real-time clock on I^2C bus
- PCB
  - 6-layer routing (4-layer signals, 2-layer power and ground)

Figure 1 shows the P2020RDB block diagram.

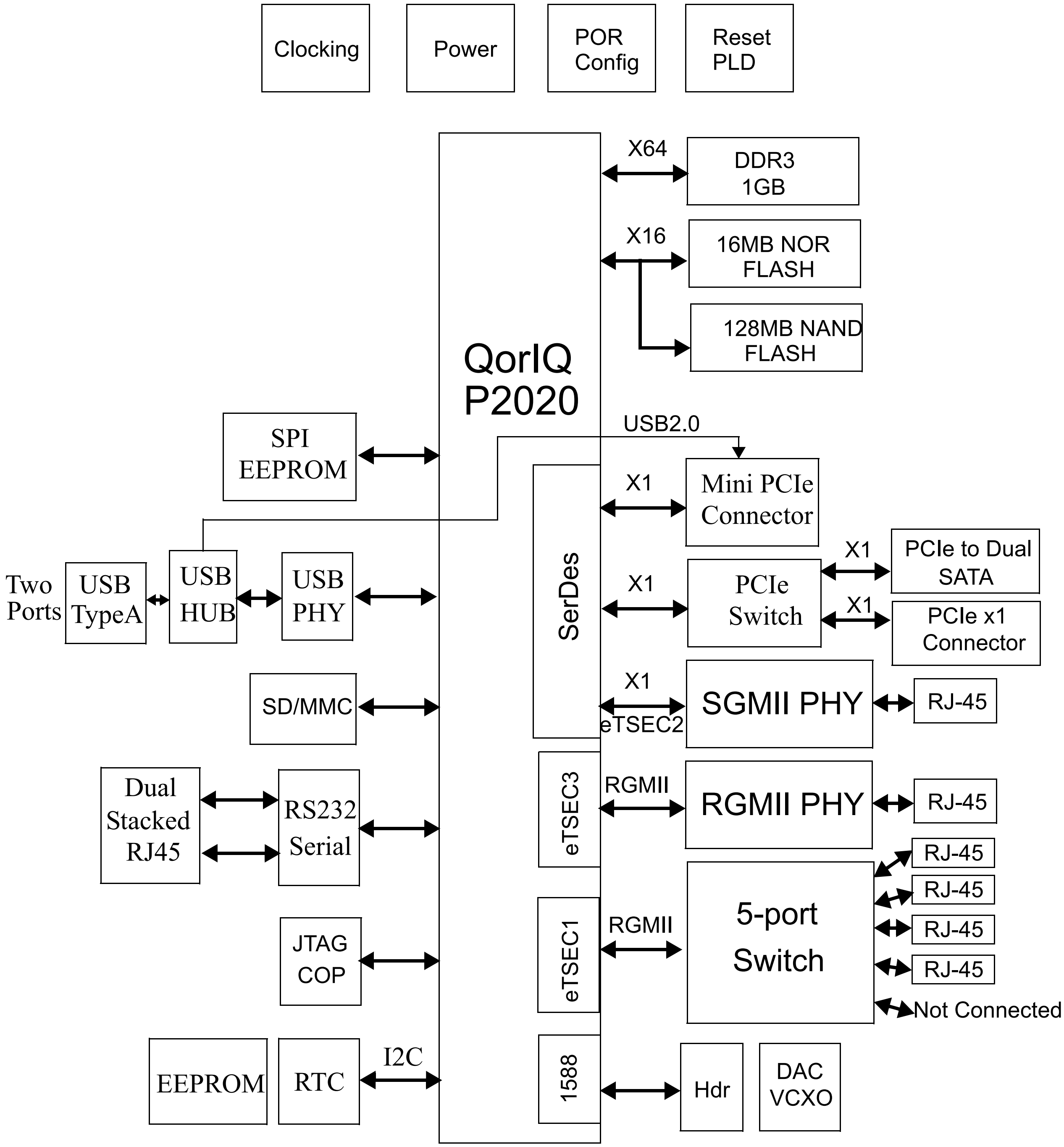

Figure 1. Block Diagram

2.2 Specifications

Table 2 lists the specifications of the P2020RDB.

Table 2. RDB Specifications

Characteristics	Specifications
Chassis Power requirements	**Typical Maximum** 40W 90~264VAC input open frame power supply
Communication processor	P2020E cores running at 1.2 GHz
Operating temperature	0^{o} C to 70^{o} C (room temperature)
Storage temperature	–25^{o}C to 85^{o}C
Relative humidity	5% to 90% (noncondensing)
PCB dimensions: Length Width Thickness	 8860 mil 8270 mil 62 mil

2.3 Mechanical Data

Figure 2 shows the P2020RDB dimensions. The board measures 225 mm × 210 mm (8860 mil × 8270 mil)

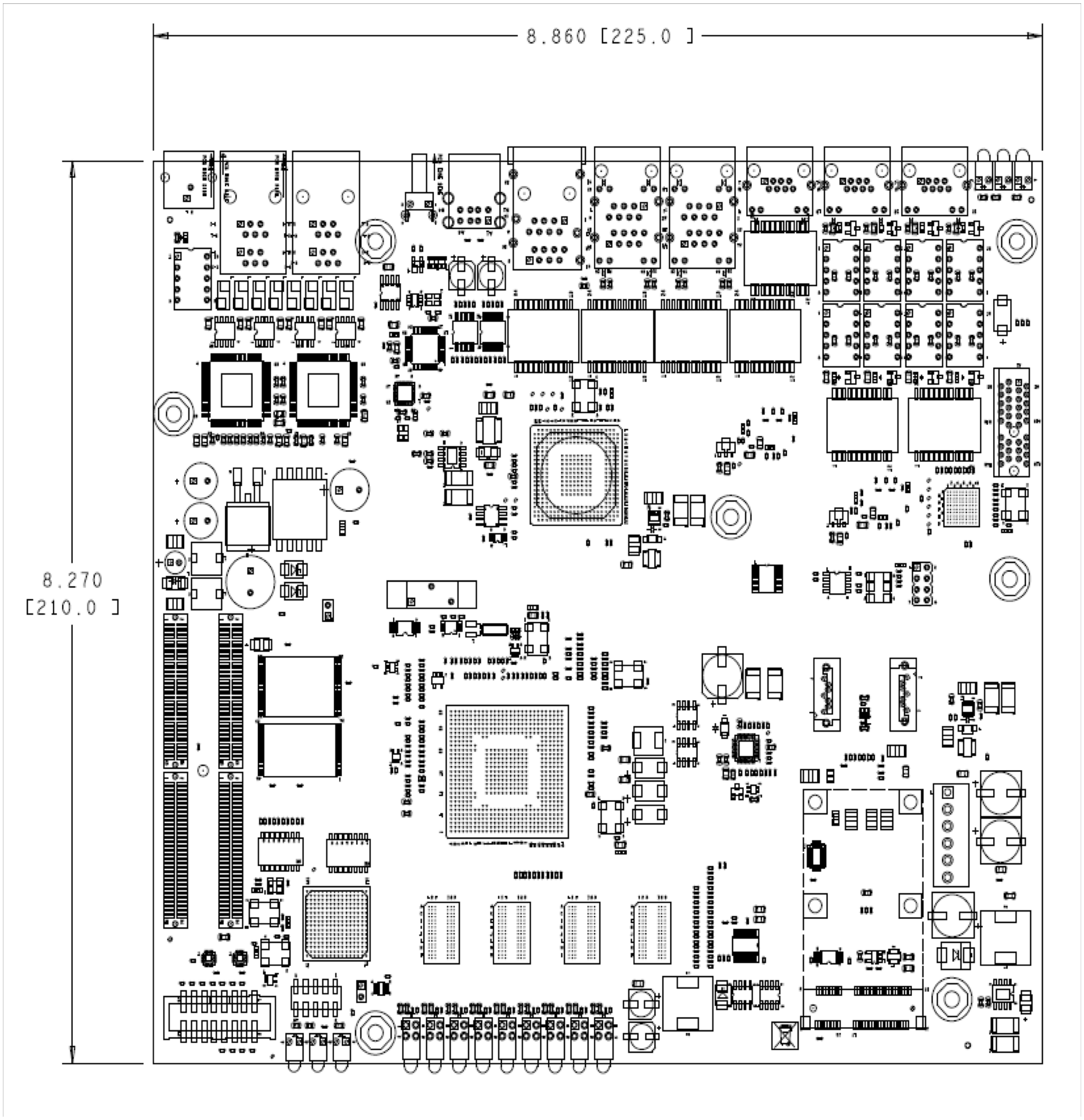

Figure 2. Dimensions of the RDB

3 Memory Interface

3.1 Description

The memory interface on the RDB is configured as DDR3 and is implemented as a single bank discrete chips(x16). ECC is not supported on the design. The memory size supported on the board is shown in Table 3 below:

Table 3. Memory Size

P2020RDB (64-bit)
1GB (4 chips * 2Gbit chips)/8bits

The PCB design is capable of running up to a clock rate of 400 MHz (800 MHz data rate). The actual and final speed of the memory design is determined by the final supported DDR3 frequency of the processor.

The DDR3 interface uses the SSTL driver/receiver and 1.5 V power. A VREF 1.5 V/2 is needed for all SSTL receivers in the DDR3 interface. For details on DDR3 timing design and termination, refer to the Freescale application note entitled “Hardware and Layout Design Considerations for DDR Memory Interfaces” (AN2582).

Signal integrity test results show this design does not require terminating resistors (series resistor (R_S) and termination resistor (R_T)) for the discrete DDR3 devices used. DDR3 supports on-die termination; the DDR3 chips and P2020E are connected directly.

The interface is 1.5 V and is provided by an on-board voltage regulator. VREF, which is half the interface voltage, or 0.75 V, is supplied by the same voltage regulator.

The DDR3 parameters are stored in I2C EEPROM (U51). An SPD binary file has been preloaded in the EEPROM.

Figure 3 shows the DDR3 SDRAM controller connection.

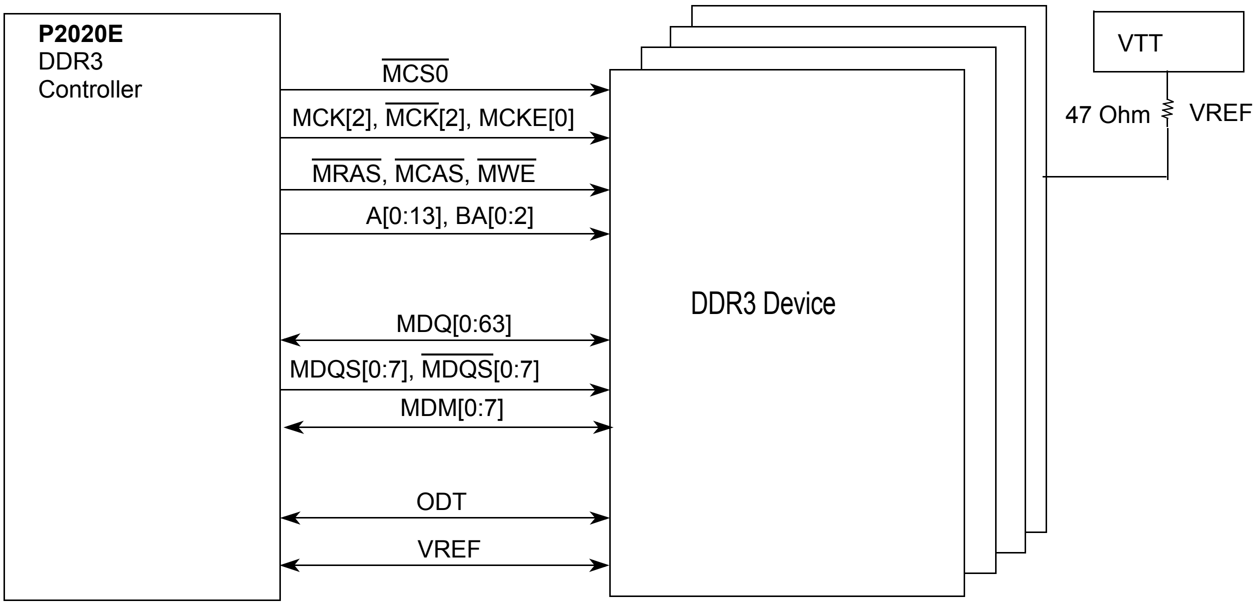

Figure 3. DDR3 SDRAM Connection

3.2 Termination

The DDR3 address, control, and command signals are terminated to the VTT rail via a 47 Ohm resistor.

4 SerDes Interfaces (PCIe/SATA/SGMII)

P2020E supports the SGMII and PCI Express high-speed I/O interface standards.

Table 4 describes the SerDes connections.

Table 4. SerDes Connectivity

SerDes Lane	Mode	Connected to	Comment
Lane 0	PCI Express 1	Mini-PCIe slot	Used for WLAN type cards
Lane 1	PCI Express 2	Standard x1 PCIe slot or PCIe to dual SATA controller	1. Select PCIe or SATA interface via SW2[7], see Section 23.2, Other configuration options 2. PCIe Slot is only intended for cards that are 10W or less
Lane 2	SGMII	Vitesse SGMII PHY	
Lane 3	not used	not used	

4.1 PCIe

On the RDB, lanes 0 and 1 are configured as two independent x1 PCI Express Interfaces. These interfaces are compliant with the PCI Express Base Specification Revision 1.0a. The physical layer of the PCI Express interface operates at a transmission rate of 2.5 Gbaud (data rate of 2.0 Gbps) per lane. The theoretical unidirectional peak bandwidth is 2 Gbps per lane. Receive and transmit ports operate independently, resulting in an aggregate theoretical bandwidth of 4 Gbps per lane.

4.2 SATA

Lane 1 is also connected to one x1 PCIe to 2x SATA controller SiI3132 via PCI Express Mux/DeMux Switch PI2PCIE212, as shown in Figure 4. SiI3132 supports 1-lane 2.5Gbit/s PCI Express and the Serial ATA Generation 2 transfer rate of 3.0Gbit/s.

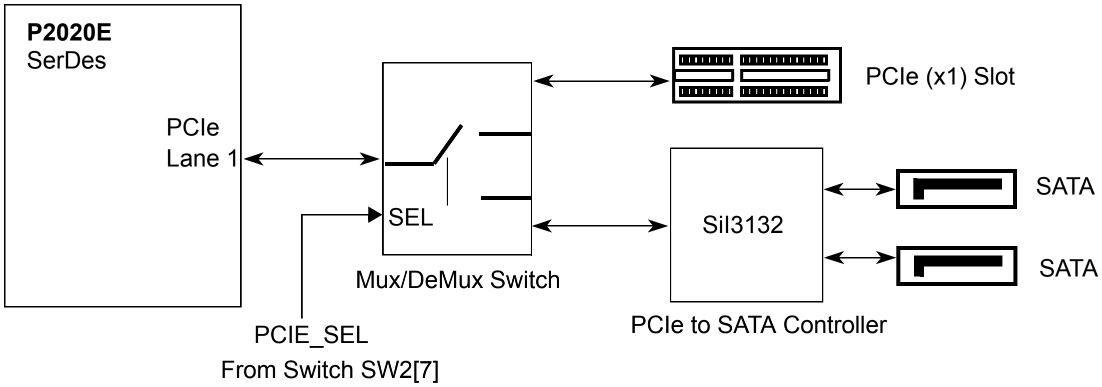

Figure 4. SATA

4.3 SGMII

Lane 2 is used in SGMII mode. The serial gigabit media independent interface (SGMII) is a high-speed interface linking the Ethernet controller with an Ethernet PHY. SGMII uses differential signalling for electrical robustness. Only four signals are required: receive data and its inverse, and send data and its inverse.

Lane 3 of the SerDes Interface is not used on the board.

4.4 SerDes Clocking

The clocking for the SerDes interface is 100MHz provided by the PI6C557-05 clock chip.

5 Enhanced Local Bus Controller (eLBC) Interface

The eLBC port connects to a wide variety of external memories, DSPs, and ASICs.

Three state machines, the GPCM, UPM, and FCM, share the same external pins and can be programmed separately to access different types of devices.

- GPCM (general-purpose chip select machine), controls access to asynchronous devices using a simple handshake protocol.
- UPM (user-programmable machine), can be programmed to interface with synchronous devices or custom ASIC interfaces.
- FCM (NAND Flash control machine), further extends interface options.

Every chip select signal can be configured so that the associated chip interface is controlled by the GPCM, UPM, or FCM state machine. All state machines can reside in the same system.

To interface with the standard memory device, an address latch is needed on the upper address bits since they are multiplexed with the data bus. The LALE is used as the latching signal. The followings modules are connected to the local bus:

- 16 Mbyte NOR flash memory
- 128 Mbyte NAND flash memory
- Vitesse Switch (processor interface)
- PLD (Lattice LCMXO1200C)

5.1 NOR Flash Memory

Through the general-purpose chip-select machine (GPCM), the P2020RDB provides 16Mbyte of flash memory. The flash memory used is configured in a 16-bit port size. Figure 5 shows the hardware connections for the flash memory.

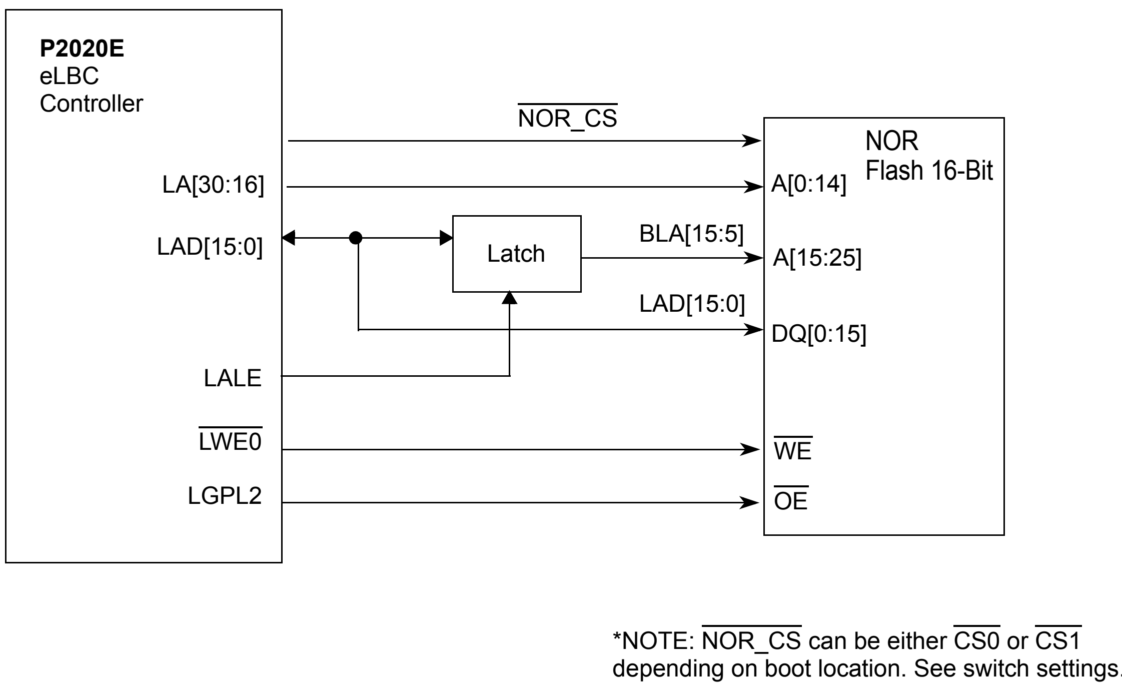

Figure 5. NOR Flash Connection

The NOR flash can be split into two logical halves by setting the FBANK_SEL signal. The FBANK_SEL signal is controlled by setting SW3[8]. Table 5 displays how the addresses are changed when using FBANK_SEL.

Table 5. Logical NOR Banks

Setting	NOR BANK used
SW3[8]=0	upper bank used for booting starting at address 0xEFF80000
SW3[8]=1	lower bank used for booting starting at address 0xEF780000

5.2 NAND Flash Memory

The P2020E has native support for NAND Flash memory through its NAND Flash control machine (FCM). The P2020RDB implements an 8-bit, 2k page-size, 128Mbyte NAND Flash from revD2 schematic. Figure 6 shows the NAND Flash connection.

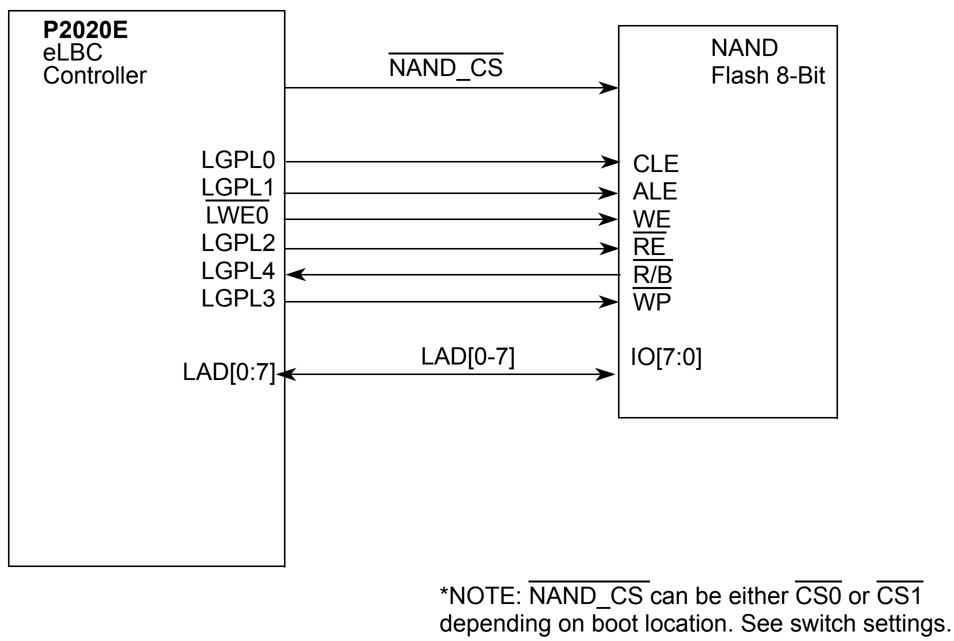

Figure 6. NAND Flash Connection

5.3 GBE L2 Switch (VSC7385) Parallel Interface

The Gigabit Ethernet L2 switch (VSC7385) parallel interface is connected to the local bus of the processor. This gives the processor the ability to load program into the internal instruction memory of the switch at boot up, and also allows access to the internal registers of the L2 switch. The general-purpose chip-select machine (GPCM) generates the timing of read/write accesses. Read/write accesses to the VSC7385 are terminated by the DONE signal, which is connected to the LGTA of the GPCM and generates the internal TA for the PowerPC™ core. Figure 7 shows the connection between the VSC7385 and the P2020E.

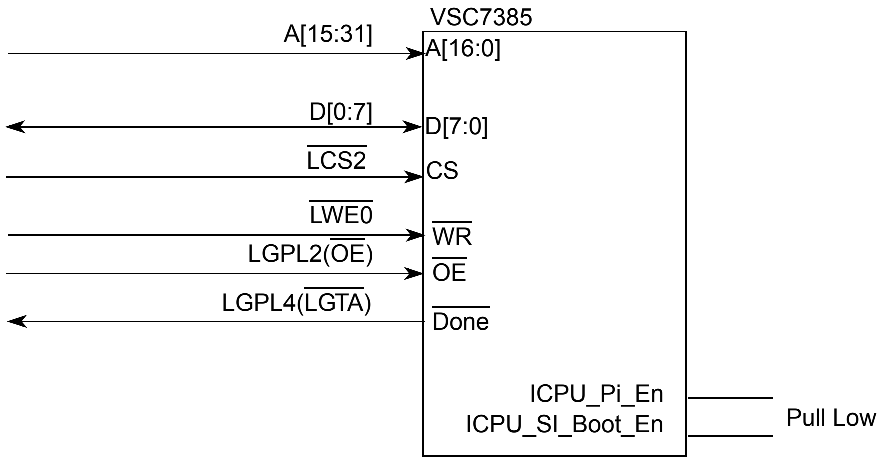

Figure 7. Parallel Interface of VSC7385

5.4 Lattice PLD

Lattice PLD LCMXO1200C is connected to the local bus of the processor. This gives the processor the ability to access the 8-bit registers in the PLD. Refer P1021RDB Combo Board CPLD Specification-V4.2 for more details. Figure 8 shows the connection between PLD and the P2020E.

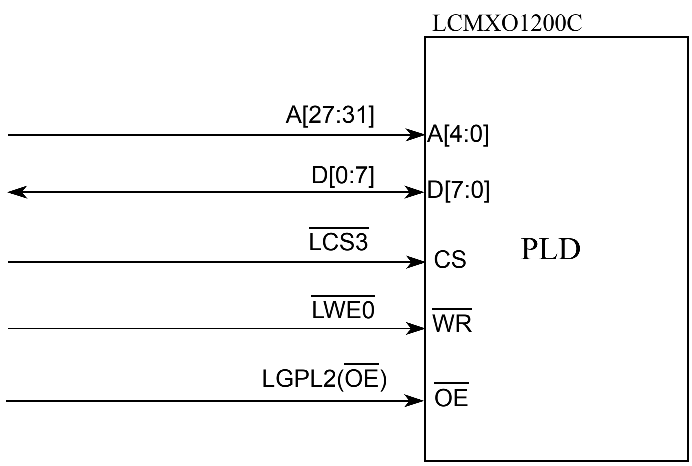

Figure 8. Local Bus Connection of PLD

Table 6 summarizes the eLBC connectivity.

Table 6. eLBC Connectivity

eLBC chip select	Manufacturer	Device	Comment
LCS0 or LCS1 Assignment dependent on which device is used for booting. Handled automatically by the POR PLD based on the switch setting.	Spansion	S29GL128S	NOR FLASH memory 16 Mbyte (16bit)
LCS0 or LCS1 Assignment dependent on which device is used for booting. Handled automatically by the POR PLD based on the switch setting.	Micron	MT29F1G08ABAEAWP:E	NAND Flash 128 Mbytes (8bit)
LCS2	Vitesse	VSC7385	Ethernet Switch
LCS3	Lattice	LCMXO1200C	PLD
LCS4-LCS7	not used	not used	

6 Ethernet

The RDB supports a total of six ethernet ports.

6.1 eTSEC1 10/100/1000 BaseT Interface

eTESC1 is set to operate in RGMII mode. It connects to a VSC7385 5-port L2 switch, as shown in Figure 9. The switch in turn provides four external ethernet ports at the rear of the RDB chassis. Since these ports are connected to the Vitesse switch, these switched ethernet ports are intended for LAN connectivity. The firmware for the switch is downloaded over the local bus.

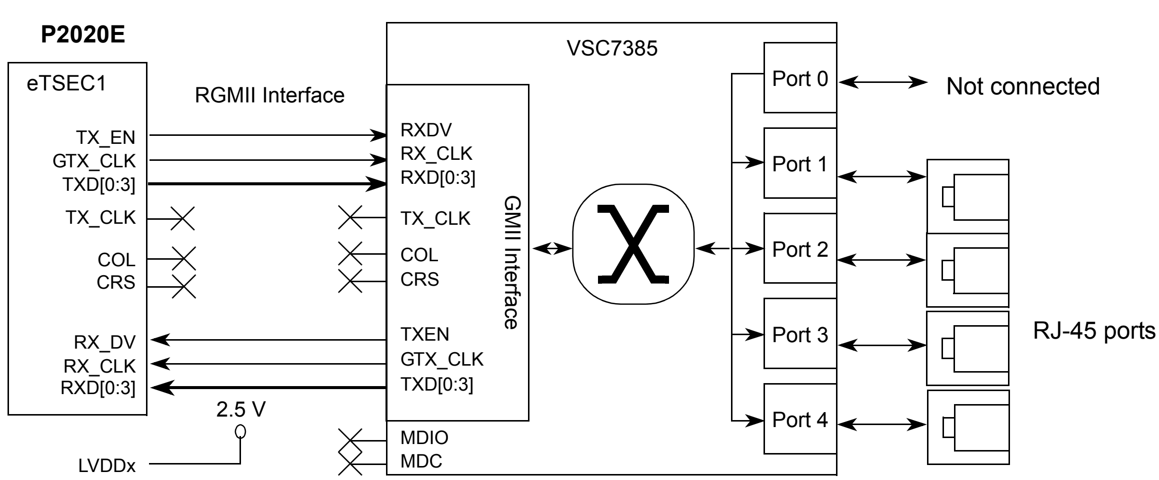

Figure 9. RGMII Interface Connection for L2 Switch

6.2 eTSEC2 10/100/1000 BaseT Interface

eTSEC2 is set to operate in SGMII and is directly connected to the Vitesse SGMII PHY (VSC8221), as shown in Figure 10. This port can be used for WAN connectivity.

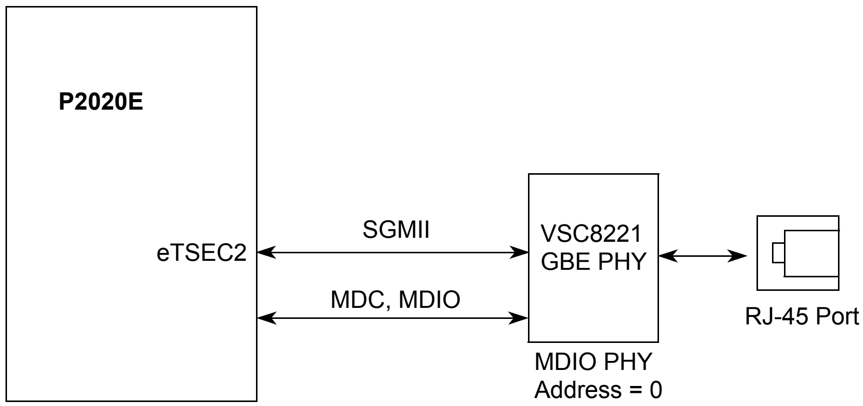

Figure 10. eTSEC2 Connection

6.3 eTSEC3 10/100/1000 BaseT Interface

eTSEC3 is set to operate in RGMII and is directly connected to the Atheros RGMII PHY (AR8021), as shown in Figure 11. This port can be used for WAN connectivity.

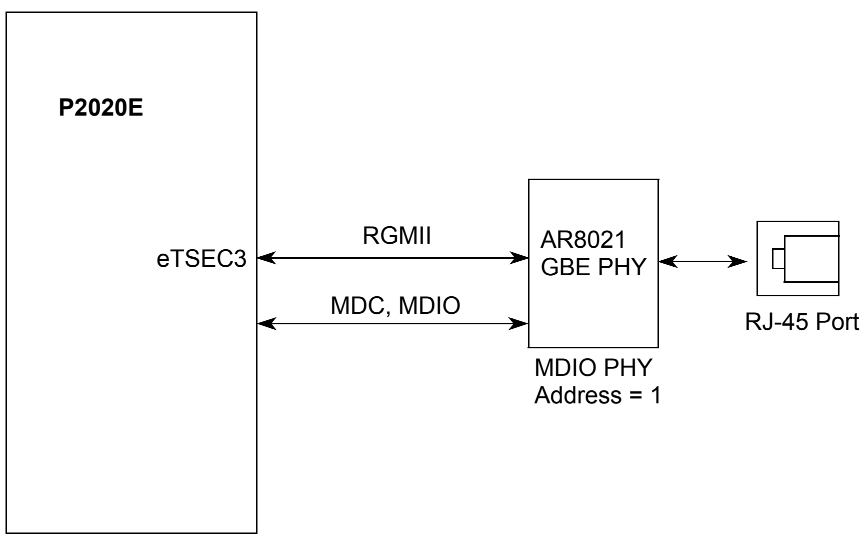

Figure 11. eTSEC3 Connection

6.4 Ethernet Management

Table 7 displays how the MDC and MDIO connections are made on the RDB.

Table 7. MDC/MDIO Connectivity

Device	PHY Address	Comment
VSC7385	------	Not used. Local bus used for configuration and management of the switch.
VSC8221	00000	
AR8021	00001	

6.5 Ethernet Ports

Figure 12 shows how the ethernet ports are connected on the backside of the RDB chassis.

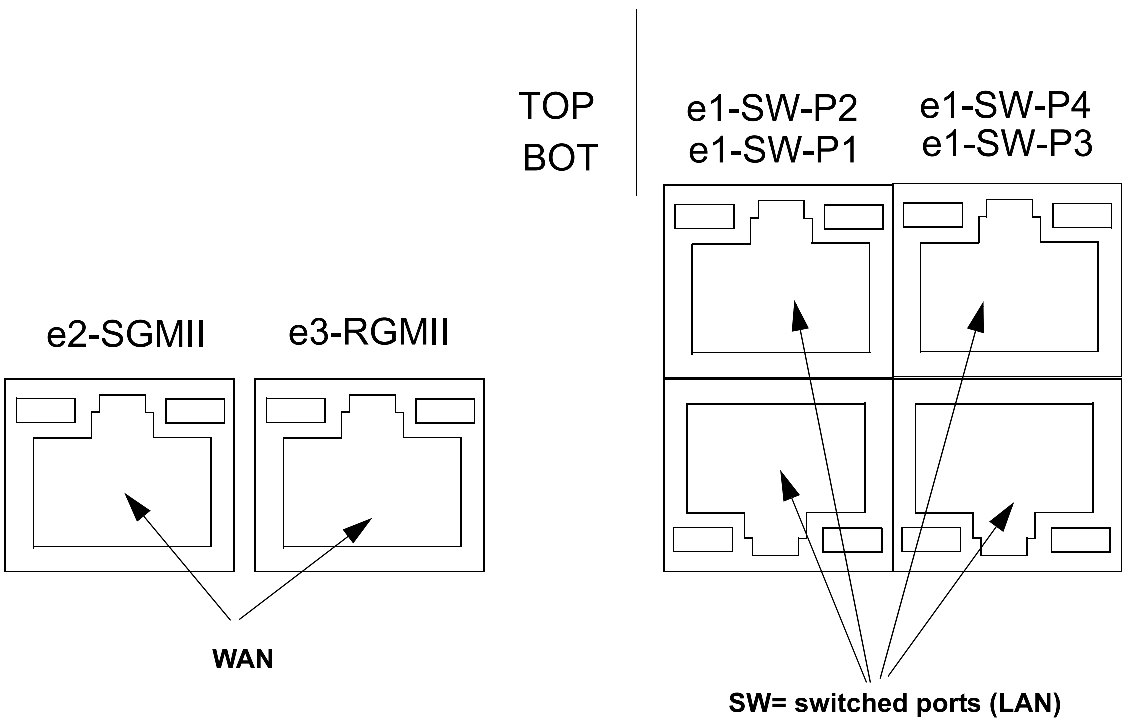

Figure 12. Ethernet Port Connectivity

7 eSPI

The eSPI is a full-duplex, synchronous, character-oriented channel that supports a four-wire interface (receive, transmit, clock, and slave select). The P2020E has the ability to boot from an SPI serial flash device in addition to supporting other peripheral devices conforming to the SPI standard.

On the RDB, a Spansion SPI flash memory is supported. Additionly, the SPI interface is also connected to 1588 test circuitry. Table 8 displays the eSPI connections.

Table 8. eSPI Connectivity

eSPI Chip Select	Manufacturer	Part #	Comment
SPI_CS0_N	Spansion	S25FL128SAGNFI001	16MB Spansion SPI Flash
SPI_CS3_N	Microchip	MCP4921	12-bit DAC

8 eSDHC Interface

The enhanced SD host controller (eSDHC) provides an interface between host system and SD/MMC cards. The secure digital (SD) card is specifically designed to meet the security, capacity, performance, and environmental requirements inherent in emerging audio and video consumer electronic devices. Booting from eSDHC interface is supported via the processor's on-chip ROM.

On the RDB, a single connector is used for both SD and MMC memory cards as shown in Figure 13.

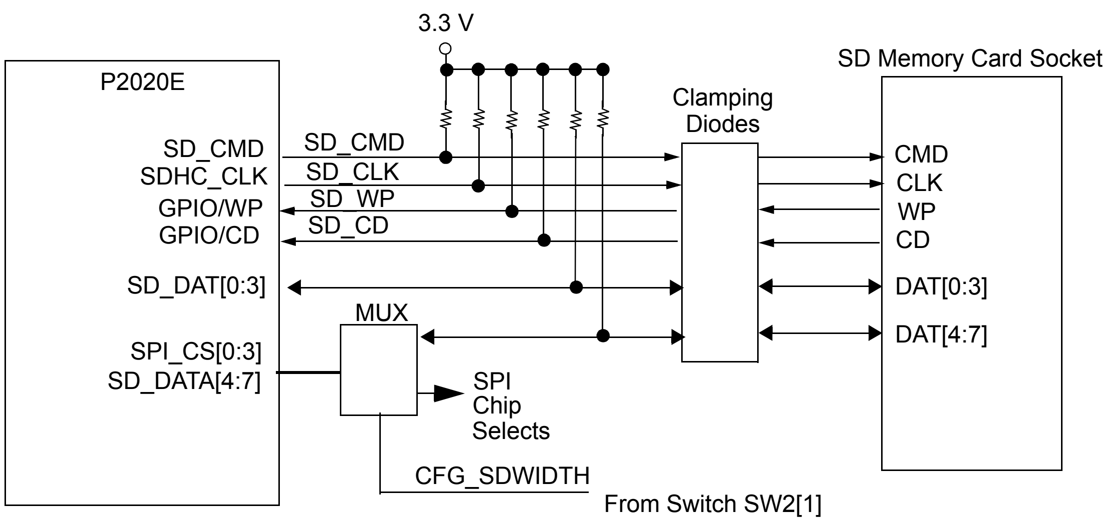

Figure 13. SD Memory Card Connection

The SPI chip selects are multiplexed with the higher data nibble of SDHC interface signals. The selection between the two is controlled by the cfg_sdwidth signal (switch2[1]). By default, CFG_SDWIDTH = 0, thereby allowing SPI and a 4-bit SD/MMC interface to co-exist on the board.

When CFG_SDWIDTH = 1, the on-board mux connects the upper data nibble to the SD/MMC connector. When doing this, the user must still configure the processor in order to realize the increased bus width. Secondly, when used in this mode, SPI connectivity is not available.

Table 9 lists the multiplexed signals.

Table 9. Multiplexed Signals

SPI Signal	Alternative Signal
SPI_CS0_B (IO)	SDHC_DAT4
SPI_CS1_B (IO)	SDHC_DAT5
SPI_CS2_B (IO)	SDHC_DAT6
SPI_CS3_B (IO)	SDHC_DAT7

9 GPIO

Table 10 lists the GPIO pin usage on the RDB platform.

Table 10. GPIO Pin Usage

GPIO	Input / Output	Signal Name	Comment
GPIO07	input	LOAD_DEFAULT_N	Default configuration load request via pushing down Reset Switch SW1 for more than 6 seconds
GPIO11	output	WDI	Periodic signal for Watchdog MAX6370 (U55) input

10 I^2C

The P2020E device has two I^2C controllers. On the RDB, the I2C buses are connected as shown in Figure 14. The M24256 serial EEPROM can be used to store configuration registers' values and/or user program if the P2020E boot sequencer is enabled. For details about the boot sequencer mode, refer to the P2020E reference manual. By default, the boot sequencer is not used and the boot code and initialization for the board is loaded from the local bus flash memory.

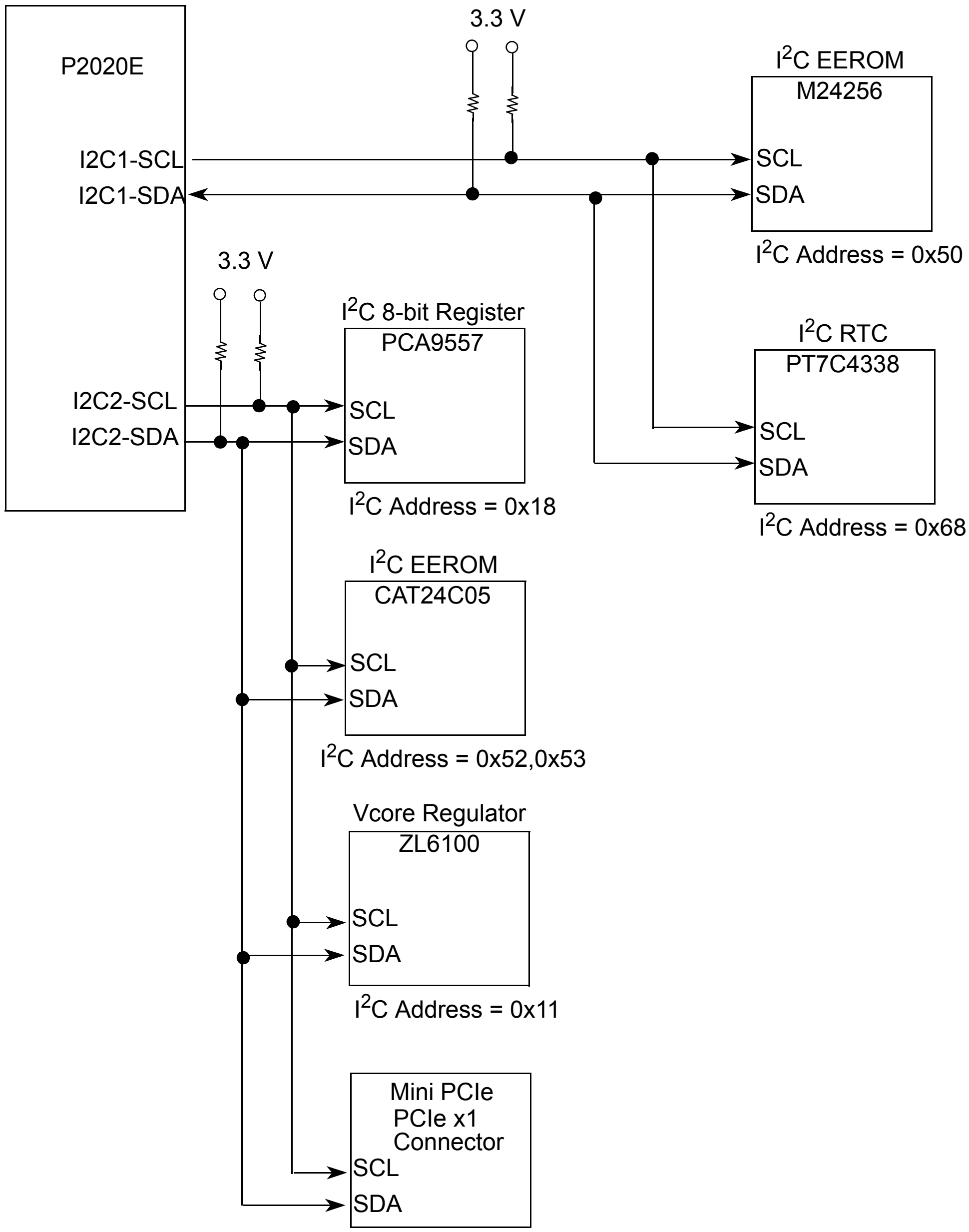

Figure 14. I²C Connection

Table 11. I2C Bus Connections

I2C Bus	I2C Address	Manufacturer	Device	Comment
I2C1	50H	ST Microelectronics	M24256	Boot sequencer eeprom 256Kbits
I2C1	68H	Pericom	PT7C4338	Real time clock

Table 11. I2C Bus Connections

I2C Bus	I2C Address	Manufacturer	Device	Comment
I2C2	11H	Zilker	ZL6100	Vcore Regulator
I2C2	18H	NXP	PCA9557	8-bit I2C register
I2C2	52H,53H	ON Semiconductor	CAT24C05	SPD EEPROM 4Kbits
I2C2			Mini PCIe PCIe x1 Connector	

11 USB Interface

The USB interface is configured to operate as a standalone host. To complete the USB interface, an external PHY is employed and connected to the processor's ULPI signals. The SMSC USB3300 PHY is used on the RDB. A 4 downstream ports, 1 upstream port USB Hub Genesys Logic GL850A is connected to the USB PHY to expand the USB ports.

The board features:

- High-speed (480 Mbps), full-speed (12 Mbps) and low-speed (1.5 Mbps) operation
- Host mode
- Dual stacked Type A connection
- One port connected to Mini PCIe connector

Figure 15 shows how the USB connectivity is implemented on the RDB.

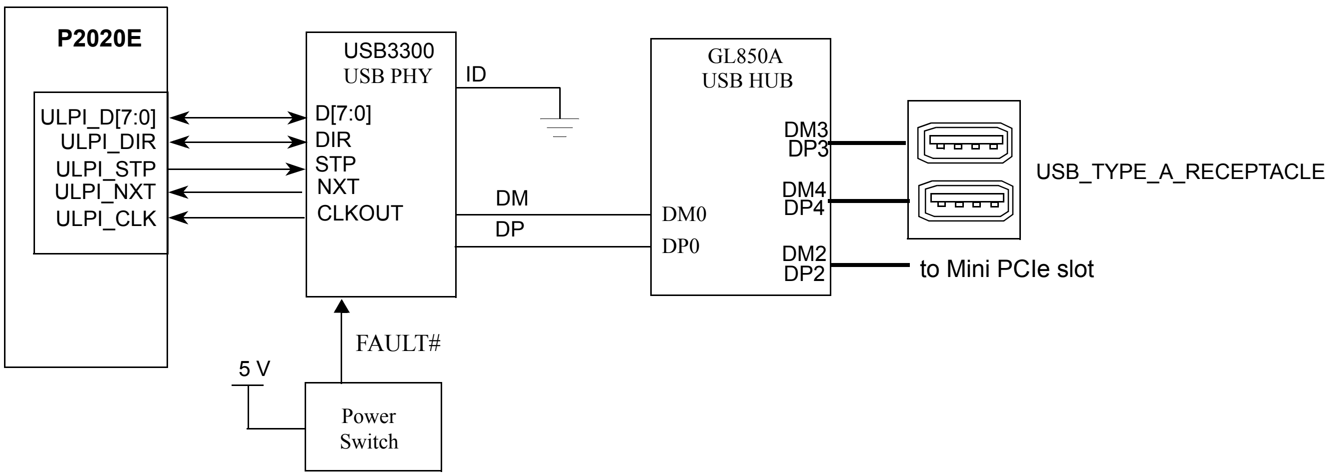

Figure 15. USB Interface

12 Dual RS-232 Ports

The P2020E device has two UART controllers. The RS-232 interface provides an RS-232 standard interconnection between the board and an external host. The serial connection is typically configured to run at 115.2 Kbps.

Each UART supports:

- Full-duplex operation.
- Software-programmable baud generators:
  - Divide the input clock by 1 to (216 – 1)
  - Generate a 16x clock for the transmitter and receiver engines
- Clear-to-send (CTS) and ready-to-send (RTS) modem control functions.
- Software-selectable serial interface data format that includes:
  - Data length
  - Parity
  - 1/1.5/2 STOP bit
  - Baud rate
- Overrun, parity, and framing error detection.

The UART ports are routed to dual stacked RJ45 connectors J5 as shown in Figure 16. UART0 is uesd as default port.

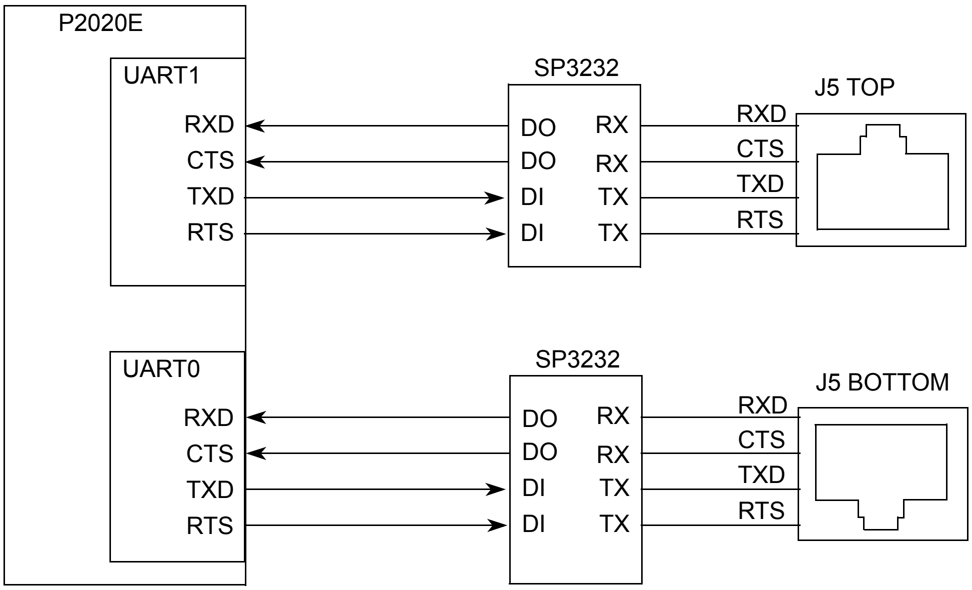

Figure 16. RS-232 Debug Ports Connection

Table 12 lists the connectivity for the UART RJ45 to DB9 female cable connections.

Table 12. UART Connections

RJ45 Pin#	RS-232 Signal	DB9 Female Pin#
1	RTS	8
2	NC	
3	TXD	2
4	GND	
5	GND	5
6	RXD	3
7	NC	
8	CTS	7

13 Lattice PLD

The Lattice PLD (U44) is used for power up sequence control, system reset, POR configuration, multiplexed function select and LEDs control. Refer P1021RDB Combo Board CPLD Specification-V4.2 for more details.

14 POR Configuration

14.1 POR Configuration PLD

The POR configuration PLD drives the appropriate configuration signals to the processor based on the selected configuration switch setting. When hard reset (HRESET) is asserted, the POR config PLD begins to drive the POR config signals to the processor. The config signals remain asserted until the POR config signals have been properly latched by the processor. The POR configuration PLD does not drive all POR configuration pins, just those needed for frequency selection and boot location.

14.2 POR Configuration Resistors

The POR settings that are not set by the POR configuration PLD are controlled via on-board resistors. For a list of POR configuration resistors, see page 16 of the schematic.

15 JTAG/COP

The JTAG connection is provided by a direct connection to the appropriate header connector.

15.1 COP/JTAG Port

The common on-chip processor (COP) is part of the P2020E's JTAG module and is implemented as a set of additional instructions and logic. This port can connect to a dedicated emulator for extensive system debugging. Several third-party emulators in the market can connect to the host computer through the Ethernet port, USB port, parallel port, RS-232, and so on. A typical setup using a USB port emulator is shown in Figure 17.

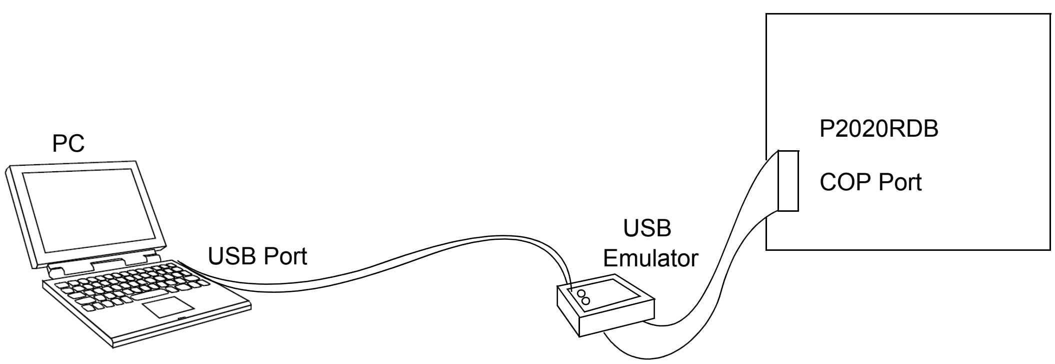

Figure 17. Connecting P2020RDB to a USB Emulator

The 16-pin generic header connector carries the COP/JTAG signals and the additional signals for system debugging. The pinout of this connector is shown in Figure 18.

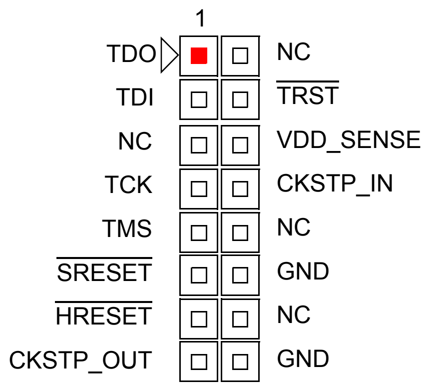

Figure 18. RDB COP Connector

Table 13 describes the connections made from the RDB COP Connector

Table 13. Connectivity from the COP Connector

Pin Number		
Pin #	**Signal Name**	**Connection**
1	TDO	Connected directly between the processor and JTAG/COP connector.
2	NC	Not connected
3	TDI	Connected directly between the processor and JTAG/COP connector.
4	TRST	Routed to the RESET PLD. TRST to the processor is generated from the PLD.
5	NC	Not connected
6	VDD_SENSE	Pulled to 3.3V via a 10 Ohm resistor
7	TCK	Connected directly between the processor and JTAG/COP connector.
8	CKSTP_IN	Connected directly between the processor and JTAG/COP connector.
9	TMS	Connected directly between the processor and JTAG/COP connector.
10	NC	Not connected
11	SRESET	Routed to the RESET PLD. SRESET to the processor is generated from the PLD.
12	GND	Connected to ground
13	HRESET	Routed to the RESET PLD. HRESET to the processor is generated from the PLD.

Table 13. Connectivity from the COP Connector

Pin Number		
14	KEY	Not connected
15	CKSTP_OUT	Connected directly between the processor and JTAG/COP connector.
16	GND	Connected to ground

16 Interrupts

Figure 19 shows the external interrupts to the P2020E.

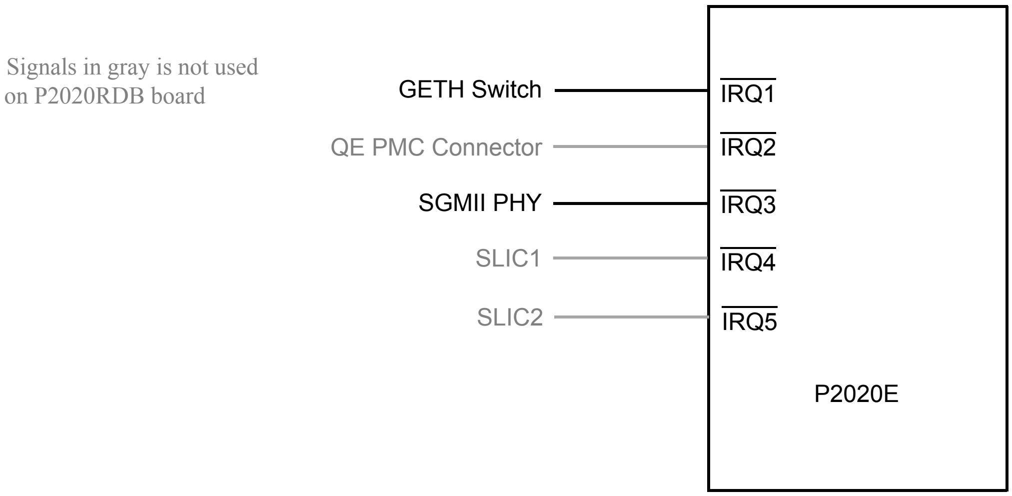

Figure 19. P2020E Interrupts

Table 14 displays how the interrupts are connected on the RDB platform.

Table 14. Interrupts

Name	Connection	Note
IRQ0	not used	On-board Pull-up
IRQ1	Gigabit Ethernet Switch VSC7385	On-board Pull-up
IRQ2	not used	On-board Pull-up
IRQ3	SGMII PHY VSC8221	On-board Pull-up
IRQ4	not used	On-board Pull-up

Table 14. Interrupts (continued)

Name	Connection	Note
IRQ5	not used	On-board Pull-up
IRQ6	not used	On-board Pull-up
IRQ_OUT	not used	On-board Pull-up

17 DMA

The DMA function itself is not utilized on the RDB platform. Unused input pins are pulled high. Since certain DMA pins have POR functionality, these pins are connected on the platform.

18 Connectors, Headers, Push Buttons and LEDs

18.1 Headers

Table 15 lists the various headers on the RDB platform.

Table 15. Headers

Reference Designators	Used for	Note
J16	Lattice Header	Used for programming the Lattice PLD devices.
J6	1588	
J17	COP/JTAG	
J19	Reset	Default Open

18.2 Connectors

Table 16 lists all the connectors on the RDB platform.

Table 16. Connectors

Reference Designators	Used for	Note
J12	Open Frame Power	
J18	SD/MMC Card	
U21	PCIe x1 cards	Intended use is for PCIe cards that are 10W are less.

Table 16. Connectors

Reference Designators	Used for	Note
P6	Mini-PCIe cards	
P3	Ethernet Port	eTSEC2 (SGMII); VSC8221
P2	Ethernet Port	eTSEC3 (RGMII); AR8021
J4	Ethernet Ports	Top Port - eTSEC1-> VSC7385 Port 2 Bot Port - eTSEC1-> VSC7385 Port 1
J3	Ethernet Ports	Top Port - eTSEC1-> VSC7385 Port 4 Bot Port - eTSEC1-> VSC7385 Port 3
J2	Dual Type A USB	
J10	SATA HD	
J11	SATA HD	
J5	UART	TOP: UART1 BOT: UART0
BT1	Battery Holder	CR-2032

18.2.1 Battery Holder

The board contains an RTC that requires a battery in order to maintain the data inside the RTC. The battery holder (BT1) accommodates a CR-2032. Figure 20 shows how to insert a battery.

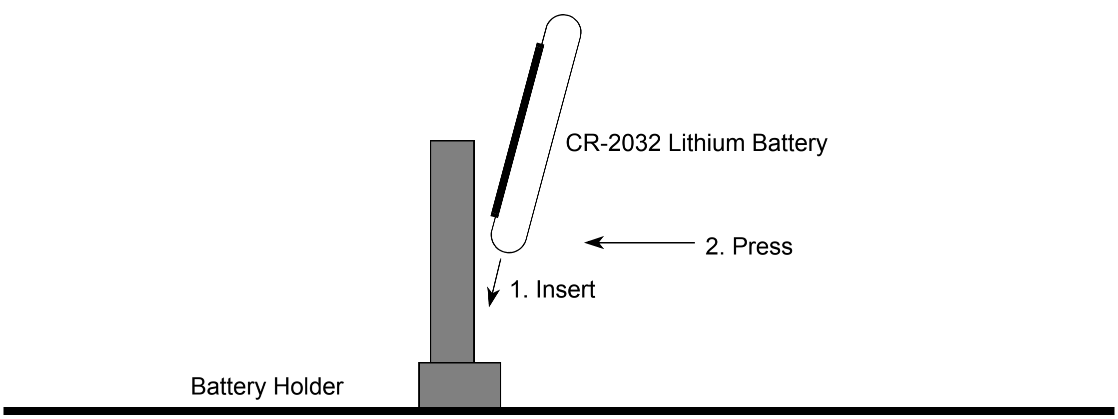

Figure 20. Installation of Battery

18.3 Push Buttons

Table 17 displays how the push button is used on the RDB platform.

Table 17. Push Buttons

Reference Designators	Used for
SW1	Reset

18.4 LEDs

Table 18 lists all the LEDs on the RDB chassis.

Table 18. LEDs

LEDs	Used for	Controlled by
D34	Power on	+3.3V rail
D35	Status	Lattice PLD (U44)
D27	TOP: Link BOT: Activity	VSC7385 Ethernet Switch eTSEC1 Port 4
D28	TOP: Link BOT: Activity	VSC7385 Ethernet Switch eTSEC1 Port 3
D29	TOP: Link BOT: Activity	VSC7385 Ethernet Switch eTSEC1 Port 2
D30	TOP: Link BOT: Activity	VSC7385 Ethernet Switch eTSEC1 Port 1
D32	TOP: Link BOT: Activity	eTSEC3 RGMII PHY AR8021
D33	TOP: Link BOT: Activity	eTSEC2 SGMII PHY VSC8221

Refer P1021RDB Combo Board CPLD Specification-V4.2 for details about how to control the LEDs by Lattice PLD.

Figure 21 shows LEDs on the front side of P2020RDB chassis.

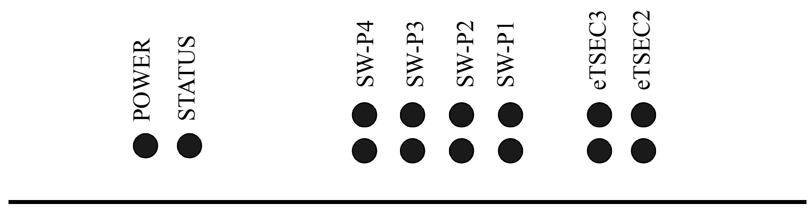

Figure 21. LEDs on Chassis

19 Power Related

19.1 Open Frame Power Supply

Open Frame power supply PD45 supplys +12V and +5V for the RDB board. The rated power is 40W.

19.2 CPU_VDD

The CPU core voltage CPU_VDD rail is sourced from an Intersil switching regulator. The device used on the RDB is the ZL6100. CPU_VDD=1.05V

19.3 AVDD Signals

All AVDD pins are sourced by the CPU_VDD rail through the recommended filter circuit.

19.4 DDR

The memory interface power rails (VTT, GVDD, and VREF) are sourced by a TI switching regulator. The part used is the TPS51116 device. For DDR3, VTT=0.75V, GVDD=1.5V, and VREF = 0.75V.

19.5 SerDes

The SerDes rails (SVDD, XVDD) are sourced from the on-board CPU_VDD core voltage rail.

19.6 USB, SPI, eSDHC (CVDD)

Each of these rails are sourced from 3.3V rail, which is a dedicated power plane on the board. The 3.3V rail is from an MPS switching regulator MP2380.

19.7 Local Bus (BVDD)

This rail is sourced from 3.3V, which is a dedicated power plane on the board.

19.8 DUARTs, System Control, I2C, JTAG (OVDD)

This rail is sourced from 3.3V, which is a dedicated power plane on the board.

19.9 eTSECs (LVDD)

The LVDD rail is used for the TSEC I/Os and is configured for 2.5V operation. The rail is sourced from MPS switching regulator, part number MP2119DQ.

19.10 Mini-PCIe (+1.5V)

The +1.5V rail is used by the mini-PCIe slot and is sourced by an MPS switching regulator. The part used is the MP2105DJ device.

19.11 PCIe x1 slot (+3.3V and +12V)

The PCIe x1 slot +12V rail is driectly derived from power supply. The 3.3V is soured from MPS switching regulator MP2380.

19.12 Vitesse Devices (+1.2V)

The +1.2V rail used by the Vitesse devices is sourced by an MPS switching regulator. The part used is the MP2365 device.

19.13 PCIe to SATA Controller (+1.8V)

The 1.8V rail used by the PCIe to SATA Controller Silicon Image SiI3132 is sourced from an MPS switching regulator. The part used is the MP2119DQ device.

19.14 Voltage Selection

The P2020E device supports multiple supply voltages on its I/O supplies. Table 19 shows how the voltage selection pins are configured on the RDB platform.

Table 19. I/O Supply Voltage Selection

Signal Name	Connection	Comment
LVDD_SEL	Pulled high. LVDD = 2.5V	eTSEC1, 2, 3, Ethernet management, 1588
BVDD_VSEL[0:1]	Pulled high. BVDD = 3.3V	Local Bus, GPIO[8:15]
CVDD_VSEL[0:1]	Pulled high. CVDD = 3.3V	USB, SD/MMC, SPI

20 1588

The 1588 signals are routed to a 1588 header on the board (J6). The 1588 clock input into the processor can be controlled over the SPI interface through a 12-bit digital-to-analog converter (U29). The output of the DAC feeds directly into a precision VCXO which in turn is used to drive the 1588 clock into the processor. The DAC and VCXO combination allows the 1588 clock to be varied as needed for testing.

21 Clocking

The input system clock for the processor is a 100 MHz clock source. The DDR clock input is driven by a 66.66 MHz clock source. All PCIe ports receive a dedicated 100 MHz clock. All Gigabit PHYs receive a dedicated 25 MHz oscillator clock.

22 Reset

All resets for the board are handled by the PLD (U44). Power-on reset is initiated by depressing the power switch if the board is in a chassis. Warm reset is initiated by pressing SW1 on the board. Software is also capable of initiating a warm reset by asserting the HRESET_REQ line from the processor.

23 Switch Settings

The RDB has user selectable switches for evaluating different frequency and boot options for the P2020E device. The table that follow describes the available options.

23.1 P2020RDB Configuration (Switch Method)

NOTE

All frequencies below assume that the input SYSCLK is set to 100 MHz for P2020RDB.

Table 20. P2020E Config Options

Switch Settings SW3[1:6]	Core1 Freq (MHz)	Core2 Freq (MHz)	Platform (MHz)	DDR Freq (MHz)	Boot Location	Boot Hold-off
01 1110	800	800	400	667	NOR	Core0 boot; Core1 hold-off
10 1110	800	800	400	800	NOR	Core0 boot; Core1 hold-off
00 1110	1000	1000	500	667	NOR	Core0 boot; Core1 hold-off
11 0110	1000	1000	500	800	NOR	Core0 boot; Core1 hold-off
10 0110	1200	1200	600	667	NOR	Core0 boot; Core1 hold-off
00 0110	1200	1200	600	667	SD/MMC	Core0 boot; Core1 hold-off
11 1010	1200	1200	600	800	NAND	Core0 boot; Core1 hold-off
01 1010	1200	1200	600	800	SD/MMC	Core0 boot; Core1 hold-off
10 1010	1200	1200	600	800	PCIe2	Core0 boot; Core1 hold-off

Switch Settings SW3[1:6]	Core1 Freq (MHz)	Core2 Freq (MHz)	Platform (MHz)	DDR Freq (MHz)	Boot Location	Boot Hold-off
00 1010	1200	1200	600	800	SPI	Core0 boot; Core1 hold-off
11 0010	1200	1200	600	800	NOR	Core0 boot; Core1 hold-off

23.2 Other configuration options

Table 21 elaborates on the other configuration options that are available on the board.

Table 21. Other Config Options

Switch	Signal Name	Signal Meaning	Setting
SW3[7]	LGPL5 (cfg_boot_seq[1])	Selects whether the boot sequencer is enabled during boot-up.	OFF: boot sequencer enabled and configuration information loaded from I2C ROM. A valid ROM must be present. If not the board will hang. ON: boot sequencer disabled
SW3[8]	FBANK_SELECT	Selects which NOR flash bank is selected.	OFF: upper 4 sectors used for booting ON: middle 4 sectors used for booting
SW2[1]	CFG_SDWIDTH	Configs the width of the SD/MMC bus, 4-bit or 8-bit	OFF: then width = 4bits, SPI interface actived ON: then width = 8bits Software can read the status of this bit by reading the I2C 8-bit register.
SW2[2]	LA18 (cfg_host_agt[1])	Controls the setting of the cfg_host_agt[1] pin	ON: cfg_host_agt[0] = 1 OFF: cfg_host_agt[0] = 0 See Section 23.4, Configuring Host/Agent Mode
SW2[3]	DMA1_DACK_N	Freescale use only	Must be set to ON for P2020E
SW2[4]	LA19 (cfg_host_agt[2])	Controls the setting of the cfg_host_agt[2] pin	ON: cfg_host_agt[2] = 1 OFF: cfg_host_agt[2] = 0 See Section 23.4, Configuring Host/Agent Mode
SW2[5]	USB1_STP	Freescale use only	Must be set to ON for P2020E
SW2[6]	TEST_SEL	Dual core or single core selection	ON: dual core OFF: single core
SW2[7]	PCIE_SEL	Selects	ON: selects PCIe x1 slot OFF: selects SATA
SW2[8]	LWE1_N (cfg_host_agt[0])	Controls the setting of the cfg_host_agt[0] pin	ON: cfg_host_agt[0] = 1 OFF: cfg_host_agt[0] = 0 See Section 23.4, Configuring Host/Agent Mode

23.3 Factory Settings of board switches

Table 22 shows default settings of all the switches on SW2 and SW3.

Switch	1	2	3	4	5	6	7	8
SW3	ON	ON	OFF	OFF	ON	OFF	ON	OFF
SW2	OFF	ON	ON	ON	ON	ON	OFF	ON

Table 22. Default Settings of Board Switches

23.4 Configuring Host/Agent Mode

Table 23 shows how the PCIe ports can be configured in either Host or Agent mode.

Table 23. Host/Agent Selection

Device	Configuration	cfg_host_agt[0] controlled SW2[8]	cfg_host_agt[1] controlled by SW2[2]	cfg_host_agt[2] controlled by SW2[4]
P2020E	PCIe1 in Host Mode PCIe2 in Host Mode	SW2[8] =ON cfg_host_agt[0] = 1	SW2[2] =ON cfg_host_agt[1] = 1	SW2[4] =ON cfg_host_agt[2] = 1
P2020E	PCIe1 in Host Mode PCIe2 in Agent Mode	SW2[8] =OFF cfg_host_agt[0] = 0	SW2[2] =ON cfg_host_agt[1] = 1	SW2[4] =OFF cfg_host_agt[2] = 0
P2020E	PCIe1 in Agent Mode PCIe2 in Host Mode	SW2[8] =OFF cfg_host_agt[0] = 0	SW2[2] =OFF cfg_host_agt[1] = 0	SW2[4] =ON cfg_host_agt[2] = 1
P2020E	PCIe1 in Agent Mode PCIe2 in Agent Mode	SW2[8] =OFF cfg_host_agt[0] = 0	SW2[2] =OFF cfg_host_agt[1] = 0	SW2[4] =OFF cfg_host_agt[2] = 0

23.5 Read and Writing of certain board switches

An 8-bit I2C register allows software to override certain switches remotely without having to change the physical switch. In addition, the CFG_SDWIDTH status can also be read via the I2C register. The I2C register is implemented by Philips PCA9557 device. The register definition is shown in Table 24. The mapping between the I2C register bits and the switches are shown in Table 25. The I2C switch is located on I2C2 and is accessible at address 18H.

After being set, software must issue a reset command (asserting HRESET_REQ_B) in order for the new switch settings to take effect. Once the I2C registers are written and enabled, they override the board switches until either the I2C bits are disabled or until a power cycle occurs.

Table 24. PCA9557 Register Definition

Name	Type	Function
Register 0	Read	Input port register
Register1	Read/Write	Output port register

Name	Type	Function
Register 2	Read/Write	Input pins polarity inversion register =1, the corresponding port pin's polarity is inverted =0, the corresponding port pin's original polarity is retained Note that default value of this register is: Bit [7:4] = 1, polarity inverted Bit [3:0] = 0, polarity not inverted
Register 3	Read/Write	Configuration register =1, the corresponding port pin is enabled as an input =0, the corresponding port pin is enabled as an output Note that default value of this register is FF

Table 25. Mapping between I2C register and POR switches

I2C Register Bit	Comment
IO7	overrides SW3[1], and thereby controls Switch1
IO6	overrides SW3[2], and thereby controls Switch2
IO5	overrides SW3[3], and thereby controls Switch3
IO4	overrides SW3[4], and thereby controls Switch4
IO3	overrides SW3[5], and thereby controls Switch5
IO2	overrides SW3[6], and thereby controls Switch6
IO1	overrides SW3[8]; and thereby controls FBANK_SELECT
IO0	"read-only" of CFG_SDWIDTH switch SW2[1]

23.5.1 Uboot steps for overriding on-board switches to change frequency

1. First change to the correct I2C bus
   - => i2c dev 1
   - Setting bus to 1
2. A read of the input register will return the current state of the on-board switches
   - => i2c md 18 0
   - 0000: 38 38 38 38 38 38 38 38 38 38 38 38 38 38 38 38
3. Set you desired values for switches.
   - => i2c mw 18 1 38
4. Next, set the appropriate pins as outputs.
   - => i2c mw 18 3 01
5. A read will return the current over-written value that will be used for all subsequent resets.
   - => i2c md 18 0
   - 0000: c8 c8 c8 c8 c8 c8 c8 c8 c8 c8 c8 c8 c8 c8 c8 c8

NOTE

This value will be used until either the power is turned off, or until the pins from the I2C device are tri-stated (....register 3 written as follows=> i2c mw 18 3 FF)

23.5.2 Example log file showing change of frequencies via software

```
U-Boot 2013.01-00115-g831b30d (Jun 14 2013 - 21:48:56)

CPU0:  P2020E, Version: 2.1, (0x80ea0021)
Core:  E500, Version: 5.1, (0x80211051)
Clock Configuration:
       CPU0:1200 MHz, CPU1:1200 MHz,
       CCB:600  MHz,
       DDR:400  MHz (800 MT/s data rate) (Asynchronous), LBC:37.500 MHz
L1:    D-cache 32 kB enabled
       I-cache 32 kB enabled
Board: P2020RDB CPLD: V4.2 PCBA: V4.0
rom_loc: nor upper bank
SD/MMC : 4-bit Mode
eSPI : Enabled
I2C:   ready
SPI:   ready
DRAM:  Detected UDIMM(s)
1 GiB (DDR3, 64-bit, CL=6, ECC off)
DDR: 1 GiB (DDR3, 64-bit, CL=6, ECC off)
FLASH: 16 MiB
L2:    512 KB enabled
NAND: 128 MiB
MMC:  FSL_SDHC: 0
PCIe1: Root Complex of mini PCIe SLOT, no link, regs @ 0xffe0a000
PCIe1: Bus 00 - 00
PCIe2: Root Complex of PCIe SLOT, x1, regs @ 0xffe09000
  02:00.0     - 1095:3132 - Mass storage controller
PCIe2: Bus 01 - 02
In:    serial
Out:   serial
Err:   serial
Net:   eTSEC2 is in sgmii mode.
uploading VSC7385 microcode from ef000000
PHY reset timed out
eTSEC1, eTSEC2, eTSEC3
Hit any key to stop autoboot:  0
=> i2c dev 1
Setting bus to 1
=> i2c md 18 0
0000: 38 38 38 38 38 38 38 38 38 38 38 38 38 38 38 38
=> i2c mw 18 1 38
=> i2c mw 18 3 01
=> i2c md 18 0
0000: c8 c8 c8 c8 c8 c8 c8 c8 c8 c8 c8 c8 c8 c8 c8 c8
=> reset

U-Boot 2013.01-00115-g831b30d (Jun 14 2013 - 21:48:56)
```

```
CPU0:  P2020E, Version: 2.1, (0x80ea0021)
Core:  E500, Version: 5.1, (0x80211051)
Clock Configuration:
       CPU0:1000 MHz, CPU1:1000 MHz,
       CCB:500 MHz,
       DDR:333.333 MHz (666.667 MT/s data rate) (Asynchronous), LBC:25   MHz
L1:    D-cache 32 kB enabled
       I-cache 32 kB enabled
Board: P2020RDB CPLD: V4.2 PCBA: V4.0
rom_loc: nor upper bank
SD/MMC : 4-bit Mode
eSPI : Enabled
I2C:   ready
SPI:   ready
DRAM:  Detected UDIMM(s)
1 GiB (DDR3, 64-bit, CL=6, ECC off)
DDR: 1 GiB (DDR3, 64-bit, CL=6, ECC off)
FLASH: 16 MiB
L2:    512 KB enabled
NAND: 128 MiB
MMC:  FSL_SDHC: 0
PCIe1: Root Complex of mini PCIe SLOT, no link, regs @ 0xffe0a000
PCIe1: Bus 00 - 00
PCIe2: Root Complex of PCIe SLOT, x1, regs @ 0xffe09000
  02:00.0     - 1095:3132 - Mass storage controller
PCIe2: Bus 01 - 02
In:    serial
Out:   serial
Err:   serial
Net:   eTSEC2 is in sgmii mode.
uploading VSC7385 microcode from ef000000
PHY reset timed out
eTSEC1, eTSEC2, eTSEC3
Hit any key to stop autoboot:  0
=>
```

23.5.3 Uboot steps for overriding on-board switch to change NOR boot bank

1. First change to the correct I2C bus
    - => i2c dev 1
    - Setting bus to 1
2. A read of the input register will return the current state of the on-board switches.
    - => i2c md 18 0
    - 0000: 38 38 38 38 38 38 38 38 38 38 38 38 38 38 38 38

    The register value shows that FBANK_SELECT on IO1 is zero, thereby the switch SW3[8] is set to OFF and the U-Boot is stored in the upper NOR boot bank now.
3. Set the FBANK_SELECT IO1 bit to one , thereby selecting the lower bank upon reset.
    - => i2c mw 18 1 02

4. Next, set the appropriate pin IO1 as outputs.
    - => i2c mw 18 3 fd
5. A read will return the current over-written value that will be used for all subsequent resets.
    - => i2c md 18 0
    - 0000: 3a 3a 3a 3a 3a 3a 3a 3a 3a 3a 3a 3a 3a 3a 3a 3a
6. Use U-Boot command to reset the system.
    - reset

NOTE

This value will be used until either the power is turned off, or until the pins from the I2C device are tri-stated (....register 3 written as follows=> i2c mw 18 3 FF)

24 Getting Started

This section describes how to boot the P2020RDB. The on-board flash memory is preloaded with a flash image from the factory. The on-board switches and jumpers are set to the factory defaults.

CAUTION

Avoid touching areas of integrated circuitry and connectors; static discharge can damage circuits.

WARNING

Turn OFF power during insertion and removal of any PCIe card and USB TAP.

24.1 External Cable Connections

Connect the serial port of the P2020RDB system and a host computer using an RS-232 cable. Also, connect the AC cable into the backside of the chassis.

24.2 Serial Port Configuration (PC)

Before powering up the P2020RDB, configure the serial port of the attached computer with the following values:

- Data rate: 115200 bps
- Number of data bits: 8
- Parity: None
- Number of Stop bits: 1
- Flow Control: Hardware/None

24.3 Power Up

Do not turn power on until all cables are connected and the serial port is configured as described previously. Once done, power up the unit by pressing the power button on the backside of the chassis. A few seconds after power up, the U-Boot prompt should be received by the serial terminal program like the example below:

```
U-Boot 2013.01-00115-g831b30d (Jun 14 2013 - 21:48:56)

CPU0:  P2020E, Version: 2.1, (0x80ea0021)
Core:  E500, Version: 5.1, (0x80211051)
Clock Configuration:
      CPU0:1200 MHz, CPU1:1200 MHz,
      CCB:600  MHz,
      DDR:400  MHz (800 MT/s data rate) (Asynchronous), LBC:37.500 MHz
L1:    D-cache 32 kB enabled
      I-cache 32 kB enabled
Board: P2020RDB CPLD: V4.2 PCBA: V4.0
rom_loc: nor upper bank
SD/MMC : 4-bit Mode
eSPI : Enabled
I2C:   ready
SPI:   ready
DRAM:  Detected UDIMM(s)
1 GiB (DDR3, 64-bit, CL=6, ECC off)
DDR: 1 GiB (DDR3, 64-bit, CL=6, ECC off)
FLASH: 16 MiB
L2:    512 KB enabled
NAND: 128 MiB
MMC:  FSL_SDHC: 0
PCIe1: Root Complex of mini PCIe SLOT, no link, regs @ 0xffe0a000
PCIe1: Bus 00 - 00
PCIe2: Root Complex of PCIe SLOT, x1, regs @ 0xffe09000
  02:00.0     - 1095:3132 - Mass storage controller
PCIe2: Bus 01 - 02
In:    serial
Out:   serial
Err:   serial
Net:   eTSEC2 is in sgmii mode.
uploading VSC7385 microcode from ef000000
PHY reset timed out
eTSEC1, eTSEC2, eTSEC3
Hit any key to stop autoboot:  0
=>
```

25 Revision History

Table 26 provides a revision history for this document.

Table 26. Document Revision History

Rev. Number	Date	Description
0	1/2011	First draft
1.0	7/2011	Initial release
2.0	10/2011	Release for production board (PCB rev4.0, CPLD rev4.1).
2.1	2/2012	Revise SW2[6] description on Table 21
2.2	7/2013	Change NAND flash to 128Mbyte because original nand flash is EOL. CPLD revision move to rev4.2.

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