Rev. 1.4
09/99

MPC8xx ATM Supplement

to the MPC860/MPC850 PowerQUICC™ User's Manual

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Chapter 1
Overview

This chapter provides an overview of the features of the MPC860SAR and the differences between the 860SAR and the MPC860. This document also serves as the programming/ design model for use with the MPC850SAR. Differences between the MPC850SAR and the MPC860SAR are detailed later in this chapter.

1.1 MPC860SAR Capabilities

The MPC860SAR is a member of the MPC860 PowerQUICC™ family. In addition to the standard MPC860MH capabilities, the 860SAR includes the universal test & operations PHY interface for ATM (UTOPIA), AAL5 and AAL0 segmentation and reassembly (SAR) functionality, an ATM pace controller (APC) and transmission convergence (TC) sublayer for E1/DS1 and xDSL implemented by the serial channels.

These features make the 860SAR a very adaptable ATM SAR controller that can be used for a variety of ATM applications. Several examples follow:

- ATM line card controllers
- ATM to WAN interworking (frame relay, T1/E1 circuit emulation, ADSL applications)
- Residential broadband network interface units (ATM-to-Ethernet)
- High performance set-top controller
- ATM25 SAR

Since the 860SAR implements a superset of the ATOM1 microcode, the 860SAR supports ATOM1 features in addition to providing SAR functionality.

1.2 Comparison with the MPC860

The 860SAR is pin compatible with the MPC860 and both controllers can be used in identical applications with some small but significant programming changes made to accommodate the controllers' differences. The MPC860 and MPC860SAR have identical electrical and mechanical specifications.

1.2.1 Microcode Changes

A significant part of the 860SAR ATM functionality is implemented by the communications processor (CP) module using certain internal ROM space. In order to make that space available, the DSP library routines (for example, FIR, IIR) have been removed, and therefore the DSP functionality described in the User's Manual for the standard MPC860 is not available in the 860SAR.

1.2.2 Functionality Limitations Due to Internal Resources

1.2.2.1 General Issues

Timer 4 is used by the ATM Pace Controller to periodically activate the APC pace algorithm. Therefore, if ATM is enabled (i.e. PDPAR[ATM]=1), then timer 4 cannot be used for its normal function, but must instead be used as the APC timer.

Also, because of a required setting of the RCCR, IDMA2 can only be used in level-sensitive mode if ATM is enabled.

1.2.2.2 Issues Concerning the UTOPIA Interface

The UTOPIA interface of the MPC860SAR is implemented using the hardware of IDMA1 and the parameter RAM page of SCC4. Therefore, if the UTOPIA port of the 860SAR is used:

- SCC4 is unavailable (due to the loss of parameter RAM page 4)
- IDMA1 is unavailable (due to the loss of handshake signals and event registers)

1.2.2.3 Issues Concerning the ATM Pace Controller (APC)

The MPC860SAR contains an ATM Pace Controller (APC) which is used to automatically multiplex and schedule ATM cells for transmission. Most applications will use the APC, so these limitations will apply to most designs. The APC can be disabled simply by disabling Timer 4. However, if the APC is used, then only the following options are available:

- the UTOPIA port can be used (and SCC4 will be unavailable)
- SCC4 can be used in ATM mode
- SCC4 can be used in transparent mode
- SCC4 can be disabled

SCC1, SCC2, and SCC3 can be used in any mode desired, including ATM.

A detailed explanation of the technical reasons for this is provided in Section 5.4, "Using the APC Without Using SCC4 or UTOPIA".

1.2.3 Functionality Limitations Due to Pin Multiplexing

If the MPC860SAR's UTOPIA interface is used, then several existing pins are used as UTOPIA data and control signals, and therefore some of those pins' alternate functions

become unavailable. Most of the UTOPIA signals are multiplexed with the port D signals.

If the UTOPIA port is used, then:

- IDMA1 is unavailable (due to the loss of the $\overline{\text{DREQ0}}$ signal).
- Ethernet CAM support for SCC2, SCC3, and SCC4 is unavailable (due to the loss of the $\overline{\text{REJECT2}}$, $\overline{\text{REJECT3}}$, and $\overline{\text{REJECT4}}$ signals)
- Parallel Interface Port (PIP) is unavailable (due to the loss of the PIP handshake signals)

The SCC3 and SCC4 signals on port D are also optionally available on ports A, B, and C. Therefore, SCC3 will be available even if the UTOPIA port is used. SCC4 will still not be available when the UTOPIA port is used, because of the resource conflicts explained above.

1.3 Features

The 860SAR supports the following features:

- Serial ATM capability available on any SCC
- Optional UTOPIA port available (replaces SCC4 if used)
- Cell processing up to 60 Mbps aggregate receive and transmit via UTOPIA interface (with 50 MHz system clock).
- Cell processing up to 20 Mbps aggregate receive and transmit via serial interface (with 50 MHz system clock)
- Memory-to-memory cell processing (via serial interface in loopback)
- Performs transmission convergence (TC) to E1/T1/ADSL serial lines.
- Support of AAL0 and AAL5 protocols on a per virtual circuit (VC) basis.
- AAL0 support allows other AAL types to be handled by software.
- Support for 32 active VCs internally, and up to 64K using external memory.
- Cell multiplexing and demultiplexing.
- Flexible and efficient cell rate pacing; supports CBR and UBR, with easy hook-up to ABR.
- Supports UTOPIA and serial (E1/T1/ADSL) interfaces.
- Compliant with ATMF UNI 4.0 specification.
- CLP and congestion indication marking.
- Separate transmit and receive buffer descriptor (BD) rings for each channel.
- Interrupt report per channel using exception queue.
- Supports 53 byte to 64 byte (expanded) ATM cell size.
- Glueless serial interface to Motorola CopperGold ADSL interface device.
- Supports AAL5 connections:
  - Reassembly:
    - Reassembles CPCS_PDU directly to host memory

- CRC32 check
- CPCS_PDU padding removal
- CS_UU, CPI, and LENGTH reporting
- CLP and congestion reporting
- Interrupt per buffer or per message
- Report on errors (CRC, length mismatch, message abort)
- Real-time time stamp capability supports connection timeout

— Segmentation:
- Segments CPCS_PDU directly from host memory
- Performs CPCS_PDU padding.
- CRC32 generation
- Automatic last cell marking (in the PTI field of the cell header)
- Automatic CS_UU, CPI, and LENGTH insertion (in the last cell)

• Supports AAL0 connections:

— Receive:
- Whole cell is stored in memory (with exception of the HEC).
- CRC10 pass/fail indication
- Interrupt per buffer (cell)

— Transmit:
- Reads a whole cell (with exception of the HEC) from the buffer.
- Optional CRC10 insertion

• PHY:

— UTOPIA provides glueless interface to PHY
- UTOPIA level 1 master (ATM side) with cell-level handshake
- Supports use of external logic to implement UTOPIA level 2 multi-PHY interface (for up to 4 PHY)

— T1/E1/ADSL serial line
- HEC generation/checking
- Cell delineation
- Cell payload scrambling/de-scrambling option ($X^{43}+1$ polynomial)
- Automatic idle/un-assigned cell insertion/stripping
- Cells with incorrect HEC are marked and counted.

• ATM pace control (APC) unit:

— 2 priority levels

— Constant bit rate (CBR) pacing on a per VC basis

— Unspecified bit rate (UBR) pacing

— Available bit rate (ABR) pacing (pace is managed by the host)

• Receive address look-up supported by three modes of operation:

— Sequential look-up table (for up to 32 channels in internal mode)
— Flexible, user-defined address compression mechanism.
— Content-addressable memory (CAM).

Figure 1-1 shows a typical 860SAR configuration for support of serial and UTOPIA mode ATM transmissions. A description of the 860SAR's serial and UTOPIA mode transmit, receive, and transmission scheduling capabilities for AAL0 and AAL5 cell types is provided in subsequent sections.

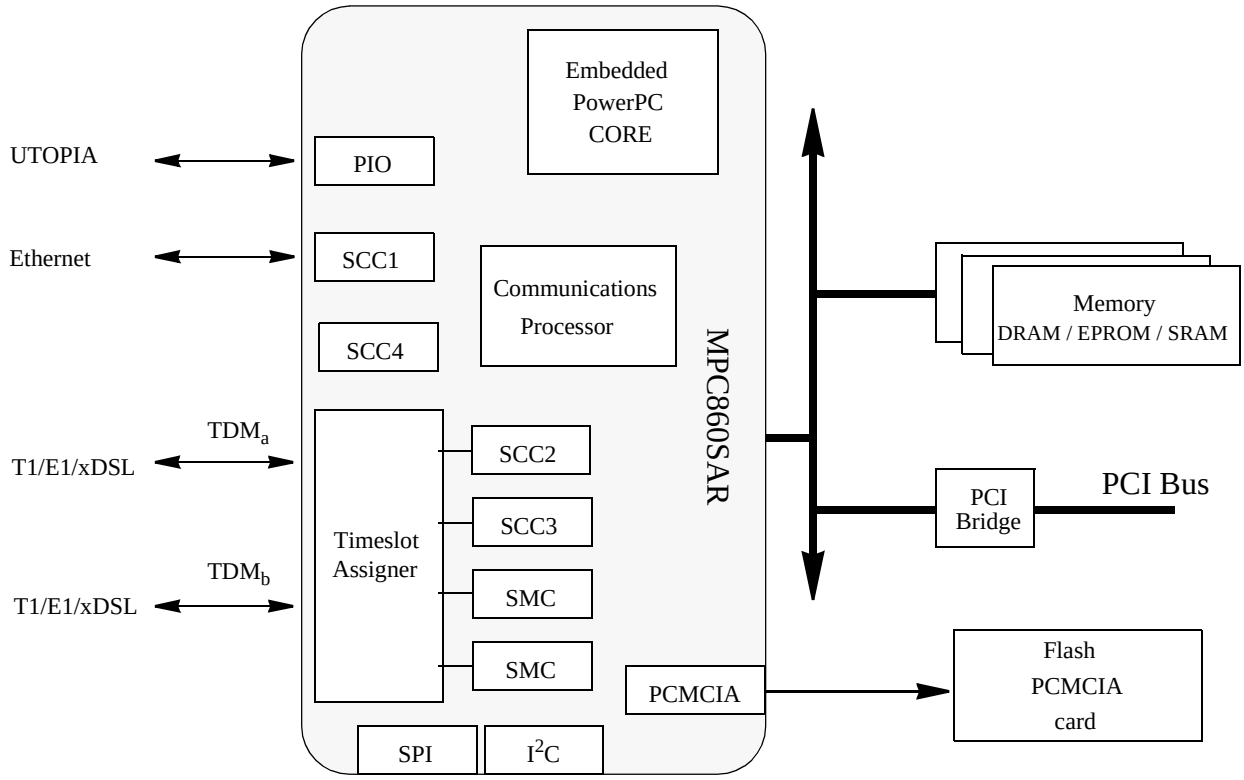


Figure 1-1. MPC860SAR Application Example

1.4 MPC860SAR and MPC850SAR Comparison

The MPC850SAR is a cost reduced version of the MPC860SAR. There are less SCCs available on the MPC850SAR. The programming model for the MPC850SAR is for the most part identical to the MPC860SAR and therefore most everything in this supplement applies to the MPC850SAR, except:

- SCC4 is not available. However, the parameter RAM page associated with SCC4 is still available in DPR. This parameter RAM page is used by the UTOPIA port.
- The pinout is different. Signal functionality is the same for both parts, but pin multiplexing is different.

The “UTOPIA Interface” chapter of this document contains a table with MPC850SAR pin assignment/definitions. For a complete description of the MPC850 refer to the MPC850 User’s Manual.

1.5 General Description

The 860SAR’s ATM controller supports several ATM sublayers and two interface modes of operation. The interface modes provide a UTOPIA interface and a serial interface. In both modes the ATM controller performs ATM adaptation layer (AAL5 and AAL0), segmentation and reassembly (SAR), and the ATM layer protocol function. In the UTOPIA mode, the ATM layer interfaces the PHY directly through the UTOPIA interface. In serial mode, the ATM controller also implements the transmission convergence (TC) sublayer and interfaces the PHY through its SCCs.

As mentioned above, the PHY interface to the ATM controller is through UTOPIA or a bit stream from the TC layer. The ATM controller also performs the AAL SAR on the user data as it is transmitted and received. The transmitted and received data resides in system memory in single or multiple data buffers.

The following sections describe the transmit and receive mechanisms for the two modes and the functionality of the ATM pace controller (APC), which is common to the two modes. Detailed information for the two modes of operation can be found in Chapter 7, “Interface Configuration.” Detailed information about the APC can be found in Chapter 5, “ATM Pace Control.” For proper operation of the 860SAR, SCC4 must be included as a channel used for either serial or UTOPIA mode ATM transactions; if only one channel is selected for ATM operations, SCC4 must be the channel configured for use.

1.5.1 ATM Controller UTOPIA Mode

In the UTOPIA mode, the 860SAR handles receive and transmit operations on a cell-by-cell basis. The UTOPIA interface implements cell-level handshake and therefore the supported bit rate is higher than the bit rate accomplished in the serial mode.

1.5.1.1 Transmitter Overview

The transmit process begins with the APC. The APC controls the ATM traffic of the transmitter through a user-configured timer that defines the maximum outgoing bit rate. The APC holds the traffic parameters of each channel and divides the total bit rate amongst the requesting channels. It can provide CBR and UBR traffic services. ABR can also be supported through software manipulation of APC parameters. The task of the APC is to define the next channel (or channels) to be transmitted. Refer to Chapter 5, “ATM Pace Control,” for additional information about the operation and programming of the APC.

The APC schedules channels for transmission by inserting the channel number in the transmit queue. If a channel is in the transmit queue and the PHY asserts the transmit cell available (TxCav) signal, the transmitter starts the transmit process. At first, the transmitter takes the first channel number from the transmit queue. The channel number determines

which channel entry is read in the transmit connection table (TCT). The transmitter then checks the status of the specific connection. If there is no open data buffer, it opens a new transmit buffer using the channel's buffer descriptor (BD) list. The APC then copies 48 octets from the external buffer, performs CRC32 for AAL5, copies the cell header from the cell header entry of the TCT, and transmits the whole cell through the UTOPIA interface.

At the last cell of an AAL5 frame, the transmitter appends to the user frame the trailer of the common part conversion sublayer-protocol data unit (CPCS-PDU). It adds pads as required, appends the length (calculated during the frame transmit), and copies the CPCS-UU and CPI from the BD. The transmitter also sets the PTI[1] bit at the header of the last cell of the message. An interrupt is optionally generated to declare the end of transmit frame.

During AAL0 transmissions the ATM controller simply copies the whole cell (except the HEC) prepared by the user from the channel's buffer and transmit it through the UTOPIA interface. Note that the HEC is not generated by the 860SAR in UTOPIA mode. The transmit HEC transferred to the UTOPIA interface is a dummy byte value (set to 0x00), and the PHY is responsible for the calculation of the HEC. The ATM controller can optionally generate CRC10 on the cell payload and place the result at the end of the payload (CRC10 field). This feature is used to support OAM CRC10; refer to ITU specification I.610 for additional details.

If no additional valid buffers are available for the requesting channel in the BD list, the transmit process ends and no cell is transmitted by the 860SAR. It is the responsibility of the PHY to generate an idle cell in an empty cell slot. An empty cell slot is generated every time this channel is scheduled by the APC until a new valid buffer is ready, or a deactivate channel command is issued. See Section 4.3, "MPC860SAR Commands," for additional information about ATM controller commands and syntax.

1.5.1.2 Receiver Overview

The receive process begins when the PHY asserts the receive cell available signal (RxCav), indicating that the PHY has a complete cell in its receive FIFO buffer.

The 860SAR begins processing the cell by receiving the cell header through the UTOPIA interface. The receiver translates the header address (VCI/VPI/PTI) to a channel number through either a look-up table in dual-port RAM, address compression tables in external RAM, or an external content-addressable memory (CAM). A cell header that has no match is treated as an AAL0 cell and is passed to the global raw cell queue (channel 0). If the cell is matched to a channel, the channel status is read from the receive connection table (RCT), and if no open buffer is available a new buffer is opened. The payload (48 octets) is copied to the buffer, the CRC is calculated, and the RCT parameters are updated. If no empty buffers are available for the received channel in the BD list an interrupt is generated and the cell is discarded.

On receipt of an AAL5 end-of-frame marker (indicated by the PTI[1] bit) the receiver separates the trailer of the CPCS-PDU from the user data. The pads are removed as

required, the length field is checked against the length which was calculated during the frame receive, the CPCS-UU and CPI are copied to the BD, and the buffer is closed. An interrupt is optionally generated to declare the end of received frame. If a CRC or length error occurs, it is marked in the BD and an interrupt is generated. AAL5 frames longer than 65535 octets will result in a CRC error and the contents of the “Data Length” field of the BD will contain (length of frame)MODULO(0xffff).

On receipt of an AAL0 cell the ATM controller simply copies the whole cell (with the exception of the HEC) from the UTOPIA interface to the channel’s current buffer, and calculates and checks CRC10 on the cell payload. This option is used to support OAM cell check per ITU specification I.610. Note that the received HEC is not checked by the 860SAR in UTOPIA mode. It is the responsibility of the PHY to check the HEC and discard cells with an incorrect HEC.

1.5.2 ATM Controller Serial Mode

The 860SAR’s serial controllers operate independently of the physical interface standard used. The physical interface must provide a synchronization signal to define the byte boundary of the receive and transmit data streams to the 860SAR, so that it can deliver and accept byte-aligned data to or from the 860SAR serial interface. This byte synchronization signal is particularly important to the serial receiver, which cannot achieve cell synchronization without it. Generally, one of the 860SAR TDM ports is used in the serial mode to allow easy connection to an E1 or T1 line interface device. However, the use of the other serial interfaces, using either the TDM ports or the NMSI mode of the SCC, is also possible. The operation of the TDM interface using the time slot assigner (TSA) is described in subsequent sections.

While operating in serial mode, the transmit and receive flows are similar to those when operating in UTOPIA mode. In addition to the functionality of the UTOPIA mode, the serial mode provides the transmission convergence (TC) layer which adds cell delineation, scrambling, idle cell generation or screening, and defines the interface characteristics for support of E1/T1 or ADSL line interface devices.

1.5.2.1 Transmitter Overview

The serial transmitting process begins with the APC. The APC controls the ATM traffic of the transmitter through a user-configured timer that defines the maximum outgoing bit rate. The APC holds the traffic parameters of each channel and divides the total bit rate amongst the requesting channels. It can provide CBR and UBR traffic services. ABR can also be supported through software manipulation of APC parameters. The task of the APC is to define the next channel (or channels) to be transmitted. Refer to Chapter 5, “ATM Pace Control,” for additional information about the operation and programming of the APC.

When operating in serial mode, transmit requests are generated by an SCC. The transmitter determines the next channel from the transmit queue for the current SCC, reads the channel data from the transmit connection table (TCT), and updates the TCT. The cell is copied to an internal buffer where the CRC32 and HEC are calculated, the cell header is appended,

and scrambling is optionally performed. After the cell assembly process, the cell is moved into the SCC's transmit FIFO for transmission.

The transmitter appends the trailer of the CPCS-PDU in the last cell of an AAL5 user frame. The CPCS-PDU consists of the frame length (which was calculated during the frame transmit), the CPCS-UU and CPI fields from the BD, and cell padding as required. The transmitter also sets the PTI[1] bit in the header of the last cell of the frame. An interrupt can be optionally generated to declare the end of a transmit frame.

When transmitting AAL0 cells the ATM controller simply copies the whole cell (except the HEC) from the channel's cell transmit buffer. The ATM controller optionally generates CRC10 for the cell payload and places the result at the end of the payload. This feature is used to support OAM CRC10 per ITU specification I.610.

In the event of an empty transmit queue or no valid BDs for the requesting channel in the BD list, the transmitter generates an idle or unassigned cell (with the cell contents defined by the user). The transmitter sends idle cells if there are no channel numbers in the transmit queue or if the current channel in the transmit queue has no valid buffers. Channels can be removed from the transmit queue with the deactivate channel command. For additional information about ATM controller commands, refer to Section 4.3, "MPC860SAR Commands."

1.5.2.2 Receiver Overview

The receive process starts after the receiver becomes synchronized with the incoming cells and can perform cell delineation. A receive request is then generated by an SCC. The receiver copies the first word from the serial controller to the dual-port RAM (DPR). The receiver translates the header address (VCI/VPI/PTI) to a channel number through either a look-up table in dual-port RAM, address compression tables in external RAM, or an external content-addressable memory (CAM). If the header has no match the incoming cell is treated as an AAL0 cell, and is passed to the global raw cell queue (channel 0). If the cell is matched to a channel the channel status is read from the receive connection table (RCT). As the FIFO of the serial controller fills, the received cell is read from the FIFO of the serial controller, the HEC is checked, and cell descrambling is optionally performed. Cells with HEC errors are passed to the global raw cell queue, and the HEC error is recorded in the BD. The receiver will screen out either idle cells or unassigned cells, as programmed.

Throughout the cell assembly process, either the entire cell (for AAL0 connections) or the cell payload (for AAL5 connections) is copied to external memory through DMA bursts and the RCT is updated. If there are no empty buffers for the received channel in the BD list, an interrupt is generated and the cell is discarded.

CRC32 is checked on the cell payload for AAL5 connections, with pass/fail indication provided in the last BD of the received CPCS_PDU. The end of an AAL5 frame is indicated by the PTI[1] bit in the received cell header. When an end-of-frame indication occurs the receiver separates the trailer of the CPCS-PDU from the user data. The length field is compared against the length calculated during the frame receive operation, the pads are

removed as required, the CPCS-UU and CPI are copied to the BD, and the receive buffer is closed. An interrupt can be optionally generated to declare the end of a receive frame. Detected CRC or length errors are marked in the BD and an interrupt is generated. AAL5 frames longer than 65535 octets will result in a CRC error and the contents of the “Data Length” field of the BD will contain (length of frame)MODULO(0xffff).

When AAL0 cells are received the ATM controller simply copies the whole cell from the serial controller without the HEC to the next receive buffer in the channel’s BD list. The ATM controller calculates and checks CRC10 on the cell payload. This option supports the OAM cell check per ITU specification I.610.

1.5.2.3 Cell Delineation

In serial mode cell delineation is part of the receiver flow control. The user must provide synchronization signals to the 860SAR and octet-align incoming cells to the synchronization signals. The ATM controller provides SDH/PDH oriented cell delineation on an octet basis using the HEC mechanism defined in ITU specification I.432. Note that when using E1 and T1 ATM links, the cells are always octet-aligned (refer to ITU specification G.804) and synchronization signals are provided by the E1 and T1 interface devices.

When cell reception commences, the ATM controller takes a short while to acquire correct cell delineation. Once the ATM controller has locked to the incoming cell stream, it remains locked unless there are excessive errors. A status bit indicates the current delineation status, and an interrupt is generated whenever the cell lock status changes. Cells received before the cell delineation process has completed will be stored in the global raw cell queue.

1.5.2.4 Cell Payload Scrambling

Cell payload scrambling is optionally performed in both transmit flow (scrambling) and receive flow (descrambling) using the $X^{43}+1$ scrambling algorithm. The first cell transmitted following initialization is not correctly scrambled because there is no valid data in the 43-bit delay line. The ATM controller always transmits an empty cell first thereby avoiding data corruption. On cell reception, the descrambling algorithm self-synchronizes before the HEC delineation process is complete and cell reception begins.

1.5.3 Extended Channel Mode

In extended mode the number of connections supported by the ATM controller is increased from 32 transmit and receive channels up to 65,535 transmit and receive channels. When extended mode is invoked the TCT and RCT structures greater than 31 are placed in the external memory and a CAM or address compression method is used for VCI/VPI/PTI mapping instead of an internal look-up table. In this case parameters for “internal” channels (channels with an internal TCT and RCT; channels 0 through 31) are directly accessed in the dual-port RAM, and “external” channels (channels with TCTs and RCTs located in external memory) require DMA accesses to read and update the external TCT and RCT.

The bit rate supported by the extended mode is reduced and throughput depends on the number of external channels and the bit rate ratio between external and internal channels.

1.5.4 ATM Pace Control (APC)

The ATM pace controller determines the next channel (or *n* channels) to be transmitted and writes the channel number of these channels in the transmit queue every APC slot time. The transmitter transmits one cell for each channel entry in the transmit queue. The APC is controlled by the communications processor (CP) through a cyclic table (APC table) in the dual-port RAM that is used to schedule transmission of all the active channels.

The operation of the APC is controlled by several input parameters programmed by the user. Scheduling of traffic is controlled through the APC table length, the number of cells to be selected in an APC slot time, and the APC request timer. The period of the APC request timer determines the length of an APC slot time. The APC uses the APC_period parameter in the TCT to schedule the channel in the APC table.

The APC may optionally handle two APC tables. The first table is serviced with high priority and the second is serviced with a lower priority; thus, channels from the second table are scheduled on a bit rate availability basis. This capability is used for channels with higher cell delay variation (CDV) tolerance and for UBR traffic.

The APC_period for CBR traffic is set by the user prior to the activation command, and CBR transmissions are scheduled through the high-priority table. The APC_period for UBR transmissions is also constant, and is scheduled in the low-priority table. The APC_period of ABR transmissions is adjusted by the host in response to RM cell reception and defines the ABR available cell rate (ACR). The APC period can be changed on-the-fly, thereby allowing the bit rate for a channel to be changed dynamically, as is necessary to control transmission of traffic types such as ABR. For ABR, it is the user's responsibility to evaluate resource management (RM) cells and update the APC_period entry in the TCT.

The APC input parameters are described in Chapter 5, "ATM Pace Control." These parameters define the minimum and maximum cell rate and cell delay variation.

1.5.5 Expanded Cells

Typical ATM cells are 53 bytes long, consisting of a header (4 bytes), HEC (1 byte) and payload (48 bytes). The 860SAR also supports cells up to 64 bytes in length (referred to as expanded cells) that use extra header fields for internal information in switch applications. Expanded cells consist of an expanded header of 0 to 3 words (0, 4, 8, or 12 bytes), a cell header (4 bytes), and a payload (48 bytes); the HEC is not included as error checking is not required within a switch. Expanded cells are available only when operating in UTOPIA mode. Figure 1-2 shows the structure of an expanded cell.

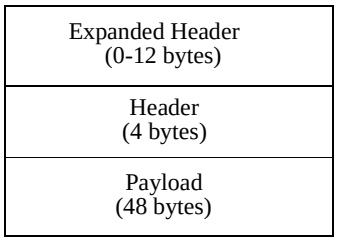


Figure 1-2. Expanded Cell Structure

During transmit operations, the expanded header of each cell is taken from the expanded field in the BD and transmitted ahead of the cell header and payload. During receive operations the expanded header of the last cell of the current connection is copied to the expanded field in the receiver's BD.

Chapter 2
Buffer Descriptor Structures and Connection Tables

The 860SAR's communication processor module (CPM) manages ATM traffic through the UTOPIA and serial interfaces by means of transmit and receive buffer descriptor (BD) structures and transmit and receive connection tables (referred to as TCTs and RCTs, respectively). Buffer descriptors are circular lists of pointers into transmit and receive buffer space in external memory. The following sections describe the organization and configuration of the buffer descriptors, TCTs, and RCTs.

2.1 Buffer Descriptors (BD)

ATM SAR operates as a multi-channel protocol, segmenting and reassembling each channel's transmit and receive data to and from different sets of memory buffers simultaneously. This behavior makes it necessary to have a separate list of BDs for each channel. The method implemented by the 860SAR ATM controller is based on the traditional 860 buffering methodology, with the difference that there are multiple BD lists which are located in the external memory. Each channel is configured with two BD lists for transmit and receive operations. The number of BDs according to channel and the size of the buffers is defined by the user. This method allows the 860SAR to perform segmentation and reassembly directly to the user memory and to better use available memory space. The 860SAR accesses BDs in list order. The BD list is a cyclic list; when the 860SAR reaches the last BD it returns to the head of the list.

Figure 2-1 shows an example of the transmitter BD lists and buffers and the pointers associated with them. In this example there are two transmit channels; channel 1 and channel 4. Each transmitting channel has a transmit BD list and an entry in the TCT where the BD pointers are placed (TBASE, TBD_PTR, and TB_PTR). TBDBASE and RBDBASE are the base addresses of the BD external memory spaces and are placed in the parameter RAM to identify separate blocks of memory for the receive and transmit BDs. TBASE holds the address offset from TBDBASE of the starting BD of a given channel. In this example, the first transmit BD of channel 1 is located at the address specified by TBD_BASE plus the offset specified by channel 1's TBASE. The TBD_PTR is an offset pointer inside a BD list specifying the current active BD.

In the example shown in Figure 2-1, when channel 1 receives a transmit request then a cell is transmitted from buffer 4 in its transmit BD list using TB_PTR of channel 1 as a pointer to the cell data. The transmitter advances the TB_PTR to point to the next cell data every time it transmits a cell for channel 1. When the end of a transmit buffer is reached, the transmitter advances the TBD_PTR to the next BD in the list and continues to transmit if the BD is valid. If the end of the BD list is reached, the transmitter returns to the head of the list by setting TBD_PTR to the TBASE address of the channel.

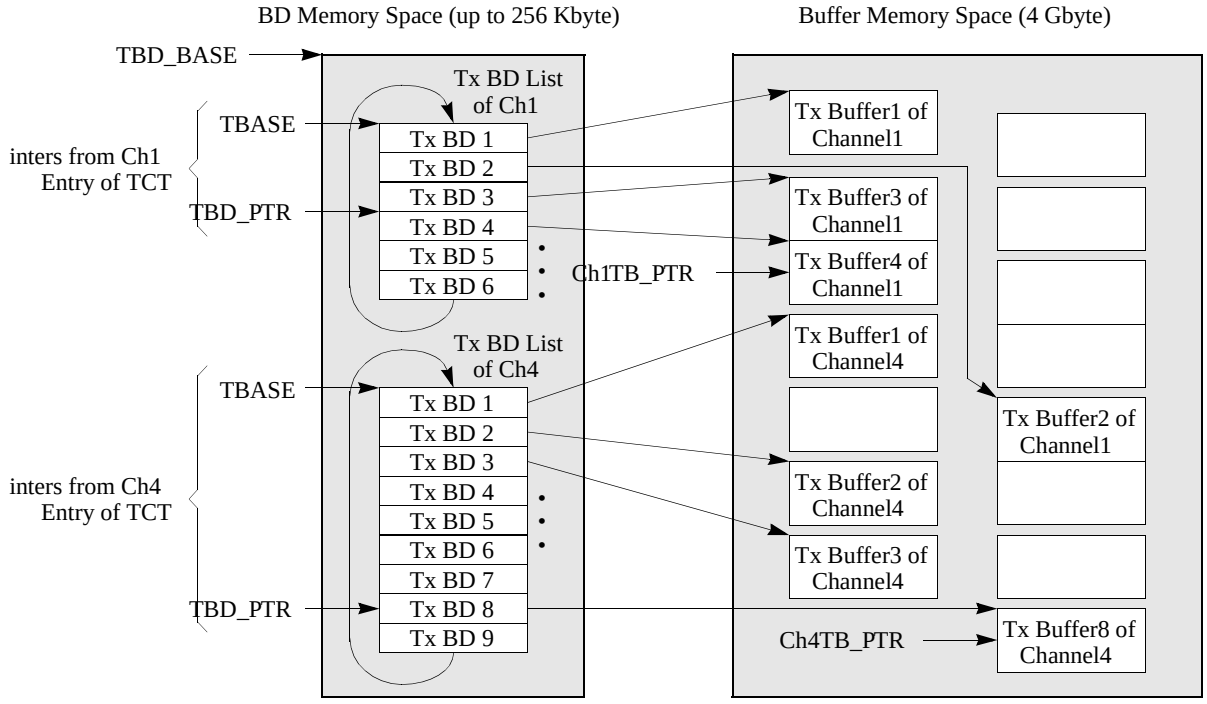


Figure 2-1. Transmit Buffer and BD List Example

2.1.1 AAL5 Buffers

The buffers used by the 860SAR may reside in either internal or external memory. Each buffer can hold a whole CPCS-PDU message or part of it. The buffers used by the 860SAR transmitter are accessed in BD list order; if more than one buffer for a message is used, all the BDs for the buffers should be in consecutive order in the BD list. The last buffer of a message is padded automatically by the 860SAR transmitter to fit an AAL5 cell payload according to ITU specification I.363. The transmit buffer data length for AAL5 transmit buffers must be greater than or equal to 48 bytes for all buffers except the first and last buffer of a CPCS-PDU; the first and last buffers of a CPCS-PDU must have a data length greater than zero. Note that AAL5 transmit buffers have no alignment restrictions.

Receive buffers can also hold either a whole CPCS-PDU message or part of it. Receive buffers must start on a burst-aligned address (divisible by 16) and their lengths can be any multiple of 48 bytes (that is, the value of SMRBLR in parameter RAM must equal N x 48, where N is an integer.) The receive BDs are used in order and in multiples of 48 bytes, except for the last buffer in a message from which the AAL5 pads are removed.

During transmit or receive operations, interrupts are optionally generated at the end of each BD or the end of an AAL5 CPCS-PDU.

2.1.2 AAL0 Buffers

During AAL0 operations each buffer contains one raw cell. When the receiver or transmitter completes writing or reading the buffer, it moves to the next buffer in the list and optionally issues an interrupt. The placement of an AAL0 cell in a buffer is shown in Figure 2-2.

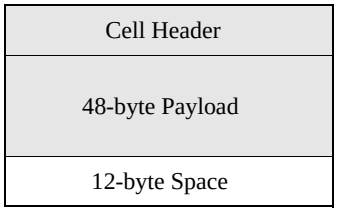


Figure 2-2. AAL0 Buffer Structure

An AAL0 buffer size is 64 bytes. 52 bytes of this buffer are used to hold cell header and payload; the HEC is not included in the receive or transmit buffers. The remaining 12 bytes of the buffer are not used by the 860SAR and are available to the user. Unlike other protocols, both the AAL0 transmit and receive buffers must start on a burst-aligned address (divisible by 16).

2.1.3 Receive Buffer Descriptor

The format of the receive buffer descriptor is applicable to both SAR UTOPIA and serial modes. The buffer descriptors are 12 bytes long in standard (53-byte) cell mode and 24 bytes long in expanded cell mode. In standard cell mode, the cell header expansion fields do not exist, and the buffer descriptor occupies a 12-byte region of memory, with the next buffer descriptor following immediately after it. Figure 2-3 describes the contents and memory locations of a receive buffer descriptor in expanded cell mode.

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
OFFSET + 0	E	—	W	I	L	F	CM	—	HEC	CLP	CNG	ABT	—	—	LN	CR
OFFSET + 2	DATA LENGTH															
OFFSET + 4	RX DATA BUFFER POINTER															
OFFSET + 8	CPCS-UU+CPI															
OFFSET + A	RESERVED															
OFFSET + C	CELL HEADER EXPANSION 1															
OFFSET + 10	CELL HEADER EXPANSION 2															
OFFSET + 14	CELL HEADER EXPANSION 3															

Note: Entries in boldface must be initialized by the user.

Figure 2-3. Receive Buffer Descriptor

Table 2-1 describes the control and status bits in a receive buffer descriptor.

Table 2-1. Receive Buffer Descriptor Field Descriptions

Offset from RBD_PTR	Bits	Name	Description
0x00	0	E	Empty. Determines whether a buffer is accessible by the CPU core or the CP. 0 The data buffer associated with this receive BD has been filled with the received data, or data reception has been aborted due to an error condition. The CPU core is free to examine or write to any fields of this receive BD. The CP will not access a BD while the E-bit is cleared to zero. 1 The data buffer associated with this RxBD is empty, or reception is currently in progress. This receive BD and its associated receive buffer are in use by the CP. Once the E bit is set, the CPU core should not write any fields of this receive BD.
	1	—	Reserved
	2	W	Wrap. Determines that this is the final BD in table. 0 This is not the last BD in the receive BD list of the current channel. 1 This is the last BD in the receive BD list of this current channel. After this buffer has been used, the CP will receive incoming data for this channel into the first BD in the list (the BD pointed to by the channels's RCT[RBASE] address). The number of receive BDs in this table is programmable and is determined only by the W bit and the overall space constraints of 256K memory space for all the receive channels.
	3	I	Interrupt. Enables RXB interrupts when a receive buffer is closed during receipt of an AAL5 frame or an AAL0 buffer. Note that RXF interrupts are not effected by this bit. 0 No interrupt is generated after this buffer has been used. 1 Interrupt occurs after this buffer has been closed by the ATM controller while processing an AAL5 frame. This class of interrupt is indicated through the setting of the RXB bit in an entry in the exception queue. The GINT bit in the ISDR or SCCE is set according to the INT_CNT counter value set in the parameter RAM.
	4	L	Last in frame. Set by the ATM controller when this buffer is the last in a frame. This implies the end of the CPCS-PDU by channels that implement AAL5, or reception of an error, in which case one or more error bits are set. The ATM controller writes the number of frame octets to the data length field. 0 The buffer is not the last in a frame. 1 The buffer is the last in a frame.
	5	F	First in frame. Set by the ATM controller when this buffer is the first in a frame. This bit is reserved in AAL0 BDs. 0 The buffer is not the first in a frame. 1 The buffer is the first in a frame.
	6	CM	Continuous mode. Determines whether the buffer associated with this BD is continuously marked as empty. 0 Normal operation 1 The E bit is not cleared by the CP after this BD is closed, allowing the associated data buffer to be automatically overwritten the next time the CP accesses this BD.
	7	—	Reserved

Table 2-1. Receive Buffer Descriptor Field Descriptions (Continued)

Offset from RBD_PTR	Bits	Name	Description
0x00	8	HEC	HEC error. A receiver HEC error occurred on at least one cell of the frame. Cells with HEC errors are passed to the global raw cell queue with this bit set.
	9	CLP	Cell loss priority. Indicates that at least one cell was received with CLP bit set. This bit is set in the last BD in the frame by the 860SAR for channels that implement AAL5. For channels that implement AAL0, this bit is not valid. The CLP bit can be found in the cell header (first word) of the AAL0 received data buffer.
	10	CNG	Congestion indication. Indicates that the last cell in the frame was received with PTI congestion bit set. This bit is set in the last BD of the frame by the 860SAR for channels that implement AAL5. For channels that implement AAL0, this bit is copied from the PTI bit in the header of the received cell.
	11	ABT	Abort. Indicates that a frame abort was detected (last cell in frame indicated zero frame length.) This error bit is set in the last BD of the aborted frame by the 860SAR for channels that implement AAL5.
	12–13	—	Reserved
	14	LN	Receive length error. The number of octets received in the frame does not match the length specified in the length field of the AAL5 CPCS-PDU. This bit is set in the last BD of the frame by the 860SAR for channels that implement AAL5. Note that the whole received PDU is written to the data buffer even if a receive length error is detected.
	15	CR	Receive CRC error. This bit indicates a CRC32 error for AAL5 channels or a CRC10 error for AAL0 channels. The receiver performs CRC32 checking on the CPCS-PDU for AAL5 channels and sets the CR bit in the last BD when a CRC error is detected. On AAL0 channels, the receiver performs CRC10 checking on the cell payload. It will set the CR bit if a CRC error is detected. 0 No error 1 Indicates CRC32 error for AAL5 channel and CRC10 failure for AAL0 channel. Note: CRC10 checking is performed for all AAL0 channels. The CR bit is set when the received cell includes a CRC10 field in the cell payload and an error is detected. This check is provided to support OAM CRC10 according to ITU specification I.610.
0x02	—	Data length	Data length. For AAL5 BDs, the data length is the number of octets written by the CP into the BD's data buffer. When the BD is the last BD in the frame (indicated by the BD[L] bit set to 1), the data length contains the total number of frame octets. This field is written by the CP as the buffer is closed. For AAL0 BDs the data length field is reserved. Note: The amount of memory allocated for all the receive buffers should be greater than or equal to the memory size specified in the SMRBLR field in parameter RAM.
0x04	—	Receive data buffer pointer	Receive data buffer pointer. The receive buffer pointer always points to the first location of the data buffer, which may reside in either internal or external memory. This pointer is specified by the host process, and must be burst aligned (divisible by 16).
0x08	—	CPCS-UU and CPI	CPCS-UU and CPI. This field contains the CPCS-UU and CPI fields received from the SAR. This field is transferred from the CPCS-PDU trailer, and contains user-to-user (UU) information and common part indications (CPI). This field is written by the 860SAR and is valid only when the BD is the last BD in the frame, and is applicable only to AAL5 channels.

Table 2-1. Receive Buffer Descriptor Field Descriptions (Continued)

Offset from RBD_PTR	Bits	Name	Description
0x0C	—	Cell header expansion 1, 2, and 3	Cell header expansion 1, 2, and 3. These fields are added to the BD when expanded cells are enabled by the user (SRSTATE[EC] bit is set in parameter RAM). When expanded cell headers are enabled and the last BD of an AAL5 frame is closed, the 860SAR copies the expanded cell header into this field; cell header expansion 1 is the first word to be received, cell header expansion 3 is the last word to be received. When expanded cell headers are enabled for AAL0 channels, the expanded cell headers will be copied into these fields for every receive BD. The bytes are ordered according to the DMA byte ordering (programmed through the SRFCR field in the parameter RAM). If the ECSIZE field in the parameter RAM is set to a value less than 3, the cell header expansion fields are populated with the number of words specified in ECSIZE.

2.1.4 Transmit Buffer Descriptor

Data is prepared for transmission by the ATM controller by arranging it in buffers referenced by the channel's transmit BD list. The ATM controller confirms transmission or indicates error conditions using the BDs to inform the host that the buffers have been serviced. The format of the transmit buffer descriptor is applicable for both SAR UTOPIA and serial modes. The buffer descriptors are 12 bytes long in standard (53-byte) cell mode and 24 bytes long in expanded cell mode. In standard cell mode, the cell header expansion fields do not exist, and the buffer descriptor occupies a 12-byte region of memory, with the next buffer descriptor following immediately after it. Figure 2-4 describes the contents and memory locations of a transmit buffer descriptor.

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
OFFSET + 0	R	—	W	I	L	—	CM	—	—	—	—	—	—	—	—	—
OFFSET + 2	DATA LENGTH															
OFFSET + 4	TX DATA BUFFER POINTER															
OFFSET + 8	CPCS-UU+CPI															
OFFSET + A	RESERVED															
OFFSET + C	CELL HEADER EXPANSION 1															
OFFSET + 10	CELL HEADER EXPANSION 2															
OFFSET + 14	CELL HEADER EXPANSION 3															

Note: Entries in boldface must be initialized by the user.

Figure 2-4. Transmit Buffer Descriptor

Table 2-2 provides a description of the control and status bits in a transmit buffer descriptor.

Table 2-2. Transmit Buffer Descriptor Field Descriptions

Offset from TBD_PTR	Bits	Name	Description
0x00	0	R	Ready. Determines whether the data buffer is ready for transmission. 0 The data buffer associated with this BD is not ready for transmission. The CPU core is free to manipulate this BD or its associated data buffer. The CP clears this bit after the buffer has been transmitted or after an error condition is encountered. 1 The data buffer, which has been prepared for transmission by the user, has not been transmitted or is currently being transmitted. No fields of this BD may be written by the CPU core once this bit is set.
	1	—	Reserved
	2	W	Wrap. Determines whether this is the final BD in the table. 0 This is not the last BD in the transmit BD table. 1 This is the last BD in the transmit BD list for the current channel. After the contents of this buffer have been transmitted, the CP continues transmitting outgoing data for the current channel from the first BD in the list (the BD pointed to by TBASE in the TCT). The number of transmit BDs in the table is programmable and is limited by the 256K memory space for all the transmit and receive channels.
	3	I	Interrupt. Determines whether an interrupt is generated when the contents of the buffer have been transmitted. 0 No interrupt is generated after the buffer has been transmitted. 1 The TXB bit is set in an entry in the exception queue after the buffer has been transmitted. The GINT bit in the IDSR or SCCE is set according to the INT_CNT counter value set in the parameter RAM.
	4	L	Last. Determines whether the buffer is the last in an AAL5 frame. 0 This is not the last buffer in the transmit frame. 1 This is the last buffer in the current transmit frame.
	5	—	Reserved.
	6	CM	Continuous mode. Determines whether the buffer associated with this BD is continuously marked as ready for transmission. 0 Normal operation 1 The R bit is not cleared by the CP after this BD is closed, allowing the associated data buffer to be automatically retransmitted the next time the CP accesses this BD.
	7–15	—	Reserved
0x02	—	Data length	Data length. The data length field specifies the number of octets the ATM controller should transmit from this BD's data buffer. The value in this field is not modified by the CP. The value of this field must follow the guidelines in section 2.1.1 "AAL5 Buffers", or section 2.1.2 "AAL0 Buffers", as appropriate.
0x04	—	Transmit data buffer pointer	Transmit data buffer pointer. The transmit buffer pointer contains the address of the associated data buffer. The buffer may reside in either internal or external memory. This value is not modified by the CP.

Table 2-2. Transmit Buffer Descriptor Field Descriptions (Continued)

Offset from TBD_PTR	Bits	Name	Description
0x08	—	CPCS-UU and CPI	CPCS-UU and CPI. This field is used to transfer to the SAR the CPCS-UU and CPI fields. These fields are used in the CPCS-PDU trailer to transfer user-to-user (UU) information and common part indications (CPI). This field is applicable only for AAL5 channels. When the BD is the last BD in the frame the transmitter will copy this field to the AAL5 frame trailer.
0x0C	—	Cell header expansion 1, 2, and 3	Cell header expansion 1, 2, and 3. These fields are added to the BD when expanded cells are enabled by the user (SRSTATE[EC] bit is set in parameter RAM). When expanded cell headers are enabled for AAL5 channels, the 860SAR copies the contents of the cell header expansion fields from the first BD of current message and appends them to every cell of the message sent. When expanded cell headers are enabled for AAL0 channels, these fields are copied into the expanded cell header of the cell the BD points to. The contents of the cell header expansion 1 field is the first word to be transmitted, and the cell header expansion 3 field is the last. The bytes are ordered according to the DMA byte ordering (programmed through the STFCR field in the parameter RAM). If the ECSIZE field in the parameter RAM is set to a value less than 3, the cell header expansion fields are populated with the number of words specified in ECSIZE.

2.2 Receive and Transmit Connection Tables

The connection tables hold channel configuration and temporary parameters for each receive and transmit channel. The internal connection tables hold parameters for up to 32 receive and 32 transmit channels (channels 0–31). In extended channel mode, parameters for channels 32 and above are kept in external memory starting at the memory location specified by ECTBASE in the parameter RAM. There is no actual relationship between transmit and receive channels although they are combined in pairs in the connection tables. An example of a 6-entry connection table located in the dual-port RAM is shown in Figure 2-5.

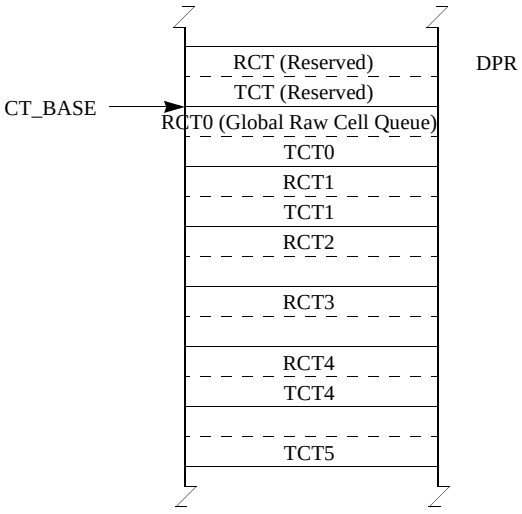


Figure 2-5. Example of a Six-Entry Connection Table in Dual-port RAM

Each entry in the connection table contains 64 bytes. The first half of the 64-byte memory space is used for the receive connection table (RCT) and the second half is used for the transmit connection table (TCT). The RCT and TCT reside in a fixed place in each entry in the connection table. The RCT address always starts at xx000000 to xx010011 and TCT starts at xx100000 to xx111111. Note that RCT entry 0 is reserved for the global raw cell queue, but that TCT entry 0 is available to the user with no restrictions. Channel 65535 is reserved as the null channel for use by the APC scheduler. If extended channel mode is used, then one additional reserved RCT and TCT entry for CP internal purposes is assigned in the memory space above the CT_BASE pointer.

2.2.1 Receive Connection Table (RCT)

The 860SAR performs reassembly for all the received channels in parallel and on a cell by cell basis. The RCT is used to hold the channel's configuration and temporary parameters. Each entry in the RCT holds parameters (the pointers, flags, and temporary data fields that are described below) for a single ATM channel. Figure 2-6 shows the memory organization of a receive connection table.

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CT_Offset + 0	FHNT	—	—	—	—	—	—	—	HEC	CLP	CNG	INF	CNGI	CDIS	AAL	
CT_Offset + 2	RBALEN															
CT_Offset + 4 CT_Offset + 6	RCRC															
CT_Offset + 8 CT_Offset + A	RB_PTR															
CT_Offset + C	RTMLEN															
CT_Offset + E	RBD_PTR															
CT_Offset + 10	RBASE															
CT_Offset + 12	TSTAMP															
CT_Offset + 14	IMASK															
CT_Offset + 16 to CT_Offset + 1F	RESERVED															

Note: Entries in boldface must be initialized by the user.

Figure 2-6. Receive Connection Table (RCT)

Table 2-3 describes the fields for a single entry in an RCT.

Table 2-3. RCT Field Descriptions

Offset	Bits	Name	Description
0x00	0	FHNT	Frame hunt mode. Indicates that this channel had a busy exception or a restart, and it is currently in a frame hunt mode. While in frame hunt mode the CP discards all received cells until a new message frame is started (indicated by the CPI bit of the last cell header). This bit is cleared by the user during initialization, and is cleared or set by the CP thereafter.
	1–7	—	Reserved.
	8	HEC	Header error control indication. Indicates that a HEC error was detected in at least one cell of the current frame. This bit is valid only when receiving AAL5 and AAL0 cells in serial mode. When receiving AAL5 channel cells this bit is set as soon as the first cell of the current frame is determined to have a HEC error. At the end of the frame the header error control indicator bit is copied to the last BD of the frame. When receiving AAL0 channel cells the header error control indicator bit is written directly to the BD HEC error indication bit.
	9	CLP	Cell loss priority indication. Indicates that cell loss priority was reported on at least one cell of the current frame. The CLP bit is set by the CP as soon as the first cell of a AAL5 message arrives with the CLP bit set. At the end of the frame the CLP bit is copied to the last BD of the frame. For AAL0 channels, this bit is a copy of the CLP bit of the cell last received or currently being received. For AAL0 channels, the CLP indicator along with the reset of header information can be found in the RX buffer.
	10	CNG	Congestion. Indicates that congestion was reported on the last cell of the current frame. The CNG bit is set by the CP only if the last cell of the current AAL5 frame has arrived with the PTI[EFCI] bit set. At the end of the frame the CNG bit is copied to the last BD of the frame. For AAL0 channels, this bit is a copy of the PTI[EFCI] bit of the cell last received or currently being received. For AAL0 channels, the CNG indicator along with the rest of the header information can be found in the RX buffer.
	11	INF	In frame. Indicates that the receiver is in the middle of a frame and the receive buffer is already open. If this bit is cleared there is no open buffer for this connection. The receiver sets the INF bit when a new frame starts and clears the INF bit when the frame ends. This bit should be cleared to zero during initialization.
	12	CNGI	Congestion interrupt mode. This bit is valid only for AAL5 channels; for AAL0 channels, it is reserved. This bit enables the generation of an interrupt by the SAR layer to indicate the detection of a PTI[EFCI] bit in a received cell. 0 No congestion interrupts. Congestion is indicated in the last BD of the frame. Refer to the CNG bit field description. 1 Congestion indication is checked for each cell and an interrupt is written to the exception table if the PTI[EFCI] is set in the received cell. A GINT interrupt is generated if INT_CNT counter has reached the user-determined threshold count.
	13	CDIS	Channel disable. This bit is set or cleared by the CP in response to the Stop Receive or Start Receive commands issued to the CP for this channel. 0 The channel is enabled to receive AAL5 cells. 1 This channel is disabled, and cells addressed to this channel are discarded. This bit should be cleared during initialization by the user; during normal operation the user should not directly manipulate this bit.

Table 2-3. RCT Field Descriptions (Continued)

Offset	Bits	Name	Description
0x00	14–15	AAL	AAL type. Determines if received cells are buffered as AAL0 or AAL5 cells. 00 This is a raw-cell channel (AAL0). When receiving a cell from the channel the receiver stores the cell using the AAL0 buffer format. 01 The channel supports ATM Adaptation Layer 5 (AAL5). The receiver performs AAL5 cell reassembly and copies the 48 bytes of payload to the receive buffer. The AAL5 CPCS-PDU trailer is checked when the last cell of the PDU is received. 1x Reserved
0x02	—	RBALEN	Receive buffer available length. This field contains the number of bytes available in the receive buffer. It is loaded with the value programmed into the SMRBLR field in the parameter RAM when a new buffer is opened and is decremented by 48 for every cell received by the channel. This field is applicable only to AAL5 channels.
0x04	—	RCRC	Receive CRC. This field contains the CRC32 value calculated during a cell receive operation. This field is only applicable to AAL5 channels.
0x08	—	RB_PTR	Receive buffer pointer. This field is valid only when INF is set. The RB_PTR field holds the physical address of the current position in the receive buffer to which data is being written.
0x0C	—	RTMLEN	Frame buffer count. This field contains the total number of bytes received during the current AAL5 frame. The value in RTMLEN is cleared at the beginning of a frame and incremented by the value in the SMRBLR field in the parameter RAM as each additional buffer is received. The receiver uses the RTMLEN field to calculate the total message length which is compared to the length field of the CPCS-PDU. This field is applicable to AAL5 channels only.
0x0E	—	RBD_PTR	Receive BD pointer. This field points to the current BD in the BD list. The actual address of the current BD is (RBD_PTR x 4) + RBDBASE (where RBDBASE is the base pointer to the receive BD memory space). This field should be initialized to the RBASE value by the user.
0x10	—	RBASE	Receive BD base. This field holds a pointer to the first BD in the BD list of the current channel. The actual address of the first BD in the list is (RBASE x 4) plus the offset value in the RBDBASE field in the parameter RAM. Note that RBASE is a word-aligned offset pointer from RBDBASE. This field provides bits [14–29] of the offset, and bits [30–31] are always 00.
0x12	—	TSTAMP	Time stamp. This field contains the arrival time stamp of the current frame. The CP copies the value from the CP timer specified by the TSTA field in the parameter RAM to the TSTAMP field on the arrival of the first cell of the current frame. The TSTAMP value can be used to determine if a receive time-out condition exists.
0x14	—	IMASK	Interrupt mask. This field contains an interrupt mask for both the receiver and transmitter of an ATM channel. The interrupt mask allows the user to enable or disable interrupt generation for any of the interrupts in the exception queue. If a bit in the IMASK field is cleared, exception queue entries are not generated for these events and the GINT interrupt counter is not advanced. Note that interrupt masking is performed in microcode, and an interval equal to approximately 40 system clocks must elapse for a change in the IMASK field to become effective. The bit positions in the IMASK field are identical to those of the exception queue entry with the exception of the APCO bit position, which is reserved in the IMASK field.

2.2.2 Transmit Connection Table (TCT)

The 860SAR performs segmentation for all the transmitted channels in parallel and on a cell-by-cell basis. The TCT is used to hold the channel's configuration and temporary parameters. Each entry in the TCT holds parameters (pointers, flags, and temporary data) for a single ATM channel. Figure 2-7 shows the memory organization of a transmit connection table.

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CT_Offset + 20	—	—	—	—	—	—	—	—	PC	—	—	INF	CR10	CDIS	AAL	
CT_Offset + 22	TBALEN															
CT_Offset + 24	TCRC															
CT_Offset + 28	TB_PTR															
CT_Offset + 2C	TTMLEN															
CT_Offset + 2E	TBD_PTR															
CT_Offset + 30	TBASE															
CT_Offset + 32	RESERVED															
CT_Offset + 34	CHEAD															
CT_Offset + 38	APCL															
CT_Offset + 3A	APCPR															
CT_Offset + 3C	OUT	APCP														
CT_Offset + 3E	APCPF															

Note: Entries in boldface must be initialized by the user.

Figure 2-7. Transmit Connection Table (TCT)

Table 2-4 describes the bit fields for a single entry in a TCT.

Table 2-4.TCT Field Descriptions

Offset	Bits	Name	Description
0x20	0–7	—	Reserved
0x20	8	PC	Padded cell. Indicates that the transmitter must add an additional padded cell to the end of an AAL5 frame. The user must clear this bit during initialization.
0x20	9–10	—	Reserved
0x20	11	INF	In frame. Indicates whether a frame is being transmitted. The transmitter sets this bit when a new frame starts and clears the bit when the frame ends. If this bit is cleared there is no open transmit buffer for the connection. If this is set the transmitter is sending a frame and the transmit buffer is open. The user must clear this bit during initialization.
0x20	12	CR10	Perform CRC10. This bit is applicable only to AAL0 channels. The CR10 bit instructs the transmitter to perform CRC10 calculation on the cell payload and place the result at the end of the cell payload in the CRC10 field. This option supports OAM CRC10 according to ITU specification I.610. 0 Do not perform CRC10 on the transmitted cell. 1 Perform CRC10 and insert the CRC result into the CRC field of the cell (the last 10 bits of OAM cell payload.)

Table 2-4.TCT Field Descriptions (Continued)

Offset	Bits	Name	Description
0x20	13	CDIS	Channel disable. Set by the STOP TRANSMIT (ABORT) command to stop transmission from the channel. When the STOP TRANSMIT (ABORT) command is issued during an AAL5 transmission the 860SAR transmits an abort cell (a “last cell” with length of zero), and stops transmission by the channel. When the STOP TRANSMIT (ABORT) command is issued during AAL0 transmissions the channel stops transmitting after the current cell. During both AAL5 and AAL0 transmit operations, the CDIS bit disables transmissions on cell boundaries only. The CDIS bit is cleared by the RESTART TRANSMIT command. After the RESTART TRANSMIT command is issued the transmitter will continue transmitting cells from this channel as scheduled by the APC. The user must not write this bit directly; the STOP TRANSMIT (ABORT) and RESTART TRANSMIT commands control the CDIS bit instead. 0 This channel is transmit enabled. 1 This channel is transmit disabled. This bit should be cleared to zero during initialization.
0x20	14–15	AAL	AAL type. These bits determine if the cells are transmitted as AAL0 or AAL5 cells. 00 This is a raw-cell channel (AAL0). When transmitting a cell from the channel the transmitter transmits the cell using the AAL0 buffer format. 01 The channel supports ATM Adaptation Layer 5 (AAL5). The transmitter performs AAL5 cell segmentation and transmits the 48 bytes of payload from the transmit buffer. The AAL5 CPCS-PDU trailer is generated when the last cell of the PDU is transmitted. 1x Reserved
0x22	—	TBALEN	Transmit buffer available length. Contains the number of bytes in a transmit BD. This field is applicable only to AAL5 channels. The value in TBALEN is copied from the data length field of the transmit BD when a new buffer opens and is decremented by 48 for every cell transmitted from the channel.
0x22	—	TCRC	CRC32 temporary result. The temporary result of the CRC32 calculation. This field is applicable to AAL5 channels only.
0x28	—	TB_PTR	Transmit buffer pointer. This field contains the real address of the current position in the transmit buffer.
0x2C	—	TTMLEN	Transmit total message length. This field counts bytes transmitted in the current AAL5 frame. The TTMLEN field is loaded with the data length copied from the transmit BD. As each additional BD is opened, the 860SAR adds the BD data length value to the TTMLEN field. At the end of the frame the value in the TTMLEN field is copied into the AAL5 length field. This field is applicable only to AAL5 channels.
0x2E	—	TBD_PTR	Transmit BD pointer. Points to the current BD in the BD list. The address of the current BD in the list is (TBD_PTR x 4) + TBDBASE (where TBDBASE is the base pointer to the transmit BD memory space). This field should be initialized to the TBASE value by the user. Note that TBD_PTR is a word-aligned offset pointer from TBDBASE. This field provides bits [14–29] of the offset; bits [30–31] are always 00.
0x30	—	TBASE	Transmit BD base. Holds a pointer to the first BD in the BD list of the current channel. The actual address of the first BD in the list is (TBASE x 4) plus the offset value in the TBDBASE field in the parameter RAM. Note that TBASE is a word-aligned offset pointer from TBDBASE. This field provides bits [14–29] of the offset; bits [30–31] are always 00.
0x32	—	—	Reserved

Table 2-4.TCT Field Descriptions (Continued)

Offset	Bits	Name	Description
0x34	—	CHEAD	Channel header. Valid only for AAL5 channels. This field contains the full (4 byte) header of the cells of the AAL5 channel. The transmitter appends the CHEAD field and the HEC field to the cell payload during transmission to create a complete cell. This field must be initialized by the user. The byte ordering of this field is little endian.
0x38	—	APCL	APC link. This field is used by the CP to link additional channels to the same APC time slot that the current channel occupies. Initialize this field with 0xFFFF to indicate an idle channel.
0x3A	—	APCPR	APC pace remainder. This field contains the rate remainder generated by the APC after adding the pace FRACTION to the additive APCPR. The user should initialize this field with 0x0000.
0x3C	0	*OUT*	APC out. The user must initialize this bit to zero. When the Transmit Deactivate Channel command is issued, this bit is set. When the APC scan reaches this channel in the APC table, if this bit is set, the channel will be removed from the APC table, and this bit will be cleared. Thus, this bit can be used as an indication of when the Transmit Deactivate Channel command has completed. NOTE: This function is available only in the 860SAR rev C and later. For earlier revisions, this bit should be written to zero whenever the APC pace is written.
0x3C	1-15	APCP	APC pace. This field contains the APC pacing value for this channel. When the channel is placed in the transmit queue, the APC reschedules the channel in a new position/time slot in the APC table. The address of the new slot is the current slot address + APCP (modulo the table length). Note that the APCP value selected is bounded as shown below: $$1 \le \left(APCP + \frac{APCPF}{65536} \right) \le [APCTablelength - 1]$$ For more information about the APC refer to Chapter 5, “ATM Pace Control.” Note that bit 0 of the APCP field is reserved, and it should be cleared to zero during initialization.
0x3E	—	APCPF	APC pace fraction. This field contains the APCP- FRACTION for the current channel in units of 1/65536 slot times. For example, if a pace of 1.5 is desired, the APCP field should be 0x0001 and the APCPF field should be 0x8000, thereby setting the pace to 1+32768/ 65536, or a value of 1.5.

Chapter 3
Parameter RAM Configuration

The 860SAR's parameter RAM is used to configure the four SCCs and the UTOPIA interface. The CP also uses the parameter RAM to store operational and temporary values used during SAR activities.

3.1 Parameter RAM Map

When performing SAR operations the 860SAR overlays the parameter RAM with the configuration structures shown in Table 3-1 and Table 3-2. The values written in the parameter RAM by the user or the CP determine the capabilities of the four SCCs and the UTOPIA interface.Table 3-1 describes the parameters for serial mode and UTOPIA interface ATM operations. Note that some of the values must be initialized by the user; values set by the CP should not be modified by the user.

Table 3-1. Serial and UTOPIA Interface Parameter RAM Configuration

Offset from SCC Base	Name	Width	Description
0x00	RBDBASE	Word	Base pointer for the receive BDs. Defines the starting location in the host memory of a memory space of up to 256 Kbytes in which receive BDs for all connections are located. The receive BD pointer for a specific connection is located in the RCT. RBDBASE is a host-initialized parameter. Must be word aligned
0x04	SRFCR	Byte	Receive function code and receive status. The SRFCR and SRSTATE parameters contain host-initialized global parameters for DMA transfers and related status. Refer to Section 3.1.1, "Receive Function Code and Status Register."
	SRSTATE	Byte	
0x06	MRBLR	Hword	Maximum receive buffer length register. The value in MRBLR must be user-initialized to zero; if programmed with a non-zero value the SCC operates in transparent mode as described in the *MPC860 PowerQUICC User's Manual.*
0x08	RSTATE	Word	SCC internal receive state parameters. Stores internal state variables and flags during receive operation. The user must initialize the first byte of RSTATE with the value in SRFCR. All other bytes must be initialized with 0. The user must not write to RSTATE during receive operations.
0x0C	—	Word	Reserved
0x10	R_CNT	Hword	Receive internal byte counter. Counter field for the bytes received during ATM cell reception. The user must not write to this location.

Table 3-1. Serial and UTOPIA Interface Parameter RAM Configuration (Continued)

Offset from SCC Base	Name	Width	Description
0x12	STFCR	Byte	Transmit function code and transmit status. STFCR contains host-initialized global parameters for DMA transfers. STSTATE contains global status parameters. Refer to Section 3.1.2, “Transmit Function Code and Status Register.
	STSTATE	Byte	
0x14	TBDBASE	Word	Base pointer for the transmit BDs. Defines the host-initialized starting location in memory for a memory space of up to 256 Kbytes where the transmit BDs for all the connections are located. The transmit BD pointer for a specific connection is located in the TCT. Must be word aligned.
0x18	TSTATE	Word	SCC internal transmit state parameters. Used to store internal state variables and flags during transmit operation. The user should initialize the first byte of TSTATE with the value in STFCR. All other bytes should be initialized with 0. The user must not write to TSTATE during transmit operations.
0x1C	COMM_CH	Hword	Command channel. Contains the channel number associated with current channel command. The host must write the required channel number to COMM_CH before a channel associated command is issued.
0x1E	STCHNUM	Hword	Current transmit channel number. During transmission and reception the CP uses SRCHNUM, STCHNUM, OLDLEN, RTEMP, TTEMP, RSTUFF, RHECTEMP, THECTEMP, RSCRAM, RSCRAM1, TSCRAM, TSCRAM1, RCHAN, TCHAN, RCRC and TCRC to store temporary data for internal use; do not write to these locations.
0x20	T_CNT	Hword	Transmit internal byte counter. Counter field for the bytes sent during ATM cell transmission. The user must not write to this location.
0x22	CTBASE	Hword	Connection table base address. Contains the word-aligned base address in the dual-port RAM of the connection table for channels 0–31. CTBASE is an offset from the beginning of the dual-port RAM. The host-initialized connection table contains control information for all connections. Each connection has an entry in the RCT and TCT.
0x24	ECTBASE	Word	External connection table base address. Contains the word-aligned base address for the external connection table, and is valid only when operating in extended mode. The external connection table contains connection information and is host-initialized.
0x28	INTBASE	Word	Interrupt base pointer. Host-initialized 32-bit pointer containing the word-aligned starting address of the interrupt circular table in external memory. Each table entry has information about an interrupt request that has been generated by the 860SAR to the host.
0x2C	INTPTR	Word	Pointer to interrupt queue. Host-initialized global parameter that contains the address of next 860SAR interrupt entry in the circular interrupt queue. The CP writes interrupt information to the entry specified by INTPTR when an interrupt occurs. The host must copy the value in INTBASE to INTPTR before enabling interrupts.
0x30	C-MASK	Word	Constant mask for CRC32. Host-initialized to 0xDEBB20E3. C-MASK is used by the receiver to check CRC32 results when supporting AAL5 connections.
0x34	SRCHNUM	Hword	Current receive channel number. During transmission and reception the CP uses SRCHNUM, STCHNUM, OLDLEN, RTEMP, TTEMP, RSTUFF, RHECTEMP, THECTEMP, RSCRAM, RSCRAM1, TSCRAM, TSCRAM1, RCHAN, TCHAN, RCRC and TCRC to store temporary data for internal use; do not write to these locations.

Table 3-1. Serial and UTOPIA Interface Parameter RAM Configuration (Continued)

Offset from SCC Base	Name	Width	Description
0x36	INT_CNT	Hword	Interrupt counter. Used as a countdown counter that is decremented for each interrupt entry reported in the interrupt circular table. On terminal count an interrupt is signaled to the host by setting the GINT bit in the event register. Refer to Chapter 6, “Exceptions,” for additional information about exception handling. The counter is reinitialized with the INT_ICNT value after an exception. The user must initialize the INT_CNT field with the value in the INT_ICNT field before enabling SAR operation.
0x38	INT_ICNT	Hword	Interrupt initiate value. INT_ICNT is user-defined and is loaded into the INT_CNT field after an exception caused by the counter reaching terminal count.
0x3A	TSTA	Hword	Time stamp timer address. Contains the address of the RISC timer to be used for the time-out process. TSTA is used for AAL5 connections only. The receiver copies the RISC timer value from the address specified by the TSTA field to the RCT when a new frame is received. The TSTA field must be initialized with a value equal to (TM_BASE+4*timer number).
0x3C	OLDLEN	Hword	Transmitter temporary length. Do not write to this location.
0x3E	SMRBLR	Hword	SAR maximum receive buffer length register. Determines the number of bytes the 860SAR writes to a receive buffer before moving to the next buffer. The contents of this field are user-defined, and must contain a value that is a multiple of 48 bytes. This parameter is common to all ATM connections.
0x40	EHEAD	Word	Empty cell header and empty cell payload The EHEAD and EPAYLOAD fields contain the data for the empty cell header (EHEAD) and payload (EPAYLOAD). The data for these fields must be written in little-endian byte format. When operating in serial mode the 860SAR sends and receives empty (idle) cells using the data contained in EHEAD and EPAYLOAD. During transmit operations an empty cell is assembled by transmitting EHEAD once, calculating and transmitting a HEC, and transmitting EPAYLOAD twelve times. During receive operations the incoming header is compared with EHEAD to check for empty cells and if an empty header is detected the following empty payload is not used. The user selects the EHEAD and EPAYLOAD values required: The ATM Forum UNI specification states that unassigned cells should be sent when no valid transmit data is available, while the ITU mandates use of idle cells. Unassigned cells are used as empty cells when EHEAD = 0x0000 0000 and idle cells when EHEAD = 0x0100 0000. In both cases, EPAYLOAD should be initialized to 0x6A6A 6A6A.
0x44	EPAYLOAD	Word	
0x48	TQBASE	Hword	Transmit queue base pointer The TQBASE field contains a user-defined pointer to the base address of the transmit queue in the dual-port RAM.

Table 3-1. Serial and UTOPIA Interface Parameter RAM Configuration (Continued)

Offset from SCC Base	Name	Width	Description
0x4A	TQEND	Hword	Transmit queue end pointer The TQEND field contains a user-defined pointer to the last entry in the transmit queue in the dual-port RAM. The size of the transmit queue is user-defined, and the minimum size should be a value equal to (NCITS +2). If a channel is in MPHY UTOPIA mode, the minimum size should be equal to $\sum_{}^{nMPHY} [\langle NCITSx \rangle + 2]$
0x4C	TQAPTR	Hword	Transmit queue APC pointer. The APC writes a pointer value to the TQAPTR field indicating the next channel number to transmit. The APC automatically wraps this pointer back to TQBASE when it reaches the end of the queue (determined by the value in the TQEND field). The user must initialize the TQAPTR to the value in TQBASE.
0x4E	TQTPTR	Hword	Transmit queue transmitter pointer. TQTPTR is a pointer to the next channel to be sent. The transmit queue transmitter pointer always follows the APC pointers. The transmitter automatically wraps back to TQBASE when it reaches the end of the queue (determined by the value in the TQEND field). Initialize TQTPTR to the value in TQBASE.
0x50	APCST	Hword	APC status. The value in the APCST field is user-defined. Refer to Section 3.1.4, “APC Status Register (APCST)” for additional information.
0x52	APCPTR	Hword	APC parameter pointer. Contains the address of the APC parameter table. APCPTR is an offset from the beginning of the dual-port RAM. This field is user-defined; the value selected for the address should be divisible by 32 (an address ending with 0b00000).
0x54	AM1	Hword	Address match parameter 1–5. The 860SAR provides three methods for address matching; a lookup table, address compression, and content-addressable memory (CAM). Refer to Section 3.1.3, “Address Match Parameters (AM1–AM5),” for more information about the configuration of these fields.
0x56	AM2	Hword	
0x58	AM3	Hword	
0x5A	AM4	Hword	
0x5C	AM5	Hword	

Table 3-1. Serial and UTOPIA Interface Parameter RAM Configuration (Continued)

<table>
<tr><th>Offset from SCC Base</th><th>Name</th><th>Width</th><th>Description</th></tr>
<tr><td>0x5E</td><td>ECSIZE</td><td>Hword</td><td>Expanded cell size/unassigned cell data. Specifies the number of words used for expanded cells (0-3). These bits are only valid if SRFCR[EC] or STFCR[EC] is set. The expanded header can be from 0 to 12 octets long as described in the following table:
<table>
<tr><th rowspan="2">ECSIZE</th><th colspan="4">Number of Octets</th></tr>
<tr><th>Expanded Cell Header</th><th>ATM Cell Header</th><th>HEC/UDF</th><th>Payload</th></tr>
<tr><td>ECSIZE=0</td><td>0</td><td>4</td><td>0</td><td>48</td></tr>
<tr><td>ECSIZE=1</td><td>4</td><td>4</td><td>0</td><td>48</td></tr>
<tr><td>ECSIZE=2</td><td>8</td><td>4</td><td>0</td><td>48</td></tr>
<tr><td>ECSIZE=3</td><td>12</td><td>4</td><td>0</td><td>48</td></tr>
</table></td></tr>
<tr><td>0x60</td><td>—</td><td>Word</td><td>Reserved</td></tr>
<tr><td>0x64</td><td>R_PTR</td><td>Word</td><td>Receiver internal data pointer. Points to the next data location in memory during cell reception. When SAR operations have been enabled this location should not be written to by the user.</td></tr>
<tr><td>0x68</td><td>RTEMP</td><td>Word</td><td>Receiver temporary data storage.</td></tr>
<tr><td>0x6C</td><td>T_PTR</td><td>Word</td><td>Transmit internal data pointer. Pointer to the next data location in memory during cell transmission. When SAR operations have been enabled this location should not be written to by the user</td></tr>
<tr><td>0x70</td><td>TTEMP</td><td>Word</td><td>Transmitter temporary data storage.</td></tr>
<tr><td>0x74 to 0x7F</td><td>—</td><td>12 Bytes</td><td>Reserved</td></tr>
</table>

Note: Parameter RAM values shown in boldface type must be initialized by the user before enabling the SAR operations. Values shown shaded and in boldface type are used for serial interface operations, and must also be initialized by the user before enabling SAR operations. Parameter RAM values not specified as user-initialized are configured by the CP, and should not be modified by the user.

Table 3-2 describes the parameter RAM values that configure the SCCs for serial interface

SAR operation.

Table 3-2. Serial Interface Parameter RAM Configuration

Offset from SCC Base	Name	Width	Description
0xC0	ALPHA	Hword	Receiver delineation alpha/delta counters. The 860SAR applies the HEC delineation mechanism described in ITU specification I.432 with an alpha value of 7 and a delta value of 6 to locate and maintain cell synchronization; ALPHA and DELTA must be user initialized to 0x7 and 0x6 respectively. The receiver updates the ALPHA and DELTA parameter locations; the user must not write to these locations during receive operations.
0xC2	DELTA	Hword	
0xC4	RSTUFF	Word	Receive data stuffing location (53 to 52 byte conversion).
0xC8	SHUFFLESTATE	Hword	Receiver data shuffling state. Initialize to 0x0000.
0xCA	RHECTEMP	Hword	Receiver temporary HEC storage area
0xCC	THECTEMP	Hword	Transmitter temporary HEC storage area
0xCE	ASTATUS	Hword	Cell synchronization status register. Initialize to 0x0000.
0xD0	HEC_ERR	Hword	HEC error counter. Contains a 16-bit count of incoming cells with HEC errors. The HEC_ERR field may be read by the user at any time.
0xD2	—	Hword	Reserved
0xD4	RSCRAM	Word	Receiver scrambling storage. Initialize to 0x0000_0000.
0xD8	RSCRAM1	Word	
0xDC	TSCRAM	Word	Transmitter scrambling storage. Initialize to 0x0000_0000.
0xE0	TSCRAM1	Word	
0xE4	RCRC	Word	Receiver temporary CRC
0xE8	TCRC	Word	Transmitter temporary CRC
0xEC	RCHAN	Word	Receiver current channel
0xF0	TCHAN	Word	Transmitter current channel
0xF4 to 0xFF	—	12 Bytes	Reserved

Note: Parameter RAM values in boldface type are used for serial interface operations and are initialized by the user before SAR operations. Parameter RAM values not specified as user-initialized are configured by the CP and should not be modified by the user.

3.1.1 Receive Function Code and Status Register

The receive function code and status register, shown in Figure 3-1, contains the user-initialized function codes and related global status parameters.

BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Figure 3-1. Receive Function Code and Status Register

FIELD	—			BO		FC			EXT	ACP	EC*	SNC *	—	DIS*	SER	MPY *
RESET	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

* Available only in SCC4 UTOPIA mode; otherwise written as 0

Figure 3-1. Receive Function Code and Status Register

The receive function code and status register fields are described in Table 3-3.

Table 3-3. Receive Function Code and Status Register Field Descriptions

Bits	Name	Description
0–2	—	Reserved
3–4	BO	Byte ordering convention to be used in the SDMA transfers 00 Little-endian byte ordering 01 PowerPC little-endian byte ordering 1X Big-endian byte ordering
5–7	FC	Contains a user-defined value driven on the address type signals AT[1–3) when the SDMA channel accesses memory.
8	EXT	Extended mode. 0 Maximum of 32 channels, with channel mapping and connection tables supported internally. Internal channel mapping mechanism is used. 1 Maximum of 65536 channels, with channel mapping and connection tables supported externally. CAM or address compression is used for channel mapping.
9	ACP	Address compression. Valid only if EXT = 1. 0 CAM is used for channel mapping. 1 Address compression mechanism is used for channel mapping.
10	EC	Expanded cell 0 Standard 53-byte ATM cell is used. 1 Expanded cell method is used on all UTOPIA cells. Cell length can be 52, 56, 60, or 64 bytes long, as defined by the ECSIZE field. This option is valid only for UTOPIA mode operations.
11	SNC	Synchronization. Valid only in UTOPIA mode (PDPAR[UT] =1); must be set to 1 by user during initialization. 0 SOC sync is lost. This is also reported via an interrupt in the UTOPIA mode event register (IDSR1). 1 SOC is in sync.
12	—	Reserved
13	DIS	Disable. Used to disable all receive processes in UTOPIA mode. This function is used only when initializing the UTOPIA port. It must not be written to while the UTOPIA port is operating. 0 Receive enabled. 1 Receive disabled.
14	SER	Serial mode select. Selects the mode of the ATM physical interface. 0 UTOPIA mode. 1 Serial mode.
15	MPY	Multiple PHY operation. Valid only when operating in UTOPIA mode. This bit is programmed by the user. 0 Single PHY mode. 1 Multiple PHY mode.

3.1.2 Transmit Function Code and Status Register

The transmit function code and status register, shown in Figure 3-2, contains the user-initialized function codes and related global status parameters.

BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
FIELD	—			BO		FC			EXT	TQF **	EC*	PBF *	—		SER	MPY *
RESET	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

* Available only in SCC4 UTOPIA mode; otherwise written as 0

** Valid only for 850SAR. Will be available in Rev. D of the 860SAR.

Figure 3-2. Transmit Function Code and Status Register

The transmit function code and status register bit fields are described in Table 3-4.

Table 3-4. Transmit Function Code and Status Register Field Descriptions

Bits	Name	Description
0–2	—	Reserved
3–4	BO	Byte ordering convention to be used in the SDMA transfers 00 Little-endian byte ordering 01 PowerPC little-endian byte ordering 1x Big-endian byte ordering
5–7	FC	The FC field contains a user-defined value that is driven on the address type signals AT[1–3) when the SDMA channel accesses memory.
8	EXT	Extended mode. 0 Maximum of 32 channels, with channel mapping and connection tables supported internally. Internal channel mapping mechanism is used. 1 Maximum of 65536 channels, with channel mapping and connection tables supported externally. CAM or address compression is used for channel mapping.
9	TQF	Transmit Queue Full. This bit is set, when the APC bypass command is used, to indicate that the transmit queue is full. It is the user's responsibility to make sure this bit is not set (i.e., this bit is 0) before issuing an APC bypass command. The transmitter will clear this bit as soon as there is space in the transmit queue. This bit should be initialized to zero (0).
10	EC	Expanded cell 0 Standard 53-byte ATM cell is used. 1 Expanded cell method is used on all UTOPIA cells. Cell length can be 52, 56, 60, or 64 bytes, as defined by ECSIZE. Valid only for UTOPIA mode operations.
11	PBF	Port B flag. May be used in multi-PHY mode to coordinate CP and HOST write cycles to their Port B general-purpose signals (if the host is using different port B general-purpose signals). The host uses PBF to notify the CP that PORTB general-purpose signals have been modified. In multi-PHY mode, the CP checks PBF before performing read-modify-write cycles to the Port B multi PHY address signals. If the PBF bit is set, the CP waits for the host to clear the bit. The CP will then start the read-modify-write cycle. The host should set PBF before performing read-modify-write cycles to prevent overwriting the CP configuration of the multi-PHY signals. 0 No-flag. The CP is allowed to perform the read-modify-write cycle. 1 Flag is set. The CP should wait until PBF is clear and then can perform the multi-PHY read-modify-write cycle from port B. The host should set PBF before its port B write cycle and ensure that PBF is cleared for at least 10 system clocks following a host read-modify-write cycle.
12–13	—	Reserved
14	SER	Serial mode select. Selects the mode of the ATM physical interface. 0 UTOPIA mode. 1 Serial mode.
15	MPY	Multiple PHY operation. Valid only when operating in UTOPIA mode. This bit is programmed by the user. 0 Single PHY mode. 1 Multiple PHY mode.

3.1.3 Address Match Parameters (AM1–AM5)

The 860SAR uses one of the three following methods for address matching.

- A lookup table—Refer to Table 3-5 for AM1–AM5 configuration for operation with an address look-up table.

- Address compression—Refer to Table 3-7 for AM1–AM5 configuration for operation with address compression.
- Content-addressable memory (CAM)—Refer to Table 3-9 for AM1–AM5 configuration for CAM operation.

AM1–AM5 parameter configuration for address look-up table operation is shown in Table 3-5.

Table 3-5. AM1–AM5 Parameter Configuration with Look-up Table

Field	Name	Function
AM1 AM2	HMASK	Header mask. The 860SAR masks the header of each incoming cell with HMASK and uses the masked cell header in the address match process. The masking process uses a bitwise AND function so bits are masked out by clearing the relevant bits in HMASK. The bit locations of HMASK are shown in Figure 3-3.
AM3	AMBASE	Address match table base. Used as a pointer to the address lookup table when operating in internal mode. The table has up to 32 entries. It is scanned from the end (AMEND) to the base, so headers for the busiest connections should be at the top of the table. When a match occurs, the CP uses the location of the match to locate the channel number in the pointer table. The user should initialize AMBASE to point to the last entry of the address match table. AMBASE must be word-aligned.
AM4	AMEND	Address match end address. Contains the address of the top entry in the table. New connections are added to table at the address specified by AMEND. The match process also starts at this address. The value in the AMEND field is maintained by the user.
AM5	APBASE	Address pointing table. Pointer to a table of address pointers to the connection tables when operating in internal mode. The address pointers are also used as channel numbers when operating in internal mode. The user must initialize APBASE to point to the last pointer of this table, which contains the offset of the connection table entry of the global raw cell queue (channel 0). APBASE must be halfword-aligned.

The bit locations in the HMASK field are shown in Figure 3-3.

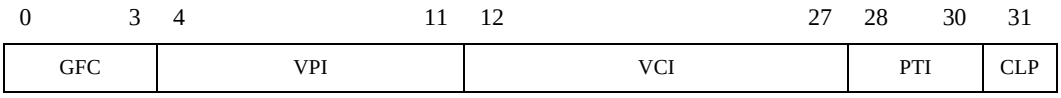


Figure 3-3. HMASK

The HMASK bit fields are described in Table 3-6.

Table 3-6. HMASK Field Descriptions

Bit(s)	Name	Description
0–3	GFC	Generic flow control. Can be cleared to 0b0000 to indicate that GFC protocol is not enforced.
4–11	VPI	Virtual path identifier
12–27	VCI	Virtual channel identifier
28–30	PTI	Payload type identifier
31	CLP	Cell loss priority

AM1–AM5 parameter configuration for extended channel mode with address compression (EXT = 1 and ACP = 1) is shown in Table 3-7.

Table 3-7. AM1–AM5 Parameter Configuration in Extended Channel Mode

Field	Name	Function
AM1	FLBASE	First-level table base. Contains the word-aligned starting address for the first-level table of the address compression algorithm.
AM2		
AM3	SLBASE	Second-level table base. Pointer to the beginning of a 64-Kbyte memory space where the set of second-level addressing tables are located.
AM4		
AM5	FLMASK	First-level mask. The 860SAR masks the GFC, VPI, and PTI bits of the header of each incoming cell with bits 1–15 of FLMASK and uses the masked cell header in the address match process. The FLMASK should contain an unbroken sequence of set bits; for example, the sequence 0b000001111111110 would be a correct sequence, while the sequence 0b000111110011100 contains a broken sequence of set bits, and would lead to undefined behavior during the address match process. The masking process uses a bitwise AND function to allow bits to be masked out by clearing the relevant bits in FLMASK. The bit locations of FLMASK are shown in Figure 3-4.

The bit locations in the FLMASK field are shown in Figure 3-4.

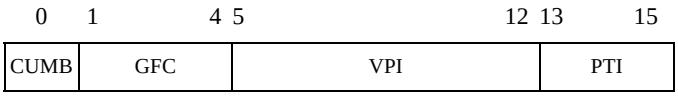


Figure 3-4. FLMASK

The FLMASK bit fields are described in Table 3-8.

Table 3-8. FLMASK Field Descriptions

Bit(s)	Name	Description
0	CUMB	Check unmasked bit. Signals the transmitter to compare the rest of the bits (unmasked bits) to 0. CUMB allows the user to screen out misinserted cells by checking if unused bits in the address matching procedure are non-zero. Reliable one-to-one mapping of VCs to channel numbers requires that bits that are masked off have a fixed value (chosen to be zero). Cells that do not conform to this can be screened out by setting CUMB, and the cells will be passed to the global raw cell queue. 0 Do not check unmasked bits. 1 Check that all unmasked bits equal 0.
1–4	GFC	Generic flow control. Can be cleared to 0b0000 to indicate that GFC protocol is not enforced.
5–12	VPI	Virtual path identifier
13–15	PTI	Payload type identifier

AM1–AM5 parameter configuration for extended channel mode CAM operation (EXT = 1 and ACP = 0) is shown in Table 3-9.

Table 3-9. AM1–AM5 Parameter Usage—Extended Channel Mode

Field	Name	Function
AM1	HMASK	Header mask. The 860SAR masks the header of each incoming cell with HMASK and uses the masked cell header in the address match process. The masking process uses a bitwise AND function so bits can be masked out by clearing the relevant bits in HMASK. The bit locations of HMASK are shown in Figure 3-3.
AM2		
AM3	CAMADD	CAM address. DMA pointer to the CAM's address in the 860SAR's address map. When using the CAM address matching method, DMA uses the CAM address for read and write cycles. The value in the CAMADD field should be divisible by 16
AM4		
AM5	CAMLEN	CAM length. Contains the number of entries in the CAM.

3.1.4 APC Status Register (APCST)

The bit fields in the APC status register are shown in Figure 3-5.

BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
FIELD	—	CSER		NSER		NMPHY			CMPHY			—	—	DIS	PL2	MPY
RESET	0	UD		UD		UD			UD			0	0	0	UD	UD
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR																

Figure 3-5. APC Status Register (APCST)

APC status register bit fields are described in Table 3-10.

Table 3-10. APC Status Register Field Descriptions

Bit(s)	Name	Description
0	—	Reserved
1–2	CSER	Current serial or UTOPIA channel. The CSER field is used by the APC to point to the currently active serial or UTOPIA interface if multiple physical ATM interfaces are active on the 860SAR. The CSER field must be initialized with the same value programmed in the NSER field.
3–4	NSER	Next serial or UTOPIA channel. The NSER field points to the next serial or UTOPIA ATM interface to be serviced after the APC completes operations for the current serial or UTOPIA ATM interface. The NSER field should point only to interfaces operating in ATM mode, thereby providing service for each APC table in the order set by the user. For additional details refer to Chapter 5, “ATM Pace Control.” 00 Serial1 01 Serial2 10 Serial3 11 Serial4 or UTOPIA interface Note that if only one ATM channel is used (through either Serial 4 or UTOPIA), the NSER bits must be set to 11.
5–7	NMPHY	Number of Multiple PHY. Valid only in page 4 of the parameter RAM when page 4 is set to UTOPIA mode; in all other parameter RAM pages this field should be cleared to 000. The NMPHY field specifies the total number of PHY devices which are connected to the UTOPIA interface of the 860SAR. The NMPHY field is valid only when MPY is set. 000 1 PHY 001 2 PHYs 010 3 PHYs 011 4 PHYs 1xx Reserved
8–10	CMPHY	Current Multi-PHY. Valid only in page 4 of the parameter RAM when page 4 is set to UTOPIA mode. The CMPHY field is only used by the CP and should be initialized with the same value that was programmed in NMPHY field.
11–12	—	Reserved
13	DIS	APC disable. This bit is set by the transmitter in serial mode when a global FIFO underrun (GUN) exception occurs. The user should initialize this bit to zero.
14	PL2	Priority table Level 2. Enables the second level APC table mechanism.
15	MPY	Multi-PHY. Valid only in page 4 of the parameter RAM, and enables multi-PHY APC mode. This mode is only valid when the 860SAR is operating in UTOPIA mode. For additional information about multi-PHY configuration refer to Chapter 4, “ATM Controller.”

3.1.5 Serial Cell Synchronization Status Register (ASTATUS)

The serial cell synchronization status register provides additional status information concerning FIFO errors and receiver synchronization status. The ASTATUS register fields are shown in Figure 3-6.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
—	—	—	—	—	—	ORUN	URUN	—	—	—	—	—	—	—	LOCK

Figure 3-6. Serial Cell Synchronization Status Register (ASTATUS)

The ASTATUS[6–7] bits are set by 860SAR and cleared by the user. The ASTATUS[15] bit is set and cleared by 860SAR. The user must clear all bits in ASTATUS during initialization. During SAR operation the user can read and clear the ASTATUS[6–7] bits but must only read the ASTATUS[15] bit. Table 3-11 shows the configuration of the ASTATUS register bits.

Table 3-11. ASTATUS Register Field Descriptions

Bits	Name	Description
0–5	—	Reserved
6	ORUN	Receiver FIFO overrun. Indicates whether a receiver overrun event has occurred. 0 No receiver FIFO overrun. 1 Receiver FIFO overrun. Note that receiver overrun events also set the SCCE[GOV] bit.
7	URUN	Transmitter FIFO underrun. Indicates whether a transmitter underrun event has occurred. 0 No transmitter FIFO underrun. 1 Transmitter FIFO underrun. Note that transmitter underrun events also set the SCCE[GUN] bit.
8–14	—	Reserved
15	LOCK	860SAR cell delineation status. Indicates the current delineation status: 0 The 860SAR receiver is out of synchronization and is not receiving cells. 1 The 860SAR receiver has gained cell delineation and is receiving cells. Note that receiver cell delineation status is also indicated by SCCE[SYNC].

Chapter 4
ATM Controller

This chapter describes the address map configuration of the 860SAR's ATM controller to support connection tables for both single- and multi-PHY interfaces, and the commands provided by the 860SAR for the control of ATM transmit and receive operations on a channel-by-channel basis.

4.1 Address Mapping

The 860SAR implements three different methods for address mapping. The first is based on a look-up table and is used in unextended channel mode where the number of connections is limited to 32 or fewer. When more than 32 connections are desired, two methods for address mapping are supported in extended channel mode: address compression and the use of content addressable memory (CAM).

Only one address mapping method can be used at a time, and it should be selected during system start-up. The mapping method is selected through the SRFCR bits of the parameter RAM. These address mapping mechanisms direct the incoming cell header to a specific internal channel entry in the connection table.

Connection table entries will reside in either DPR or external memory depending on the channel number (i.e., the CT entry number) returned by the address mapping mechanism:

- Ch 0 - 31: connection table resides in DPR.
- Ch 32 and above: connection table resides in external memory.

Note: Channel 0 of the receive side is reserved for the global raw cell queue and channel 65535 is reserved for the null channel used by the APC scheduler.

4.1.1 VCI/VPI Look-up Table

The VCI/VPI look-up table is used to perform address mapping for incoming cells in unextended channel mode (SRFCR[EXT] = 0).

There are two tables used for this mapping mechanism. The first table is the matching table, which contains up to 32 entries of 32 bits each. Each entry contains a match address (VCI/VPI). The second table is the pointing table of 32 entries, each containing a 16-bit pointer. Each pointer points to the connection table entry (the first address location of a specific

RCT) which matches the VCI/VPI located in the same position in the address matching table.

Upon a reception of a cell header, the received cell header is masked by performing bitwise AND logic with HMASK. The masked header is then compared with each entry in the matching table. If there is a match, the pointer in the pointing table is read to get the channel number associated with this incoming cell. The channel number used in this method is the actual address of the RCT. If there is no match, the global raw cell queue address is used. Note that the user should always reserve an entry in the address matching table at AMBASE containing a pointer to the raw cell RCT in the pointing table.

Note that the address mapping mechanism searches the address mapping table sequentially from the end (AMEND) to the base (AMBASE). Therefore, it is recommended to put the most frequently used connections at the top of the table (near AMEND). Note that AMEND points to the lowest address and that new channels are added above this pointer.

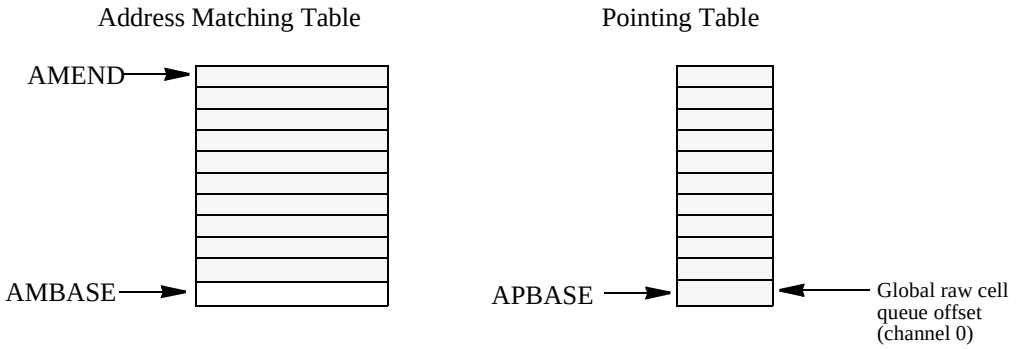


Figure 4-1. Address Mapping Tables

4.1.1.1 Adding a New Channel Entry

A new channel entry is added to the mapping table during operation in three steps:

1. An address pointer is added at the top of the pointing table.
2. A VCI/VPI match entry is added to the top of the address mapping table.
3. AMEND is updated to point to the new entry (this step lets the new entry be used by the CP).

4.1.1.2 Removing a Channel Entry

A channel entry is removed from the mapping table during operation in three steps. Note that a channel entry can be removed only when channel has stopped sending cells. Remove a channel entry as follows:

1. Move the top pointer of the pointing table (that is, the pointer parallel to AMEND) to the position to be deleted.
2. Move the top entry of the match table (the VCI/VPI match entry specified by the AMEND pointer) to the position to be deleted.

3. Increment the AMEND pointer by 2, moving it one entry toward AMBASE.

4.1.2 Address Compression

Address compression is selected by setting SRFCR[EXT] and SRFCR[ACP] to 1. This mapping method is based on dual-level address compression through two levels of addressing tables. Dual-level address compression allows maximum flexibility of the cell header while using a minimum amount of memory.

In the first level, the GFC, VPI, and PTI fields of the received header are masked together to create a pointer (consisting of the offset from FLBASE) to the first-level addressing table. The first-level table (FLT) contains an additional mask and table pointer to one of the second-level tables (referred to as the second-level table offset (SLTOFFSET)). In the second stage, the VCI bits are masked (using the contents of the SLMASK field in the first-level table) and used as a pointer to an entry in the second-level table (SLT) addressed by SLTOFFSET. This second-level table entry contains the channel number of the received cell.

4.1.2.1 First-Level Addressing Table

The size of the first-level addressing table depends on the number of mask bits in the FLMASK. If, for example, FLMASK contains a sequence of 10 “1” bits, pointer1 will contain 10 bits and the resulting size of the table is 4 Kbytes. The actual address of the pointer entry in the FLT is (FLBASE + pointer1 x 4).

Each entry in the FLT contains a 16 bit second-level mask (SLMASK) which is used to mask the incoming cell’s VCI. This mask should contain a sequence of 1 bits that operate in the same way as the FLMASK bit sequence. The FLT entry also contains a 16-bit second-level table offset (SLTOFFSET) that points to the SLT start address.

Part of the FLT may be unused, and is initialized with a null entry of 0x0. The 860SAR will transfer cells with a null entry pointer to the global raw cell queue.

NOTE: SLMASK should contain a chain of ones (1) and MUST contain at least one “1”. Failure to have at least one “1” in SLMASK will result in having the cells associated with the corresponding VP (VPI x FLMASK) routed to the raw cell queue.

4.1.2.2 Second-Level Addressing Tables

Each FLT entry points to a single SLT. The size of each SLT depends on the length of the sequence of bits set in SLMASK. For example, the size of an SLT with a sequence of 10 bits set in the SLMASK is 2 Kbytes. The actual address of an entry in an SLT is equal to (SLBASE + SLOFFSET + pointer2 x 2).

An SLT contains the channel number (0-65534) that matches the received cell header’s VCI and VPI.

4.1.2.3 Dual-Level Address Compression Example

Figure 4-2 shows an example of the address compression process. The first-level mask (FLMASK) was set to mask the third PTI bit and five VPI bits. Bitwise ANDing of the

FLMASK with the GFC, VPI, and PTI bits resulted in a 6-bit (in this example) pointer. Pointer1 is equal to 0x4, and therefore is pointing to the fourth entry of the first-level table. The first-level table contains a 16-bit mask (SLMASK) for the VCI field, and the second-level table offset (SLTOFFSET) pointer to one of the second-level tables. SLMASK masks VCI[5–7], resulting in a 7-bit pointer to the requested channel number in the second-level table.

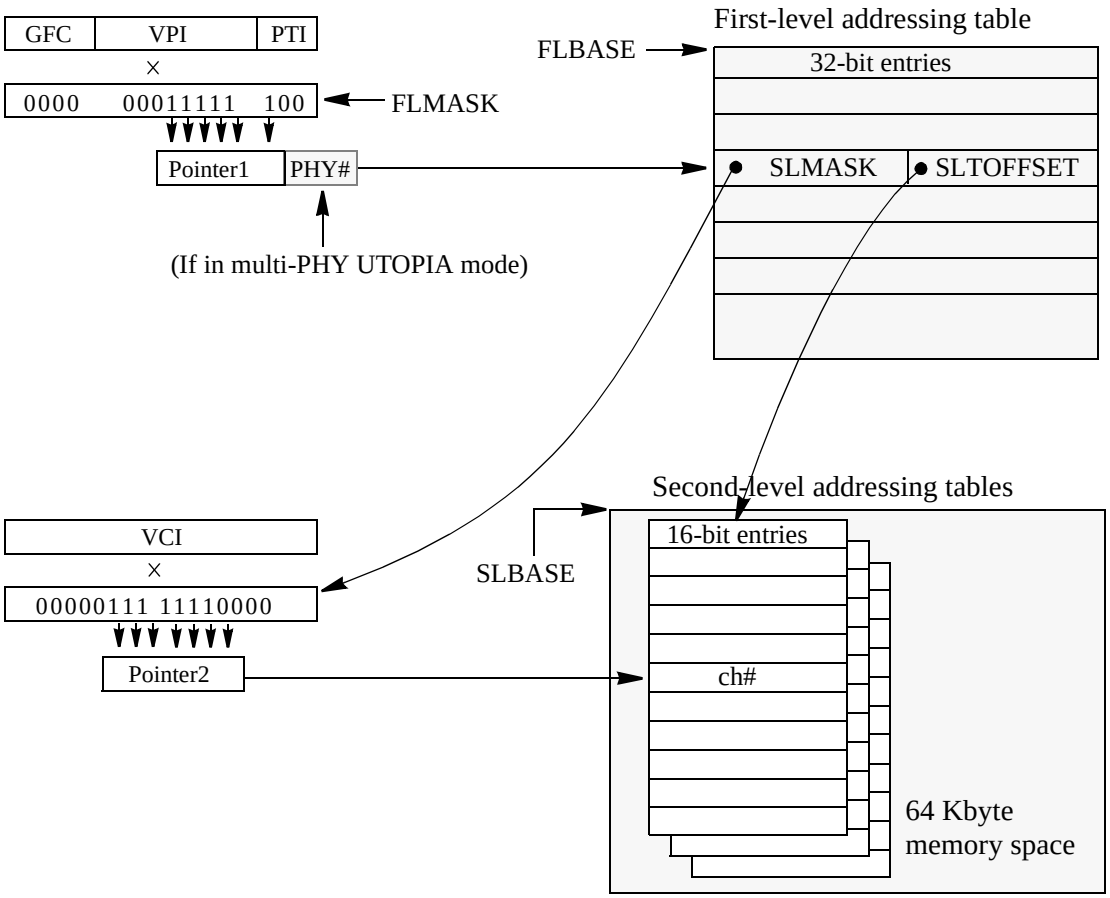


Figure 4-2. Address Compression

4.1.2.4 Anti-Channel Aliasing Function

Reliable one-to-one mapping of VCs to channel numbers requires that bits that are masked off have a fixed value (chosen to be zero). The CUMB feature allows the user to screen out misinserted cells by checking if unused bits in the address matching procedure are non-zero. If FLMASK[CUMB] is set, all unmasked bits from the first- and second-level mask process are tested to see if all are zero; cells that do not conform to this are passed to the global raw cell queue. Note that if CUMB is set, the user should also include the PTI bits in FLMASK, or all cells marked as congested (EFCI = 1) or last (PTI[1] =1) in the PTI will be sent to the global raw cell queue.

4.1.2.5 OAM Screening Function

If the most significant PTI bit in the FLMASK is equal to 0 (indicating that OAM/

managment cells are not a part of the address mapping process), and the most significant bit in the received cell header's PTI is set (indicating an OAM cell), the cell is passed to the global raw cell queue instead of being routed to the buffer indicated by the VPI/VCI mapping. This treatment keeps the OAM cells of an AAL5 connection from interfering with the SAR process, and allows the OAM cells to be processed separately.

4.1.2.6 Location of Connection Tables

Each entry in the SLT contains a channel number, where:

- Channel number 0—Reserved for the global raw cell queue. This RCT entry is located in the dual-port RAM pointed by CT_BASE.
- Channel number 1–31—The RCT for these connections are located in the dual-port RAM. The address of each RCT entry is (channel number x 64 + CT_BASE).
- Channel numbers greater than 31—Connection tables for these channel numbers are located in the external memory. The address of each RCT is equal to (channel number x 64 + ECT_BASE).

4.1.3 CAM Address Mapping

The CAM address mapping method is based on dual DMA accesses to an external CAM-based look-up table. CAM address mapping is selected by setting SRFCR[EXT] to 1 and clearing SRFCR[ACP] to 0. Following the receipt of a cell, the incoming header is masked by HMASK. The CP then performs a DMA write access to CAMADD with the address generated from the masked header as its data operand. The second access is a read DMA access to CAMADD. During this read access, the CAM should drive a "match successful" indication on the data bus[D0] signal, and the matched channel number on the [D16–31] signals. The "match successful" indication driven on data bus[D0] is active low, (a 0 indicates a successful match). If there is no "match successful" signal driven, the cell is passed to the global raw cell queue.

4.2 Multi-PHY Configuration (MPHY)

The 860SAR can handle up to 4 different PHYs in UTOPIA mode. The interface to the PHYs is done through the UTOPIA and 4 additional port B signals. The configuration of parameters for multi-PHY operations is described in this section.

4.2.1 Setting Multi-PHY mode

To initiate multi-PHY mode the user must set the MPY bit in the SRSTATE, STSTATE and APCST fields in the parameter RAM. The user must also select UTOPIA mode (through the PDPAR[UT] bit) and set the number of PHYs in the NMPHY field of APCST.

When operating in multi-PHY mode the two least-significant bits of the channel number entry in the pointing/address tables represent the associated PHY number. The format of the Pointing Table, Second Level Addressing Table, or CAM entries is shown in Figure 4-3. This is also the format used when activating a multi-PHY channel. The transmit queue entries have

this format (needed to identify the transmitting channel's PHY).

Figure 4-3. Multi-PHY Pointing Table Entry

4.2.2 Receive Multi-PHY Operation

A receive operation starts with the PHY address driven on PHREQ[0–1] and the assertion of RxCav by one of the PHYs. The 860SAR reads the PHY number through PHREQ[0–1] and writes the selected address to PHSEL[0–1] before to the assertion of $\overline{\text{RxEnb}}$.

4.2.2.1 Look-up Table MPHY Support

When performing multi-PHY operations the user must prepare up to 4 separate look-up and pointing tables (thereby providing a table set for each PHY). The AMBASE, APBASE and AMEND values used for all PHYs during multi-PHY operations are configured as shown in the following calculations:

$$AMBASE\{N\} = AMBASE + N \times 8 \times 4$$

$$AMEND\{N\} = AMEND + N \times 8 \times 4$$

$$APBASE\{N\} = APBASE + N \times 8 \times 2$$

In the preceding calculations, N represents the PHY number. When performing multi-PHY operations using the internal dual-port RAM, each PHY may use up to 8 channels (as only 32 channels are available in the internal dual-Port RAM). Note that one channel out of each group of 8 must be reserved for the global raw cell queue. If the extended channel mode operation is selected, more than 8 channels per PHY are supported. Figure 4-4 shows the configuration of the address mapping tables for multi-PHY operations.

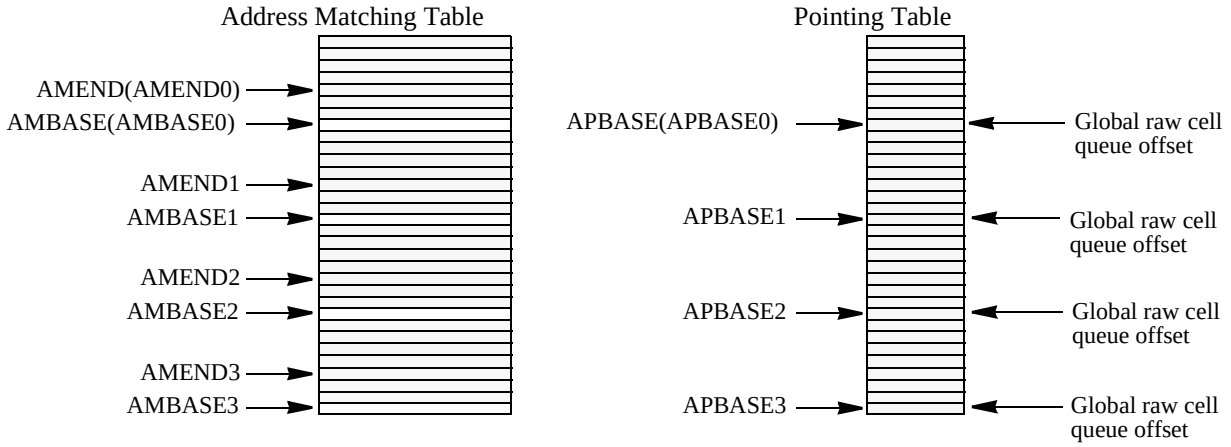


Figure 4-4. Address Mapping Tables for Multi-PHY Operations

Note that the address in the AMEND field is common to the four look-up tables. AMEND points to the highest valid channel number in any one of the four tables. For example, if PHY3 handles 5 channels and the other PHYs handle only 2 channels, the address in AMEND should be set to point to the fifth channel of PHY3. The unused address pointers in PHY0, PHY1, and PHY2 should point to the raw cell queue.

4.2.2.2 Address Compression Multi-PHY Support

During multi-PHY operations the 2-bit PHY address is appended as the least significant bits of the first-level address pointer.

4.2.2.3 CAM Multi-PHY Support

When performing CAM addressing the PHY address is added to the CAMADD address. The user must configure the CAMADD field with the last 5 address bits cleared. The PHY address is driven on the ADDR[28–31] signals during the CAM access. This allows the user to use either 4 separate CAMs with each mapped to its own address, or to have a single unified CAM with the ADDR[28–31] signals used as part of the match data for the CAM.

4.2.3 Transmit Multi-PHY Operation

A transmit operation starts with the assertion of the TxCav signal. This signal signals the ability of all PHY interfaces to load a cell in their transmit FIFOs. The 860SAR indicates the PHY selected for transmission by writing the PHY number on PHSEL[0–1] prior to assertion of $\overline{\text{TxEnb}}$.

4.2.4 APC Multi-PHY Parameters

Each PHY in multi-PHY mode has a dedicated APC. The APC parameter table is extended to include the parameters for each APC. The APCPTR field in the parameter RAM points to the first table (MPHY0), and the parameter tables for the remaining PHYs are attached to the bottom of the first table. For example, the address (APCPTR+32) will point to MPHY1 parameter table, (APCPTR+64) will point to MPHY2 parameter table, and (APCPTR+96) will point to MPHY3 parameter table.

4.3 MPC860SAR Commands

The host issues commands to the 860SAR by writing to the CPM command register (CPCR). The 860SAR commands are similar to those of the standard MPC860 protocols (refer to the MPC860 PowerQUICC User’s Manual for additional information). The CPCR format for 860SAR is shown in Figure 4-5. All the available commands are described in the following section. All other initialization and function enabling is implicitly configured through parameter bit setting. Note that the worst case command execution latency is 480 clocks and the typical command execution latency is 40 clocks (serial mode) or 180 clocks (UTOPIA mode).

BITS	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
FIELD	RST	860SAR OPCODE			OPCODE = 1111[1]				CH_NUM[2]				—	APC_LEV		FLG
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR																

Notes:

1. Opcode for all 860SAR commands = 1111.
2. The 860SAR commands have a channel number associated with them. The channel number must be written by the user in the COMM_CH field of the parameter RAM prior to writing the command into the CPCR.

Figure 4-5. CPM Command Register (CPCR)

Table 4-1 describes the configuration of the CPCR for SAR operations.

Table 4-1. CPCR Field Descriptions

Bits	Name	Description
0	RST	—
1–3	860SAR OPCODE	860SAR opcode. This field contains the 3-bit opcode of the channel command. 000 Transmit channel activate 001 Transmit channel deactivate 010 Stop transmit (abort) 011 Restart transmit 100 Stop receive 101 Restart receive 110 APC bypass
4–7	OPCODE	Opcode. This field must always contain 0b1111.
8–11	CH_NUM	Channel Number. The CH_NUM field specifies the SCC for a command issued to a serial-mode channel. For a command issued to a UTOPIA mode channel, the CH_NUM field should specify SCC4. Refer to the CPCR definition in the MPC860 PowerQUICC User's Manual for more information.
13–14	APCLEV	APC Level. This field is valid only for the transmit activate channel command only. APCLEV specifies into which level of the APC table the current channel should be inserted. 00 Insert the channel to first-level APC table. 01 Insert the channel to second-level APC table. 1x Reserved
15	FLG	—

The commands supported by the 860SAR are described in Table 4-2.

Table 4-2. MPC860SAR Commands

Command	Opcode	Description
Transmit activate channel	000	This command activates the channel specified by COMM_CH by inserting its channel number into the APC table at the location indicated by the service pointer. The channel most recently inserted is the first to be chosen by the APC. This command can be issued only after initializing the channel by preparing valid BDs and an entry in the TCT. If the same channel was deactivated, a period of time equal to (APC_length x APC slot time) must be maintained by the user between deactivation and activation commands, thereby allowing an entire APC table scan between commands.
Transmit deactivate channel	001	This command deactivates the channel specified by COMM_CH by extracting its channel number from the APC table and removing its channel number from the transmit queue, if it has been inserted there by the APC. This command should not be issued before the CP completes transmitting all the BDs associated with the current channel number. The TCT entry can be assigned to a different channel only after this command has been executed. The time required for deactivation is equal to (APC_length x APC slot time). The activation of the same channel number also requires a time period equal to (APC_length x APC slot time) after the execution of this command.
Stop transmit (ABORT)	010	The stop transmit command instructs the transmitter to stop the transmission for the channel specified by COMM_CH. For AAL5 channels, the 860SAR sends an abort cell for the channel specified by COMM_CH. An abort cell terminates the transmission of the current frame by sending “last cell” with PTI[0] = 1 and message length = 0000. The abort cell is sent as soon as the channel is scheduled for next cell transmission by the APC. After this abort cell is transmitted the BD is closed. If the BD interrupt bit and IMASK[TXB] are set, an interrupt is signaled. For AAL0 channels, the transmission of cells will simply stop after the current cell. After the stop transmit command executes the transmitter places nothing into the transmit queue whenever the aborted channel is scheduled to transmit by the APC, effectively leaving a “null” in the transmit cell stream. After the transmit BD is closed the BD pointer is advanced to the next BD. Channel transmit operations can be restarted upon receipt of a restart transmit command.
Restart transmit	011	The restart transmit command restarts transmissions following a stop transmit command. This command is used to restart transmission at the current buffer descriptor.
Stop receive	100	The stop receive command stops the receiver from receiving cells for the specified channel. The CDIS bit in the RCT is set, and the INF bit is cleared. The current BD pointed to by RBD_PTR will remain empty. Any cells received for this channel number after the stop receive command executes are ignored.
Restart receive	101	The restart receive command restarts the receiver to allow receiving cells for the specified channel. RCT[CDIS] is cleared, and the receiver reinitiates data reception to the data buffer pointed to by the RBD_PTR.

Table 4-2. MPC860SAR Commands

Command	Opcode	Description
APC bypass	110	The APC bypass command inserts the specified channel number directly into the transmit queue. This command enables out-of-rate cell transmission, with cell pacing determined by the user. It is the user's responsibility to assure that the overall bit rate of the APC channels and the out of rate channels do not exceed the total bit rate available to the PHY. For 860SAR prior to rev C: The time from command execution to the time the cell is transmitted depends on the number of channels in the transmit queue and the command execution latency. For 860SAR rev C and later: The channel number inserted by the APC_BYPASS command is placed in the top of the transmit queue, and will therefore be the next channel sent. For 850SAR: Before activating this command, make sure the TQF bit in the STFCR is not set. The transmit queue should contain at least 2 entries when this command is issued.

Chapter 5
ATM Pace Control

The ATM layer performs cell multiplexing and demultiplexing. The ATM pace controller (APC) is part of the multiplexing process and actually processes the traffic parameters of each channel and defines the multiplex timing for all the channels. Cell multiplexing is done by the transmitter according to the traffic control function implemented by the APC.

5.1 APC Algorithm

The APC consists of four major parts:

- APC timer (Timer 4), supplying a global tick to the APC process
- APC table, a data structure used by the APC algorithm for scheduling channels at programmed intervals
- APC pace parameters (APC_Pace), defined in the TCT for each channel
- Transmit queue, holding scheduled channels (output of the APC algorithm)

The APC is a CPM process that dynamically reads the APC_period of each active transmit channel from the TCT and uses a periodic table-scanning algorithm to define the next channel to be transmitted. Having identified channels to be scheduled in its table scan, it then places the channel number of the selected channels in the transmit queue. The order in which the APC places channel numbers in the transmit queue is the order in which cells from the ATM channels will be multiplexed onto the line.

The transmit process is a separate CPM process from the APC algorithm, which exchanges information with the APC via the transmit queue. When the transmit process receives a request from the physical layer (either the SCC or the UTOPIA interface), the transmit process reads the transmit queue to determine the channel from which to transmit the next cell. The transmitter sends one cell for every channel number appearing in the transmit queue.

Figure 5-1 illustrates the APC process and transmit flow in UTOPIA mode. The APC obtains pacing data and channel numbers from TCT, and writes the channel number to the transmit queue. For AAL5 channels, the transmitter implements AAL and SAR functions on the external memory for the chosen channel. The transmitter then sends the cell through the UTOPIA interface to the PHY. The PHY implements the transmission convergence (TC) layer and the physical media dependent (PMD) layer.

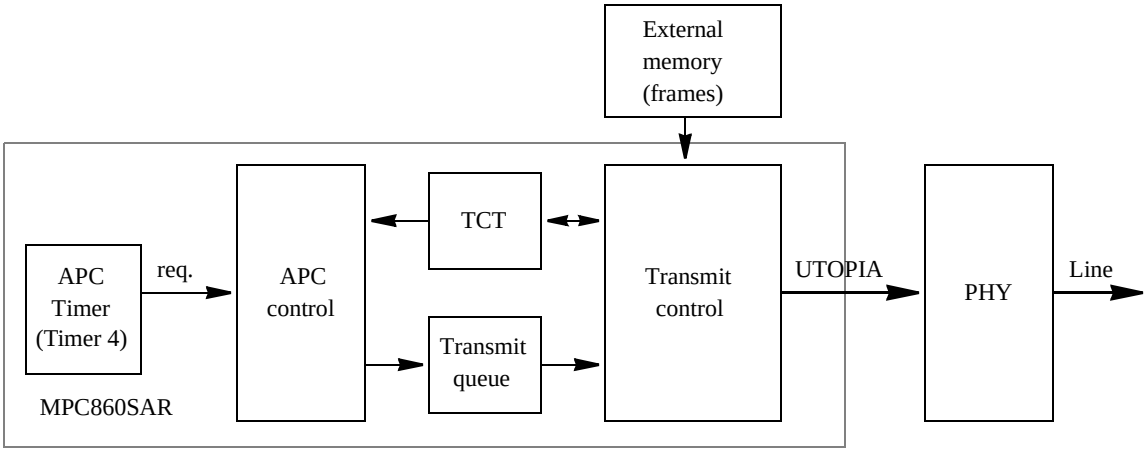


Figure 5-1. APC in the MPC860SAR UTOPIA Mode—Transmit Flow

5.1.1 APC Implementation Details

The APC is based on a dynamic scheduling table that contains pointers (implemented as channel numbers) to the channels of the TCT. The rate at which the table scan encounters a channel number in the scheduling table determines the transmit rate for that particular channel.

The APC table consists of an array of halfwords containing channel numbers, and two scan pointers (APC_PTRx and APC_SPTRx). Each table entry represents a time slot in which the number of cells specified by the parameter NCITS will be sent. The APC table is initialized with all null channel numbers (defined as 0xFFFF). Issuing the TRANSMIT_ACTIVATE_CHANNEL command to the CPM for a channel causes its channel number to be inserted in the APC table in the entry to which the table scan pointer (APC_PTRx) currently points.

Periodic timeouts of the APC timer activate the APC algorithm, which causes the table scan pointer (APC_PTRx) to advance one table entry in the APC table. Each time the table scan pointer steps to the next entry in the table, the APC reads the table entry to determine from which channels it should schedule cells for transmission.

The table entries in the APC table are actually the heads of linked lists. That is, if more than one channel is scheduled to the same time slot, the first channel points to the next channel to be sent (by means of the APC link field (APCL) in the TCT), and so on.

Having read the table entry, the APC inserts a certain amount (determined by NCITS) of channel numbers to the transmit queue. The APC then reschedules those selected channels a certain number of time slots (i.e. table entries) ahead, according to the APC Pace parameter in each channel’s TCT. If more than NCITS channel numbers are scheduled for the same time slot, the remaining channel numbers will pend until the next time slot. The lagging APC_SPTRx service pointer mechanism allows for this. Therefore, no cells are dropped; they are only deferred.

If a channel scheduled for transmission has no buffer descriptors ready, nothing is inserted into the transmit queue. This results in one or more idle cells in the cell stream.

5.1.2 APC Parameters

The APC mechanism is very flexible, in that it can be programmed to provide a wide variety of transmit rates and support a large number of channels. However, there are several important parameters which define its capabilities. These include:

- Cell scheduling rate. This effects the timeout rate of the APC timer (timer 4), which defines the period of the scheduling time slots, and the number of cells transmitted in a time slot (NCITS). The maximum of this rate is, of course, the bit rate of the physical medium. However, it could also be any amount less than that, if the user desires to use only a certain percentage of the bandwidth.
- Maximum and minimum bit rates supported for particular channels. A channel number can appear only once in a time slot, but must appear at least once during each table scan. The maximum bit rate for a particular channel is achieved when it is scheduled for transmission in every APC table entry (i.e. APC Pace = 1). the minimum bit rate for a particular channel is achieved when it is scheduled for transmission only once in a table scan (i.e. APC Pace = APC_table_size - 1). These limitations define the upper and lower bounds at which the transmit rate of a particular channel can be scheduled.
- APC table size and CPM performance. If the NCITS parameter is increased, the APC table size will decrease (thereby conserving dual-port RAM space) and the APC timer will make fewer requests to the CPM (thereby decreasing CPM processing overhead). However, increasing NCITS decreases the maximum bit rate supported and increases cell delay variation.

Therefore, tradeoff decisions must be made when programming these parameters. The following subsections provide examples of the analysis required to make these determinations.

5.1.3 Programming APC Table Size and NCITS

The size of the APC table is defined by the minimum bit rate desired for a single connection and the number of cells transmitted in a time slot.

Defining:

P = cell scheduling bit rate (usually equal to the PHY bit rate)

min_rate = minimum data rate at which a channel can be scheduled

max_rate = maximum data rate at which a channel can be scheduled

M = minimum APC table size allowable for a particular configuration

The maximum transmit data rate for a single channel supported by the APC is:

$$\text{max\_rate} = \frac{P}{NCITS}$$

The minimum transmit data rate for a single channel supported by the APC is:

$$\text{min\_rate} = \frac{P}{(M-1)NCITS}$$

For example, assuming a PHY transceiver with a transmit data rate of 51.84 Mbps, and assuming that the APC is to be configured to use all of this transmit bandwidth, then P = 51.84Mbps. Also assume that no single ATM channel (virtual connection) will ever require more than 25% of this bandwidth. By this assumption, (P / max_data) is 4, and we therefore choose NCITS to be 4. We also decide that no single connection will ever require a bandwidth less than 32kbps (i.e. min_rate = 32kbps).The minimum APC table size is therefore equal to:

$$M = \frac{\frac{51.84Mbps}{32kbps}}{4} + 1 = 406$$

We are fortunate in this example to be able to deal entirely in integers. However, note that while M must be an integer, NCITS may include an integer and a fraction. In any other application of this analysis, NCITS may be tuned in order to achieve an exact integer value M.

Note that a fractional value of NCITS does not mean that a fractional number of channel numbers will be written to the transmit queue. It means that the number of cells scheduled per APC timeout will vary around the average defined by NCITS. For example, if NCITS were programmed to 2.5, then 2 cells would be scheduled during one iteration of the APC algorithm, followed by 3 cells the next time, followed by 2, and so on.

5.1.4 Defining APC Slot Time

The APC defines the maximum bit rate of the cell scheduler through the period of the APC timer tick (timer 4) and the number of cells scheduled per APC timer tick (NCITS). The period of the APC timer is referred to as an APC time slot.

Defining:

P = cell scheduling bit rate (usually equal to the PHY bit rate)

TMR4 = timer 4 period, programmed in **T**imer **M**ode **R**egister.

Then:

$$P = \frac{\text{CLKOUT}}{\text{TMR4}}(\text{NCITS})(\text{number\_of\_bits\_per\_cell})$$

Using the previous example, if CLKOUT=50MHz, P=51.84Mbps, and NCITS=4, then TMR4 is approximately 1635.8. The closest value we can program in TMR4 is 103*16 = 1648, by programming TMR4[PS] = 0x96 and TMR4[ICLK]=0b10. We choose the next

largest value from that which we calculated; otherwise, the transmit queue would eventually overrun as the scheduler would provide slightly more traffic than the physical layer can transmit.

5.1.5 Programming Rates for Channels

The bit rate for a particular ATM channel is defined by that channel's APC pace parameter in its TCT entry. The APC pace value (APCP + (APCPF/65536)) for any channel must fall between 1 and (APC table size -1). Values outside this range result in erratic pace and/or table overflows (APCO interrupts). The maximum rate for transmission of a particular channel is achieved when APC pace is equal to one.

Defining:

P = cell scheduling bit rate (usually equal to the PHY bit rate)

des_rate = desired bit rate for this channel

Then:

$$\text{APC\_Pace} = \frac{P}{(\text{NCIST})(\text{des\_rate})}$$

For example, again using the previous example with P=51.84Mbps and NCIST=4, assume that a channel with a bit rate of 100kbps is desired. APC_Pace should therefore be programmed to 51.84Mbps / (4 * 100kbps) = 129.6. This can be approximated by programming APCP=129 and APCPF=39322.

For another example, assume the desired bit rate is 10Mbps. Then APC_Pace should be programmed to 51.84Mbps / (4 * 10Mbps) = 1.296. This can be approximated by programming APCP=1 and APCPF = 19399.

Note that APC Pace consists of an integer and a fraction. A channel with a non-integer APC_Pace will be scheduled such that its average pace will be as defined by APCP and APCPF. For example, if APCP and APCPF were programmed to define a pace of 1.5, then after transmission the channel would be alternately rescheduled either one time slot following or two time slots following, averaging to 1.5.

5.1.6 APC Initialization and Operating Considerations

As long as the APC timer (timer 4) is not active, the APC parameters may be initialized in any order. Timer 4 must be initialized last, following the initialization of the APC tables of all the ATM ports in the system. Failure to initialize timer 4 last will allow the scheduling algorithm to start prematurely, resulting in unpredictable behavior.

Furthermore, the APC table parameters must be initialized before any TRANSMIT_CHANNEL_ACTIVATE commands are issued. However, these commands may be issued at any time, whether the APC timer is active or inactive. For more information, see the description of the TRANSMIT_ACTIVATE_CHANNEL command.

Also, note that the physical interface (serial or UTOPIA) must be enabled and its associated clocks and synchronization signals must be active before the APC timer is activated. Otherwise, the transmit queue will simply overflow (causing an APCO interrupt).

5.1.7 Modifying Channel Transmit Pace

The APC Pace parameter in the TCT of any channel can be manipulated at any time. Software can use this capability to support various dynamic traffic types, such as ABR.

5.1.8 Minimizing Cell Delay Variation

The number of cells sent in each time slot (determined by the NCITS value) has an effect on the maximum cell delay variation (CDV) since the order of the cells in a given time slot is not controlled. Therefore, the CDV increases as the value in NCITS increases.

Also, as described before, the entries in the APC table are actually the heads of linked lists, which allows the APC to schedule multiple channels for the same time slot. These linked lists can be of unlimited depth, and although only NCITS cells will actually be written to the transmit queue each time the APC_PTRx advances, no cells will be lost because of the lagging APC_SPTRx service pointer. However, note that deeper linked lists will result in more cell delay variation. Therefore if cell delay variation is a concern, it is best, to schedule channels such that they distributed as uniformly as possible throughout the APC table. This can effectively be implemented by activating channels (by the TRANSMIT_ACTIVATE_CHANNEL command) at random intervals, such that they are not all written to the same APC table entry.

5.2 Direct Scheduling of Cells

The ATM controller implements an APC_Bypass command that allows the user to insert a channel number directly into the transmit queue on a cell-by-cell basis. This command can be used at any time in either serial mode or UTOPIA mode to insert a single cell for a channel into the transmit queue, with no direct transmit queue pointer manipulation required.

If the APC is programmed to never schedule cells (either by disabling timer 4 or by removing all channels from the APC table with TRANSMIT_CHANNEL_DEACTIVATE commands), then groups of cells can be directly scheduled for back-to-back transmission. To send *n* cells back-to-back in serial mode, the user would write *n* channel numbers to the transmit queue and then advance TQAPTR by *n*. To send *n* cells back-to-back in UTOPIA mode the user would write (*n* - 1) channels numbers to the transmit queue, advance TQAPTR by (*n* - 1), and issue an APC_Bypass command for the *n*th cell.

5.3 Using the APC with Multiple ATM Ports

The APC algorithm always begins in page 4 of the dual-port RAM. Thus, normally, when the 860SAR is configured with a single ATM port (in either UTOPIA or serial mode), the

ATM port operates in page 4 of the dual-port RAM. Although it is possible to run a single serial ATM port on SCC1, SCC2, or SCC3, this requires that the APCST parameter on page 4 of the dual-port RAM define the APC of page 4 as ‘inactive,’ and point to the active APC tables. The following discussion assumes that the APC for page 4 is active; however, the same general concepts apply to a system in which the APC for page 4 is inactive.

If the 860SAR is configured with multiple ATM ports, all the APCs are strobed by the same timer 4 request, which provides the common basic pace from which all the APCs are scheduled. Timer 4 activates several independent sub-timers in each APC implemented in the APCNT field of the APC parameters. Scheduling of cells from a particular APC will occur only when APCNT exceeds one. Timer 4 should be programmed to supply an optimized common pace for all the APCs. This pace can then be divided or multiplied by setting NCITS appropriately for each APC.

For example, if the 860SAR is configured for a 50 MHz system clock and implements two SARs one of which (in page3) is a 25-Mbps SAR and the other is a T1 serial SAR, timer 4 is programmed to generate an APC request every 4 cell times of the 25-Mbps SAR (timer 4 should be programmed to 50 MHz/25 Mbps*53*8*4 = 3392). An NCITS value of 4 is selected for the 25-Mbps SAR and an NCITS value of 0.24 for the 1.544-Mbps SAR so that the 25-Mbps APC will schedule 4 cells per timer 4 timeout, and the T1 APC will schedule one cell per 4.166 timer 4 timeout (an average of 0.24) for the T1 SAR.

In the example shown in Figure 5-2, the APCST[NSER] field in page 4 points to page 1, APCST[NSER] of page 1 points to page 4. When a timer 4 timeout occurs, the NCITS timer of page 1 is updated. Once per 4.166 requests the APCNT timer will exceed one, and APC1 schedules a channel for transmission. After the APCNT timer of page 1 is updated, APC2 is selected and schedules up to four NCITS channels.

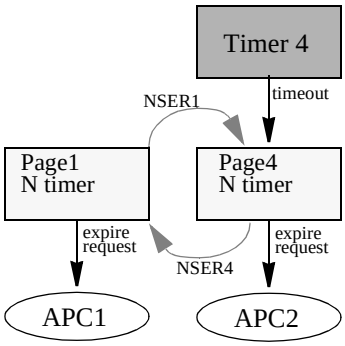


Figure 5-2. Example of Single PHY and Single Serial APC Configuration

Multi-PHY scheduling works in the same way as the scheduling process described above. Each PHY can support a different bit rate which is derived from the same timer 4 basic rate. In this way the 860SAR can support up to seven different APCs (four multi-PHY and three serial mode SARs). Upon a timer 4 timeout, the 860SAR will start servicing the serial APCs and then services multi-PHY3 through multi-PHY0. The order of serial APC service is defined by APCST[NSER]. Figure 5-3 shows the 860SAR fully configured with four multi-

PHY SARs and three serial mode SARs.

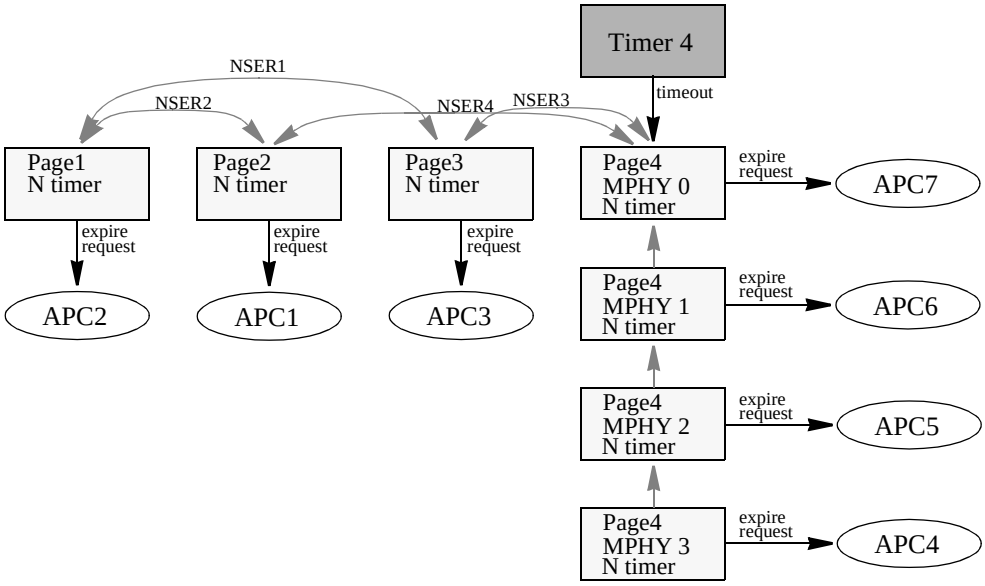


Figure 5-3. Example of Maximum Multi-PHY and Multi-Serial APC Configuration

5.4 Using the APC Without Using SCC4 or UTOPIA

As described in Section 5.3, “Using the APC with Multiple ATM Ports”, the APC algorithm begins and terminates by referring to the APCST parameter on parameter page 4. Therefore, the APCST parameter on parameter page 4 must always be valid, even if the communication channels associated with parameter page 4 (i.e. SCC4 or UTOPIA port) are not used in ATM mode.

If SCC4 or the UTOPIA port are not used, then the APCST parameter on parameter page 4 must indicate that the APC on page 4 is disabled, and must also point to the active APC page(s). This is accomplished using the APCST[NSER,CSER] mechanism described in Section 5.3, “Using the APC with Multiple ATM Ports”. The APC on parameter page 4 can be disabled by setting APCST[DIS].

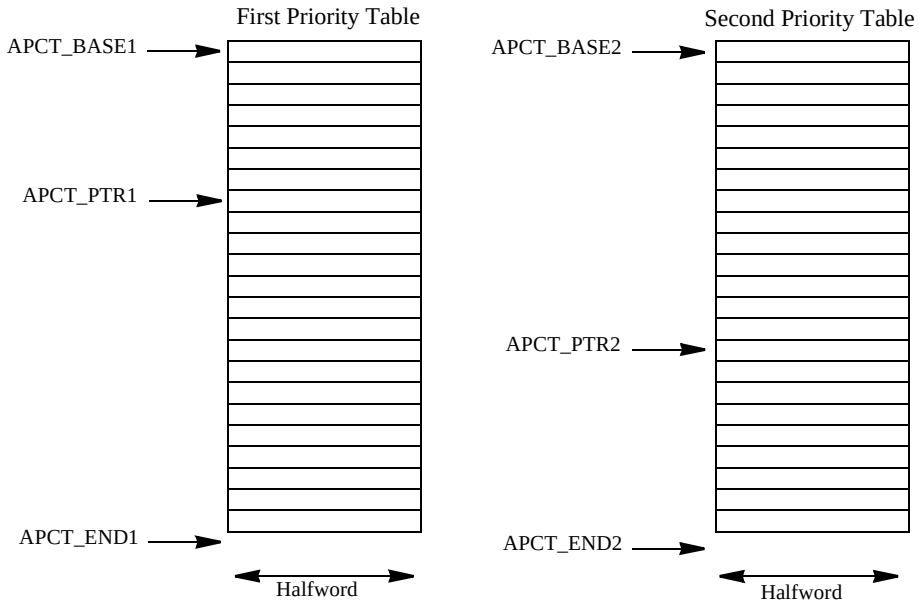
For example, if only SCC1 is used in ATM mode, then APCST on page 4 should be programmed to 0x0004, which sets APCST[NSER]=APCST[CSER]=00 (indicating SCC1) and APCST[DIS]=1. For the APCST on page 1, APCST[NSER] and APCST[CSER] should be programmed to 11, to point the APC algorithm back to page 4 to terminate.

Note, however, that by programming APCST4, the use of most other protocols on SCC4 is precluded, due to parameter RAM conflicts with this parameter. The only protocol which does not conflict with this parameter is transparent mode. Therefore, if the APC is used, then parameter RAM page 4 can only be used with SCC4 in transparent mode, SCC4 in ATM mode, or the UTOPIA port.

5.5 APC Table

The APC table is a memory space located in the dual-ported RAM. The user configures the number of entries in the APC table according to the required traffic parameters. The APC can be configured to handle two levels of priority through the configuration of APCST[PL2]. The APC will first schedule channels from the first priority table, scheduling up to NCITS channels from the APCT_PTR slot. If there are fewer than NCITS channels in this slot and the PL2 bit is set, the APC tries to select the rest of the channels from the second priority table. The total number of channels selected from both tables will always be NCITS or less. On each APC timeout, the APC advances the pointer of both tables by one slot. Note that during initialization all entries in the APC tables (from APCT_BASEx to APCT_ENDx) must be loaded with a value of 0xFFFF to indicate an empty slot. The first- and second-priority APC tables are shown in Figure 5-4.

Note that the first- and second- level tables need not be the same length; the length of the table effects only the minimum programmable transmit rate, which might be different for high-priority or low-priority channels.



Note: APCT_END points to one position after the last entry in the table

Figure 5-4. APC Table

5.6 Transmit Queue

The APC schedules up to NCITS channels in a time slot. It writes each channel number into the transmit queue in the position indicated by TQAPTR. The transmitter tracks the TQAPTR pointer and reads the channel numbers from the transmit queue and transmits a single cell for each channel. The channels to be sent lie between TQTPTR and TQAPTR. Figure 5-5 shows the organization of the transmit queue.

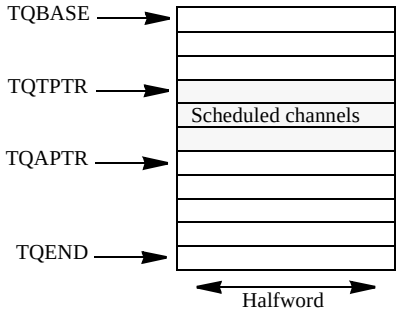


Figure 5-5. Transmit Queue

The transmit queue will never overflow because the TQAPTR pointer never wraps to point to the TQTPTR pointer. The depth of the transmit queue is equal to the number of entries minus 1. If the transmit queue is full the APC will not insert more channels, and the APC_SPTR stalls until space is available in the transmit queue.

5.7 APC Parameters

Table 5-1 describes the memory location and size of the user configurable parameters of the ATM pace controller. The shaded portion of the table contains the parameters used to configure the second priority APC table.

Table 5-1. APC Parameters

Address	Name	Width	Description	User Writes (hex)
APC Par + 00	APCT_BASE1	Half Word	APC table—First priority base pointer. See Table 5-2.	User defined
APC Par + 02	APCT_END1	Half Word	First APC table—Length. See Table 5-2.	User defined
APC Par + 04	APCT_PTR1	Half Word	First APC table pointer. See Table 5-2.	APCT_BASE1 value
APC Par + 06	APCT_SPTR1	Half Word	APC table first priority service pointer. See Table 5-2.	APCT_BASE1 value'
APC Par + 08 - 0F	Reserved	—	—	—
APC Par + 10	APC_MI	Half Word	APC—Max iteration	User defined
APC Par + 12	NCITS	Half Word	Number of cells in time slot. See Table 5-2.	User defined
APC Par + 14	APCNT	Half Word	APC—N timer	0000
APC Par + 16 - 1F	Reserved	—	—	—
APC Par + 20	APCT_BASE2	Half Word	APC table—Second priority base pointer	User defined
APC Par + 22	APCT_END2	Half Word	Second APC table—Length	User defined
APC Par + 24	APCT_PTR2	Half Word	Second APC table pointer	APCT_BASE2 value
APC Par + 26	APCT_SPTR2	Half Word	APC table second priority service pointer	APCT_BASE2 value‘

Table 5-1. APC Parameters

Address	Name	Width	Description	User Writes (hex)
APC Par + 28 - 3F	Reserved	—	—	—

Note:

1. The APC parameter table base address must be divisible by 32 (APCPTR must end with 00000).
2. Shadow area - Optional: Only used if APCST, PL2 bit is set.

Table 5-2 describes the operation of the user configurable ATM pace controller parameters.

Table 5-2. APC Parameter Descriptions

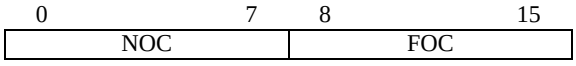
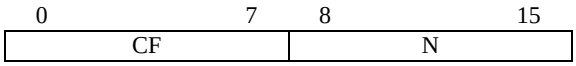
Name	Description
APCT_BASE1 and APCT_BASE2	APC table base for first and second priority tables. Holds the pointer to the first entry in each APC table. The pointers should be half-word aligned (even address).
APCT_END1 and APCT_END2	APC table end. Holds the end pointer of the APC tables, and is set to the address of the last entry in the APC table + 2 (APCT_END1=Last_Entry1+2 and PCT_END2=Last_Entry2+2).
APCT_PTR1 and APCT_PTR2	APC table pointers. Holds the location of the current APC time slot in the APC table. The APC advances both pointers by 1 on every APC N timer timeout. The APC table pointers should be initialized by the user to the APCT_BASE1 and APCT_BASE2 values respectively.
APCT_SPTR1 and APCT_SPTR2	APC table service pointers for first and second priority tables. Additional APC pointers used internally by the APC. The APCT_SPTR1 and APCT_SPTR2 parameters should be initialized by the user to the APCT_BASE1 and APCT_BASE2 values respectively.
NCITS	Number of cells in time slot. Parameter set by the user. It holds the number of cells which are transmitted in a time slot. This number can include fractions of a cell. The NCITS field is defined as follows:  The NCITS bit fields are described below. Bits / Name / Description 0–7 / NOC / Number of cells. This field contains the integer value for the number of cells. 8–15 / FOC / Fraction of cell. This field holds the fraction of cell where: $NCITS = NOC + \frac{FOC}{256}$

Table 5-2. APC Parameter Descriptions (Continued)

<table>
<tr><th>Name</th><th>Description</th></tr>
<tr><td>APCNT</td><td>APC N timer. Field in used internally by the APC. It should be initialized by the user to zero. The APC adds NCITS to this timer on every APC Timer request. This timer holds the APC N parameter and additional cell fraction remainder which is used by the APC. The APCNT field is defined as follows:
 

The APCNT bit fields are described below.
<table><tr><th>Bits</th><th>Name</th><th>Description</th></tr><tr><td>0–7</td><td>CF</td><td>Cell fraction used by the APC.</td></tr><tr><td>8–15</td><td>N</td><td>APC N parameter.</td></tr></table></td></tr>
<tr><td>APC_MI</td><td>Max iteration. Number of times/steps that the APC advances the service pointer. This parameter limits the time spent in a single APC routine, thereby avoiding excessive APC latency. The recommended value for APC_MI is equal to the minimum value of APCP of all channels, and should not exceed 32.</td></tr>
</table>

Chapter 6
Exceptions

Interrupt handling by 860SAR involves two principle data structures, the event register (SCCE or ISDR) and circular exception queue. The circular exception queue is shown in Figure 6-1.

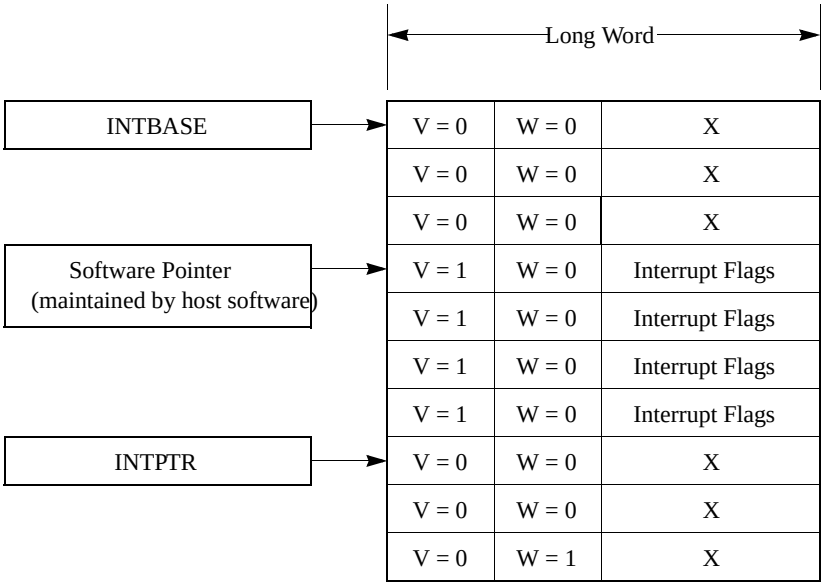


Figure 6-1. Circular Exception Queue

The INTBASE and INTPTR pointers are host-initialized global 860SAR parameters that respectively point to the starting location of the table in external memory and to the current empty position available to the CP. The end of the table is defined by the entry containing the W-bit set to 1. When one of the 860SAR channels generates an interrupt request, the CP writes a new entry to the table consisting of the channel's number and a description of the exception. The valid (V) bit is then set and INTPTR is incremented. When INTPTR reaches the location with the W bit set to 1, it wraps around so that INTPTR contains the same value as INTBASE.

After an interrupt request, the host reads the event register (SCCE or ISDR). A dedicated event register bit (GINT) indicates that at least one new entry was added to the table. After clearing GINT, the host starts processing the table and clears each entry's V bit. The host follows this procedure until it reaches an entry where V is 0.

The user must clear all interrupt bits in the table entry when servicing the interrupt. Otherwise, a later access to this location may reveal multiple interrupts, only one of which is the desired event.

6.1 Event Register

The event registers generate interrupts to the host and report on events that are common to all channels. The GINT bit indicates that a channel-specific interrupt was signaled in the interrupt table. In UTOPIA mode, the IDSR1 register is used as an event register, and in serial mode the SCCE register of each serial interface is used as an event register.

6.1.1 UTOPIA Mode Event Register (IDSR1)

The IDSR1 register is the 860SAR event register when the 860SAR is operating in UTOPIA mode. IDSR1 is used to report events and generate interrupt requests for the 860SAR UTOPIA interface. Note that in parallel mode, interrupts from the ATM channel are reported with an IDMA1 vector in the CIVR, and the IDMA1 bit set in the CIPR. For each flag in IDSR1 there is a programmable mask/enable bit in IDMR1 that determines whether an interrupt request is generated. The fields of the IDSR1 register are shown in Figure 6-2.

BIT	0	1	2	3	4	5	6	7
FIELD	RESERVED			SYNC	IQOV	GINT	RESERVED	

Figure 6-2. UTOPIA Mode Event Register (IDSR1)

Table 6-1 describes the IDSR1 bit fields.

Table 6-1. IDSR1 Field Descriptions

Bits	Name	Description
0–2	—	Reserved
3	SYNC	Cell synchronization changed status. Indicates that the 860SAR has lost the UTOPIA start of cell (SOC) indication. When this occurs the 860SAR stops receiving cells until it regains SOC synchronization. The SYNC bit in SRSTATE indicates that the 860SAR is waiting for resynchronization.
4	IQOV	Interrupt queue overflow. This bit is set (and interrupt request generated) by the CP whenever an overflow condition in the circular exception queue occurs. This condition occurs if the CP attempts to write a new interrupt entry into an entry that has not handled by the host (identified by the V bit set to 1).
5	GINT	Global interrupt. Indicates that at least one new entry in the circular exception queue was generated by 860SAR. The host clears GINT by a writing 1 to its location in IDSR1. After clearing the GINT bit, the host reads the next entry from the circular exception queue, and starts processing a specific channel’s exception. The host returns from the interrupt handler when it reaches a table entry with V = 0.
6–7	—	Reserved

6.1.2 Serial Mode Event Register (SCCE)

The SCCE is the 860SAR event register for serial mode. The SCCE is used to report events and generate interrupt requests. For each SCCE bit a programmable mask/enable bit in SCCM determines whether an interrupt request is generated. Note that in serial mode, interrupts from the ATM channel are reported with the appropriate SCC vector in the CIVR, and the appropriate SCC bit is set in the CIPR. Figure 6-3 shows the bit fields in the SCCE register.

BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
FIELD	RESERVED			GLR	GLT	DCC	RESERVED					SYNC	IQOV	GINT	GUN	GOV

Figure 6-3. Serial Mode Event Register (SCCE)

Table 6-2 describes the SCCE bit field settings.

Table 6-2. SCCE Field Descriptions

Bits	Name	Description
0–2	—	Reserved
3	GLR	Glitch on receive. A clock glitch has been detected by the SCC on the receive clock.
4	GLT	Glitch on transmit. A clock glitch has been detected by the SCC on the transmit clock.
5	DCC	DPLL carrier sense status change. Indicates carrier sense status generated by the DPLL has changed state. The value of the DCC bit is valid only when the DPLL is enabled.
6–10	—	Reserved
11	SYNC	Cell synchronization changed status. Indicates that the 860SAR has lost or gained cell delineation. The sync interrupt is signaled whenever the 860SAR changes lock status (refer to the ASTATUS lock bit in Section 3.1.5, “Serial Cell Synchronization Status Register (ASTATUS).” If sync loss occurs (lock bit is cleared), this interrupt indicates a fatal ATM reassembly error since it is unknown which channels were affected. Following the assertion of SCCE [SYNC] bit the 860SAR stops receiving data from all channels and all data transfer to memory is terminated. After re-initializing the channels, the host may resume receiving cells by executing the restart receive command for each channel. If enabled in the SCCM an interrupt request is generated when SCCE[SYNC] bit is set. The host clears SYNC by writing a 1.
12	IQOV	Interrupt Queue Overflow. This bit is set (and interrupt request generated) by the CP whenever an overflow condition in the circular exception queue occurs. This condition occurs if the CP attempts to write a new interrupt entry into an entry that has not been handled by the host (identified by the V bit set to 1).
13	GINT	Global Interrupt. Indicates that at least one new entry in the circular exception queue was generated by 860SAR. The host clears the GINT bit by setting it. After clearing the GINT bit, the host reads the next entry from the circular exception queue, and starts processing a specific channel’s exception. The host returns from the interrupt handler when it reaches a table entry with V = 0.

Table 6-2. SCCE Field Descriptions (Continued)

Bits	Name	Description
14	GUN	Global transmitter underrun. Indicates that an underrun occurred in the SCC's transmitter FIFO. A global transmitter underrun error is fatal, as the channel(s) affected by the underrun are unknown. Following the setting of the GUN bit, the 860SAR stops data transmission from all channels and sets APCST[DIS], and the transmit line enters an idle state (logic high). After re-initializing the channels, the host may resume transmitting by issuing a restart transmit command for each channel through the CPCR. If enabled in the SCCM an interrupt request is generated when GUN is set. The host clears GUN by writing a 1 to it. For fast recovery from a GUN error the user can reinitialize TSTATE by writing the STFCR value to the first byte and zeroes to the second byte and restart the APC by clearing APCST[DIS]. This will result in some corrupted transmit frames, as the user normally only writes to TSTATE during initialization. [Note also that clearing APCST[DIS] may be overwritten by the APC scheduling task, and therefore the user should verify after at least 50 system clocks that APCST[DIS] was indeed cleared.]
15	GOV	Global receiver overrun. Indicates that an overrun occurred in the SCC's receiver FIFO. A global receiver overrun error is fatal, as the channel(s) affected by the overrun are unknown. Following the setting of GOV the 860SAR stops receiving data from all channels and all data transfer to memory is terminated. After re-initializing the channels the host may resume receiving by executing the restart receive command for each channel through the CPCR. If enabled in the SCCM, an interrupt request is generated when GOV is set. The host clears GOV by a 1 to it. For fast recovery from a GOV error the user can reinitialize RSTATE by writing the SRFCR value to the first byte and zeroes to the second byte. This will result in some corrupted receive frames which should be disposed of by software; normally the user only writes to RSTATE during initialization.

6.2 Exception Queue Entry

The exception queue contains information about channel specific events. The exception queue entry flags are shown in Figure 6-4.

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
OFFSET + 0	V	W	—	CNG	—	—	—	—	APCO	—	—	UN	RXF	BSY	TXB	RXB
OFFSET + 2	CHNUM															

Figure 6-4. Exception Queue Entry

Table 6-3 describes the exception queue entry bit fields.

Table 6-3. Exception Queue Entry Field Descriptions

Bits	Name	Description
0	V	Valid bit. Indicates that this entry contains valid interrupt information. Upon generating a new entry, the CP sets this bit. The V bit is cleared by the host immediately after it reads the interrupt flags in this entry. The V bits in all entries must be cleared to 0 by the host during initialization.
1	W	Wrap bit. Indicates the last entry in the circular exception queue The next event's entry in the interrupt circular table is written/read by the CP or host from the address contained in INTBASE. During initialization the host must clear all W bits in the queue except the one in the last entry, which is set to indicate the end of the queue.
2	—	Reserved

Table 6-3. Exception Queue Entry Field Descriptions (Continued)

Bits	Name	Description
3	CNG	Congestion (AAL5 only). Set by the CP if there is a congestion indication on a received cell (indicated by the PTI middle bit set to 1). This interrupt is signaled only for channels with the CNGI bit set in the RCT. For AAL0 channels, the CNG indicator, along with the other header information, can be found in the RX buffer.
4	—	Reserved
5	—	Reserved
6	—	Reserved
7	—	Reserved
8	APCO	APC overrun. Set by the CP if an APC overrun occurs. This interrupt indicates that the total cell rate which was programmed in the APC is higher then the cell rate capability of the transmitter. Specifically, the APC_PTR has wrapped around to the APCT_SPTR position, effectively causing an entire APC scheduling pass to be lost. Note that no cells have been lost, but the cell rate of all the channels has been diminished below the programmed rate. This only occurs when (1) the programmed pace is greater than NCITS (that is, if NCITS = 1, and 1/APCP1 + 1/APCP2 + 1/APCP*n* > 1), or (2) the APCT_SPTR has stalled for some reason, such as a full transmit queue. The address of the APC table associated with the exception is placed in the CHNUM field of the dual-ported RAM.
9	—	Reserved
10	—	Reserved
11	UN	Transmit underrun. Occurs for both AAL0 and AAL5 any time a channel is scheduled to transmit and there is insufficient data to send a complete cell to the transmitter. No other action is taken and the channel remains enabled; if more data is not supplied, another UN exception will be generated the next time that the channel is scheduled. When an underrun occurs, an idle cell will be sent, either generated by the 860SAR (in serial mode) or by the UTOPIA PHY (in UTOPIA mode).
12	RXF	Receive frame. This interrupt signals that a complete AAL5 frame has been received.
13	BSY	Busy. Indicates that a cell was received but was discarded due to lack of empty buffers. For AAL0, the 860SAR will attempt again to open the BD when the next cell for this channel arrives. For AAL5, following the signalling of a BSY interrupt, the remaining cells for the current AAL5 frame will be discarded until a cell with last cell indication (PTI[1]=1) is received; at this point, the 860SAR will attempt again to open the BD when a cell from the next frame is received.
14	TXB	Transmit buffer. Set (and an interrupt request is generated) when the transmitter sends the last cell in a buffer to the UTOPIA interface when operating in UTOPIA mode, or to the serial FIFO when operating in serial mode. This exception is enabled through the I bit in the transmit BD.
15	RXB	Receive buffer. Set when a buffer has been received for a BD with the I bit set, and (for AAL5) the buffer was not the last buffer in frame. This interrupt is enabled through the I bit in the receive BD. This interrupt is also generated by various errors that occur during receive operations. The error conditions that caused the interrupt are reported in the receive BD.
0–15	CHNUM	Channel number. The channel number field identifies the interrupt channel index. When operating in regular mode, the CHNUM is the channel's RCT address in dual-ported RAM when receiving, or TCT address when transmitting. When operating in extended channel mode, the CHNUM field contains the actual channel number. If the interrupt is the result of an APC overrun (signaled by the APCO bit), the CHNUM field contains the dual-port RAM offset of APCT_BASEx of the APC table experiencing the overrun.

6.3 Interrupt Table Mask (IMASK)

The IMASK field in the RCT is common to the receiver and the transmitter. The IMASK field allows the user to enable or disable any of the interrupts that in turn generate a global interrupt (GINT) in the exception queue. If a bit in the IMASK field is cleared, the interrupt corresponding with the bit in the exception queue entry is not signaled in the exception queue, and the GINT interrupt counter is not advanced. The bit positions in the IMASK field is identical to those of the exception queue entry except for V, W, and APCO bits, which are not implemented in the IMASK field.

Chapter 7
Interface Configuration

The following sections describe the configuration of the 860SAR's registers for ATM operations through the UTOPIA and serial interfaces.

7.1 General Registers

The following sections describe the general registers implemented on the 860SAR

7.1.1 Port D Pin Assignment Register (PDPAR)

The ATM and UT bits have been added to the PDPAR register, shown in Figure 7-1. The PDPAR register is cleared at system reset.

Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Field	ATM	UT	—	DD3	DD4	DD5	DD6	DD7	DD8	DD9	DD10	DD11	DD12	DD13	DD14	DD15
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Oper	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	OFFSET TO IMMR: 0X972 (PDPAR)															

Figure 7-1. Port D Pin Assignment Register (PDPAR)

The fields in the PDPAR register are described in Table 7-1.

Table 7-1. PDPAR Field Descriptions

Bit	Name	Description
0	ATM	ATM enable. Determines whether SAR operations are enabled. 0 =No SAR functionality 1 =ATM SAR functionality
1	UT	UTOPIA enable. Determines whether page4 operates in serial or UTOPIA mode. 0 =Serial mode using SCC4 1 = UTOPIA mode
2	—	Reserved

Table 7-1. PDPAR Field Descriptions (Continued)

Bit	Name	Description
3–15	DDx	Signal assignment. Determines whether signal is a general-purpose I/O signal or performs dedicated function. 0 =General-purpose I/O. The peripheral functions of the signal are not used. 1 =Dedicated peripheral function. The signal performs the function assigned by the internal module.

7.1.2 Timer 4

Timer 4 is used internally by the ATM pace controller for both serial and UTOPIA modes. Timer 4 should be programmed to run in active-low pulse and restart mode (refer to the *MPC860 PowerQUICC User's Manual* for additional information about timer configuration). The timer 4 period should be programmed according the required APC rate which is discussed in Chapter 5, "ATM Pace Control."

7.1.3 CP Timer

The CP timer specified by the TSTA field in the parameter RAM is programmed by host software with the desired time-out interval. This timer allows the host to determine if a receive time-out has occurred.

7.2 UTOPIA Mode Registers

When operating in UTOPIA mode the PHY layer is connected to the 860SAR UTOPIA interface. The UTOPIA data signals and some of the control signals are connected to port D. The remaining UTOPIA control signals are connected to port B and C. The UTOPIA mode requires several 860SAR registers to be configured as described in the following sections.

7.2.1 System Clock Control Register (SCCR)

The system clock control register is described in the *MPC860 PowerQUICC User's Manual*. Bits 27–31 are defined to control the UTOPIA clock (UTPCLK).

The frequency of UTPCLK defaults to system frequency. The ratio between the system clock frequency value and the UTPCLK clock value is an integer value ($freq_{syst}/freq_{utpia}$ = integer > 0). The UTOPIA clock has a 50% duty cycle and is derived from the system frequency divided by two dividers. Note that the UTOPIA clock must be programmed to operate at a frequency less than or equal to 25 MHz. The SCCR[DFUTP] and SCCR[DFAUTP] fields should be set such that the total UTOPIA clock division factor never exceeds 5 (that is, the bounds of UTPCLK are 25 MHz > UTPCLK > SYSCLK/5). The UTOPIA clock frequency can be determined using the following formula:

$$FREQ = \frac{FREQsysmax}{(2^{DFUTP}) \times (2 \times DFAUTP + 1)}$$

For example, to achieve a 25-Mhz UTOPIA clock with a 50Mhz 860SAR system clock, the DFUTP field should be set to 1 and the DFAUTP field should be cleared to 0. The SCCR is shown in Figure 7-2.

BIT	0		27	28	29	30	31
FIELD	As specified in the *MPC860 PowerQUICC User's Manual*		DFUTP			DFAUTP	
RESET			0	0	0	0	0
OPER			R/W	R/W	R/W	R/W	R/W
ADDR	OFFSET TO IMMR: 0X280 (SCCR)						

Figure 7-2. System Clock Control Register (SCCR)

The fields in the SCCR register are described in Table 7-2.

Table 7-2. SCCR Field Descriptions

Bit	Name	Description
27–29	DFUTP	Division factor. Divide the system clock by $2^{\text{DFUTP value}}$. Note that the system clock division factor is limited to 4.
30–31	DFAUTP	Additional division factor for the UTPCLK. Divide the system clock by the following value: 00 = Divide by 1 01 = Divide by 3 10 = Divide by 5 11 = Reserved

7.2.2 Port B—TxCAV Signal

The 860SAR port B includes the TxCav input signal. PB15 is configured to support the TxCav signal when PBPAR[15] is set and PBDIR[15] is cleared.

NOTE: The 850SAR TxCav signal is included in PORT C, PC[12]. PCPAR[12] and PCDIR[12] should be cleared and PCSO[12] should be set.

UTOPIA MPHY operations require the use the port B PHREQ[0–1] and PHSEL[0–1] signals. These signals are configured by clearing PBPAR[16–21] and PBDIR[16–17], and setting PBDIR[20–21].

NOTE: The 850SAR UTOPIA MPHY operations require the use the port B PHREQ[0–1] and PHSEL[0–1] signals. These signals are configured by clearing PBPAR[16–17], PBPAR[19] and PBPAR[22] and PBDIR[16–17], and setting PBDIR[19] and PBDIR[22].

7.2.3 Port C—RxCav Signal

The 860SAR port C includes the RxCav input signal. When PDPAR[UT] is set, DREQ0[PC15] is configured to support the RxCav signal. The PCPAR and PCDIR fields must be cleared and the PCSO field must be set to enable the RxCav signal input on the PC15 signal.

7.2.4 Port D—UTOPIA Data and Control Signals

The 860SAR port D includes the UTOPIA data and control signals. When PDPAR[UT] is

set, most of the port D signals are configured to support UTOPIA signals as shown in Table 7-3. The UTOPIA interface is described in Chapter 8, “UTOPIA Interface.”

NOTE: Port D **MUST** be initialized before Port C to prevent the CPM from trying to use IDMA functionality.

Table 7-3. Port D Pin Assignment

Signal	Signal Function			
	PDPAR = 0	PDPAR = 1, PDDIR = 0		Input to On-Chip Peripherals
		UT = 0	UT = 1	
PD15	PORT D15	L1TSYNCA	UTPB[0]	L1TSYNCA=GND
PD14	PORT D14	L1RSYNCA	UTPB[1]	L1RSYNCA=GND
PD13	PORT D13	L1TSYNCB	UTPB[2]	L1TSYNCB=GND
PD12	PORT D12	L1RSYNCB	UTPB[3]	L1RSYNCB=GND
PD11	PORT D11	RXD3	$\overline{\text{RxEnb}}$	—
PD10	PORT D10	TXD3	$\overline{\text{TxEnb}}$	—
PD9	PORT D9	RXD4	UTPClk	—
PD8	PORT D8	TXD4	—	—
PD7	PORT D7	$\overline{\text{RTS3}}$	UTPB[4]	—
PD6	PORT D6	$\overline{\text{RTS4}}$	UTPB[5]	—
PD5	PORT D5	$\overline{\text{REJECT2}}$	UTPB[6]	$\overline{\text{REJECT2}}$=VDD
PD4	PORT D4	$\overline{\text{REJECT3}}$	UTPB[7]	$\overline{\text{REJECT3}}$=VDD
PD3	PORT D3	$\overline{\text{REJECT4}}$	SOC	$\overline{\text{REJECT4}}$=VDD

7.2.5 CP Controller Configuration Register (RCCR)

The RCCR[DR0M] and RCCR[DR1M] bits must be set for UTOPIA mode operation. Set RCCR[DRQP] to 01 to give SCC transfers higher priority.

7.2.6 UTOPIA Mode Initialization Process

The following procedure is required for proper initialization of the UTOPIA interface:

1. Configure the ATM parameters and data structures before initializing the UTOPIA port. The UTOPIA port activates immediately upon initialization, and if its associated data structures are not initialized, the CPM will lock up.
2. Set SRFCR[DIS] to 1 to mask the RxCav signal.
3. Program PDPAR and PDDIR.Note that when the PDPAR[ATM] and PDPAR[UT] bits are set there is a spurious assertion of RxCav that is masked by SRFCR[DIS].
4. Program PCPAR, PCDIR, and PCSO to enable RxCav.

5. Program PBPAR and PBDIR to enable TxCav.
6. Clear SRFCR[DIS] to unmask the RxCav signal, thereby enabling the UTOPIA interface. At least 20 system clocks must elapse between the configuration of the PDPAR and clearing SRFCR[DIS].

The 860SAR starts searching for SOC and sets SNC as soon as the first SOC is found.

If at any time software re-initializes the UTOPIA port (e.g. as part of a ‘warm boot’ procedure), the RxCav signal should be disabled before this procedure is restarted (i.e., the PCPAR, PCDIR, and PCSO should be programmed to disable RxCav).

7.3 Serial Mode Configuration

860SAR serial mode ATM operations use one or more SCCs and serial interfaces. The following sections describe the configuration of registers for serial mode ATM operations.

7.3.1 CP Controller Configuration Register (RCCR)

The RCCR[DR1M] bit must be set, and RCCR[DRQP] field must be programmed to 01 to allow higher priority for SCC transfers.

7.3.2 SCC Configuration

The following sections describe the configuration of the SCC registers for serial ATM operations. Note that the ATM parameters and data structures must be initialized before enabling the SCC. Otherwise, the SCC will activate immediately, and if its associated data structures are not initialized, the CPM may lock up.

7.3.2.1 General SCC Mode Register (GSMR)

The use of an SCC as an ATM controller requires the setting of the TRX, TTX, CDP, CTSP, CDS, and CTSS bits in the GSMR. When the initialization sequence has been completed, GMSR[ENT] and GMSR[ENR] must be set to enable transmit and receive functions. Additional information about the configuration of the GSMR is provided in the *MPC860 PowerQUICC User’s Manual*.

To enable an SCC to operate in ATM serial mode, the GSMR[MODE] bits must be set to transparent mode and have MRBLR = 0. If the MRBLR is configured with a non-zero value, the SCC operates in transparent mode.

An 860SAR operating in serial mode does not support mixed mode SCC operation (in which the transmitter is configured for ATM transmissions, and the receiver is in transparent mode or vice versa).

7.3.2.2 Protocol-Specific Mode Register (PSMR)

The SCC protocol specific mode register (PSMR) controls the various protocol-specific SCC functions. The user should initialize the PSMR only when the transmitter and receiver are disabled, or undefined behavior can result.

The PSMR controls the scrambling and HEC coset functions of the ATM controller for both the transmitter and receiver. The PSMR is shown in Figure 7-3.

BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
FIELD	—	—	SCRAM	—	—	—	—	COSET	—	—	—	—	—	—	—	—
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR																

Figure 7-3. Protocol-Specific Mode Register (PSMR)

The fields of the PMSR are described in Table 7-4.

Table 7-4. PSMR Field Descriptions

Bits	Name	Description
0–1	—	Reserved
2	SCRAM	Scrambling function 0 = Disable cell payload scrambling during transmission and reception. 1 = Enable cell payload scrambling during transmission and reception.
3–6	—	Reserved
7	COSET	HEC coset function 0 = Do not apply the HEC coset rules. 1 = Apply the HEC coset to all transmitted and received cells.
8–15	—	Reserved

7.3.2.3 SCC Event Register (SCCE)

The generation and handling of 860SAR exceptions are described in Chapter 6, “Exceptions.”

7.3.2.4 SCC Mask Register (SCCM)

The SCCM has the same bit definitions as the SCCE and allows the user to mask interrupts. Additional information about the configuration of the SCCM is provided in the *MPC860 PowerQUICC User’s Manual*.

7.3.3 Serial Interface Configuration

When operating the 860SAR in serial mode, the user can use the serial interface in either NMSI mode or through the time slot assigner. Note that the time slot assigner (TDM) mode allows easy connection to E1, T1, and ADSL line interface devices. Either of the TDM

ports can be used to provide this function. Additional information about the serial interfaces is provided in the *MPC860 PowerQUICC User's Manual*.

The user must ensure that incoming cells are octet-aligned with the serial interface handshake or synchronization pulses. This ensures that the 860SAR applies the cell HEC delineation mechanism correctly and properly synchronizes with the incoming cell stream.

7.3.3.1 Serial Interface Registers

The serial interface SIMODE, SIGMR, and SICR registers should be programmed for the required interface standard, and the user must configure the serial interface RAM pointer (SIRP) as required for the desired system configuration.

Chapter 8
UTOPIA Interface

The 860SAR supports single- and multi-PHY ATM operations through an industry-standard UTOPIA interface. The sections below describe the signals provided for UTOPIA support, and signal timing for single- and multi-PHY ATM operations.

8.1 MPC860SAR UTOPIA Interface Signals

The 860SAR system bus signals are identical to the MPC860 signals described in the *MPC860 PowerQUICC User's Manual*. In addition to MPC860 signals, additional 860SAR signal functions were added to support the UTOPIA interface operations. Table 8-1 summarizes the signal functions provided by the 860SAR to support the UTOPIA interface. Table 8-2 provides the signal fucntions provided by the 850SAR to support the UTOPIA interface. The remainder of the 850SAR's signals are detailed in the *MPC850 PowerQUICC User's Manual*

Table 8-1. MPC860SAR Signal Functions

Signal Name	Signal Number	Description
PA[11] L1TXBD RXD3	G16	General-purpose I/O port A bit 11—Bit 11 of the general-purpose I/O port A. L1TXDB—The transmit data output signal for the serial interface time-division multiplex port B. L1TXDB has an open-drain capability. **RXD3**—Receive data input for SCC3.
PA[10] L1RXDB TXD3	J17	General-purpose I/O port A bit 10—Bit 10 of the general-purpose I/O port A. L1RXDB—The receive data input signal for the serial interface time-division multiplex port B. **TXD3**—Transmit data output signal for SCC3. TXD3 has an open-drain capability.
PA[9] L1TXDA RXD4	K18	General-purpose I/O port A bit 9—Bit 9 of the general-purpose I/O port A. L1TXDA—The transmit data output signal for the serial interface time-division multiplex port A. L1TXDA has an open-drain capability. **RXD4**—Receive data input for SCC4.
PA[8] L1RXDA TXD4	L17	General-purpose I/O port A bit 8—Bit 8 of the general-purpose I/O port A. L1RXDA—The receive data input signal for the serial interface time-division multiplex port A. **TXD4**—Transmit data output signal for SCC4. TXD4 has an open-drain capability.

Table 8-1. MPC860SAR Signal Functions (Continued)

Signal Name	Signal Number	Description
PB[21] SMTXD2 L1CLKOB PHSEL[1]	K16	General-purpose I/O port B bit 21—Bit 21 of the general-purpose I/O port B. SMTXD2—SMC2 transmit data input signal. L1CLKOB—Clock output from the serial interface TDM port B. PHSEL[1]—Least significant bit of PHY select bus (used in MPHY mode only).
PB[20] SMRXD2 L1CLKOA PHSEL[0]	L16	General-purpose I/O port B bit 20—Bit 20 of the general-purpose I/O port B. SMRXD2—SMC2 receive data input signal. L1CLKOA—Clock output from the serial interface TDM port A. PHSEL[0]—Most significant bit of PHY select bus (used in MPHY mode only).
PB[17] L1ST3 $\overline{\text{RTS3}}$ PHREQ[1]	P18	General-purpose I/O port B bit 17—Bit 17 of the general-purpose I/O port B. L1ST3—One of four output strobes generated by the serial interface. $\overline{\text{RTS3}}$—Request to send signal for SCC3. PHREQ[1]—Least significant bit of PHY request bus (used in MPHY mode only).
PB[16] L1ST4 $\overline{\text{RTS4}}$ PHREQ[0]	N16	General-purpose I/O port B bit 16—Bit 16 of the general-purpose I/O port B. L1ST4—One of four output strobes generated by the serial interface. $\overline{\text{RTS4}}$—Request to send signal for SCC4. PHREQ[0]—Most significant bit of PHY request bus (used in MPHY mode only).
PB[15] BRGO3 TxCav	R17	General-purpose I/O port B bit 15—Bit 15 of the general-purpose I/O port B. BRGO3— BRG3 output clock. TxCav—Transmit cell available input signal.
PC[15] $\overline{\text{DREQ0}}$ $\overline{\text{RTS1}}$ L1ST1 RxCav	D16	General-purpose I/O port C bit 15—Bit 15 of the general-purpose I/O port C. $\overline{\text{DREQ0}}$— IDMA channel 1 request input signal. $\overline{\text{RTS1}}$— Request to Send modem line for SCC1. L1ST1— One of four output strobes generated by the Serial Interface. RxCav—Receive cell available input signal
PC[13] $\overline{\text{L1RQB}}$ L1ST3 $\overline{\text{RTS3}}$	E18	General-Purpose I/O Port C Bit 13—Bit 13 of the general-purpose I/O port C. $\overline{\text{L1RQB}}$—The D-channel request signal for the serial interface time-division multiplex port B. L1ST3—One of four output strobes that can be generated by the serial interface. **$\overline{\text{RTS3}}$**—Request to send signal for SCC3.
PC[12] $\overline{\text{L1RQA}}$ L1ST4 $\overline{\text{RTS4}}$	F18	General-Purpose I/O Port C Bit 12—Bit 12 of the general-purpose I/O port C. $\overline{\text{L1RQA}}$—The D-channel request signal for the serial interface time-division multiplex port A. L1ST4—One of four output strobes that can be generated by the serial interface. **$\overline{\text{RTS4}}$**—Request to send signal for SCC4.
PD[15] L1TSYNCA UTPB[0]	U17	General-purpose I/O port D bit 15—Bit 15 of the general-purpose I/O port D. L1TSYNCA—Input transmit data sync signal to TDM channel A. UTPB[0]—UTOPIA bus bit 0 input/output signal.
PD[14] L1RSYNCA UTPB[1]	V19	General-purpose I/O port D bit 14—Bit 14 of the general-purpose I/O port D. L1RSYNCA—Input receive data sync signal to TDM channel A. UTPB[1]—UTOPIA bus bit 1 input/output signal.

Table 8-1. MPC860SAR Signal Functions (Continued)

Signal Name	Signal Number	Description
PD[13] L1TSYNCB UTPB[2]	V18	General-purpose I/O port D bit 13—Bit 13 of the general-purpose I/O port D. L1TSYNCB—Input transmit data sync signal to TDM channel B. UTPB[2]—UTOPIA bus bit 2 input/output signal.
PD[12] L1RSYNCB UTPB[3]	R16	General-purpose I/O port D bit 12—Bit 12 of the general-purpose I/O port D. L1RSYNCB—Input receive data sync signal to TDM channel B. UTPB[3]—UTOPIA bus bit 3 input/output signal.
PD[11] RXD3 $\overline{\text{RXENB}}$	T16	General-purpose I/O port D bit 11—Bit 11 of the general-purpose I/O port D. RXD3—Receive data for serial channel 3. $\overline{\text{RXENB}}$—Receive enable output signal.
PD[10] TXD3 $\overline{\text{TXENB}}$	W18	General-purpose I/O port D bit 10—Bit 10 of the general-purpose I/O port D. TXD3—Transmit data for serial channel 3. $\overline{\text{TXENB}}$—Transmit enable output signal.
PD[9] RXD4 UTPCLK	V17	General-purpose I/O port D bit 9—Bit 9 of the general-purpose I/O port D. RXD4—Receive data for serial channel 4. UTPCLK—UTOPIA Clock output signal.
PD[7] $\overline{\text{RTS3}}$ UTPB[4]	T15	General-purpose I/O port D bit 7—Bit 7 of the general-purpose I/O port D. $\overline{\text{RTS3}}$—Active low request to send output indicating that SCC3 is ready to transmit data. UTPB[4]—UTOPIA bus bit 4 input/output signal.
PD[6] $\overline{\text{RTS4}}$ UTPB[5]	V16	General-purpose I/O port D bit 6—Bit 6 of the general-purpose I/O port D. $\overline{\text{RTS4}}$—Active low request to send output indicating that SCC4 is ready to transmit data. UTPB[5]—UTOPIA bus bit 5 input/output signal.
PD[5] $\overline{\text{REJECT2}}$ UTPB[6]	U15	General-purpose I/O port D bit 5—Bit 5 of the general-purpose I/O port D. $\overline{\text{REJECT2}}$—Input signal to SCC2 indicating rejection the current ethernet frame after an external CAM determined the frame address did not match. UTPB[6]—UTOPIA bus bit 6 input/output signal.
PD[4] $\overline{\text{REJECT3}}$ UTPB[7]	U16	General-purpose I/O port D bit 4—Bit 4 of the general-purpose I/O port D. $\overline{\text{REJECT3}}$—Input signal to SCC3 indicating rejection the current ethernet frame after an external CAM determined the frame address did not match. This signal capability is not available when operating in UTOPIA mode. UTPB[7]—UTOPIA bus bit 7 input/output signal. (most significant bit of UTPB)
PD[3] $\overline{\text{REJECT4}}$ SOC	W16	General-purpose I/O port D bit 3—Bit 3 of the general-purpose I/O port D. $\overline{\text{REJECT4}}$—Input signal to SCC4 indicating rejection the current ethernet frame after an external CAM determined the frame address did not match. This signal capability is not available when operating in UTOPIA mode. SOC—Start of cell input/output signal.

Note: The signals with added capabilities in the 860SAR are shown in boldface. These signal capabilities are valid only in UTOPIA mode.

Table 8-2. MPC850SAR Signal Functions

Signal Name	Signal Number	Description
PB[22] SMSYN2 SDACK2 PHYSEL[1]	R9	General-Purpose I/O Port B Bit 22—Bit 22 of the general-purpose I/O port B. SMSYN2—SMC2 external sync input. SDACK2—SDMA acknowledge 2 output that is used as a peripheral interface signal for IDMA emulation. PHSEL[1]—lsb of the PHY select bus (MPHY mode only).
PB[19] L1ST1 PHYSEL[0]	R7	General-Purpose I/O Port B Bit 19—Bit 19 of the general-purpose I/O port B. L1ST1—One of eight output strobes that can be generated by the serial interface. PHSEL[0]—msb of the PHY select bus (MPHY mode only).
PB[17] L1ST3 PHYREQ[1]	N7	General-Purpose I/O Port B Bit 17—Bit 17 of the general-purpose I/O port B. L1ST3—One of eight output strobes that can be generated by the serial interface. PHREQ[1]—lsb of the PHY request bus (MPHY mode only).
PB[16] L1RQa L1ST4 PHYREQ[0]	R5	General-Purpose I/O Port B Bit 16—Bit 16 of the general-purpose I/O port B. L1RQa—D-channel request signal for serial interface TDMa. L1ST4—One of eight output strobes that can be generated by the serial interface. PHREQ[0]—msb of the PHY request bus (MPHY mode only).
PC[15] DREQ0 L1ST5 RXCAV	R16	General-Purpose I/O Port C Bit 15—Bit 15 of the general-purpose I/O port C. DREQ0—IDMA channel 1request input. L1ST5—One of eight output strobes that can be generated by the serial interface. RXCAV—MPC850SAR's receive cell available input signal.
PC[12] L1RQa L1ST8 TXCAV	T13	General-Purpose I/O Port C Bit 12—Bit 12 of the general-purpose I/O port C. L1RQa—D-channel request signal for serial interface TDMa. L1ST8—One of eight output strobes that can be generated by the serial interface. TXCAV—MPC850SAR's transmit cell available input signal.
PD[15] UTPB[0]	R4	General-Purpose I/O Port D Bit 15—Bit 15 of the general-purpose I/O port D. UTPB[0]—UTOPIA bus bit 0 input/output signal.
PD[14] UTPB[1]	T3	General-Purpose I/O Port D Bit 14—Bit 14 of the general-purpose I/O port D. UTPB[1]—UTOPIA bus bit 1 input/output signal.
PD[13] UTPB[2]	P5	General-Purpose I/O Port D Bit 13—Bit 13 of the general-purpose I/O port D. UTPB[2]—UTOPIA bus bit 2 input/output signal.
PD[12] UTPB[3]	R3	General-Purpose I/O Port D Bit 12—Bit 12 of the general-purpose I/O port D. UTPB[3]—UTOPIA bus bit 3 input/output signal.
PD[11] RXENB	N5	General-Purpose I/O Port D Bit 11—Bit 11 of the general-purpose I/O port D. RXENB—Receive enable output signal.
PD[10] TXENB	T2	General-Purpose I/O Port D Bit 10—Bit 10 of the general-purpose I/O port D. TXENB—Transmit enable output signal.
PD[9] UTPCLK	P4	General-Purpose I/O Port D Bit 9—Bit 9 of the general-purpose I/O port D. UTPCLK—UTOPIA clock output signal.
PD[7] UTPB[4]	R2	General-Purpose I/O Port D Bit 7—Bit 7 of the general-purpose I/O port D. UTPB[4]—UTOPIA bus bit 4 input/output signal.

Table 8-2. MPC850SAR Signal Functions (Continued)

Signal Name	Signal Number	Description
PD[6] UTPB[5]	R1	General-Purpose I/O Port D Bit 6—Bit 6 of the general-purpose I/O port D. UTPB[5]—UTOPIA bus bit 5 input/output signal.
PD[5] UTPB[6]	P2	General-Purpose I/O Port D Bit 5—Bit 5 of the general-purpose I/O port D. UTPB[6]—UTOPIA bus bit 6 input/output signal.
PD[4] UTPB[7]	P3	General-Purpose I/O Port D Bit 4—Bit 4 of the general-purpose I/O port D. UTPB[7]—UTOPIA bus bit 7 input/output signal (most significant bit of UTPB).
PD[3] SOC	N4	General-purpose I/O Port D Bit 3—Bit 3 of the general-purpose I/O port D. SOC—Start of cell input/output signal.

8.2 UTOPIA Single-PHY

The 860SAR acts as an ATM layer UTOPIA master per the ATM Forum UTOPIA level 1 specification for an ATM single-PHY configuration. The 860SAR implements the UTOPIA interface as an 8-bit wide bidirectional data bus using a cell-level handshake, and operates at frequencies up to 25 MHz. The UTOPIA controller controls all interface signals.

Assertion of transmit cell available (TxCav) or receive cell available (RxCav) issues a request to the CP to handle a receive or transmit operation. During the cell transfer, the UTOPIA controller controls the enable signals ($\overline{\text{TxEnb}}$ or $\overline{\text{RxEnb}}$) and the transmit start of cell signal (TxSOC). It also samples the RxSOC signal during the cell transfer.

Most of the UTOPIA signals are multiplexed on 860SAR port D pins as shown in Figure 8-1. The IDMA request connected to the DREQ0 signal is replaced with RxCav. TxCav signal is connected to the port B[15] signal.

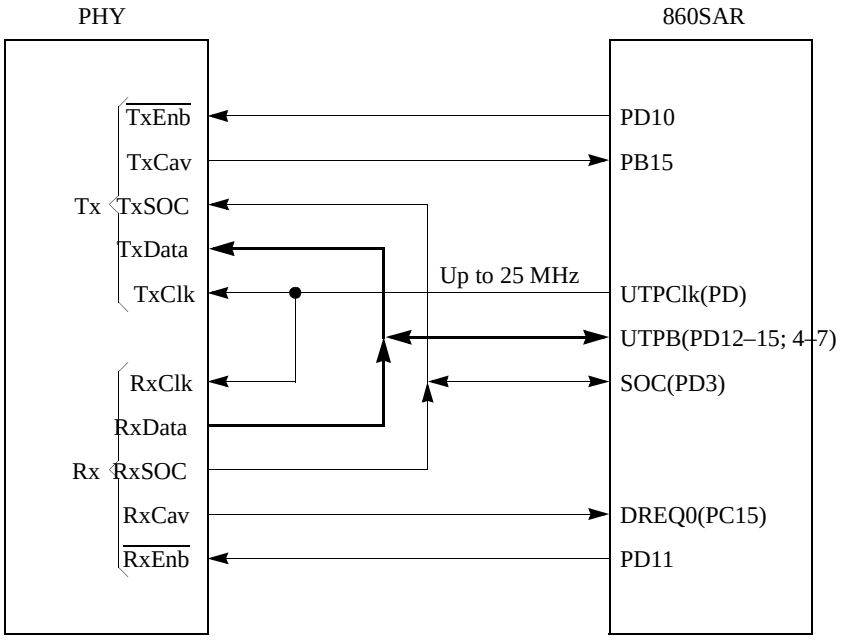


Figure 8-1. MPC860SAR UTOPIA Interface

The 860SAR implements a cell level interface. The cell level handshake is identical to the octet level handshake except that once the TxCav or RxCav signals are asserted the PHY must be capable of receiving or transmitting a whole cell. The 860SAR transmits or receives a whole cell directly to or from system memory during a receive or transmit operation.

8.2.1 Receive Cell Transfer Operation

Assertion of RxCav generates a request to receive a cell transfer. The 860SAR UTOPIA provides the cell level handshake, and as soon as RxCav is asserted, the PHY must be able to transfer a whole cell upon $\overline{\text{RxEnb}}$. The 860SAR's UTOPIA controller divides the cell

transfers into 1 to 4 byte groups and uses $\overline{\text{RxEnb}}$ to control the transfer. For example, a 53-byte cell transfer sequence is divided into the following UTOPIA transfers:

- Header transfer (4 octets)
- UDF (HEC) transfer (1 octet)
- 12 cell body transfers (12 x 4 octets)

The 860SAR asserts $\overline{\text{RxEnb}}$ for each transfer. The following cycle the 860SAR starts sampling the UTOPIA bus (through the UTPB signals) and RxSOC. During the UDF tenure only one octet is transferred; all other sections are four octets long.

The receive start of cell timing sequence is shown in Figure 8-2. The circles shown during the data tenure represent the sampling points of the 860SAR. Note that RxCav is not sampled during the transfer.

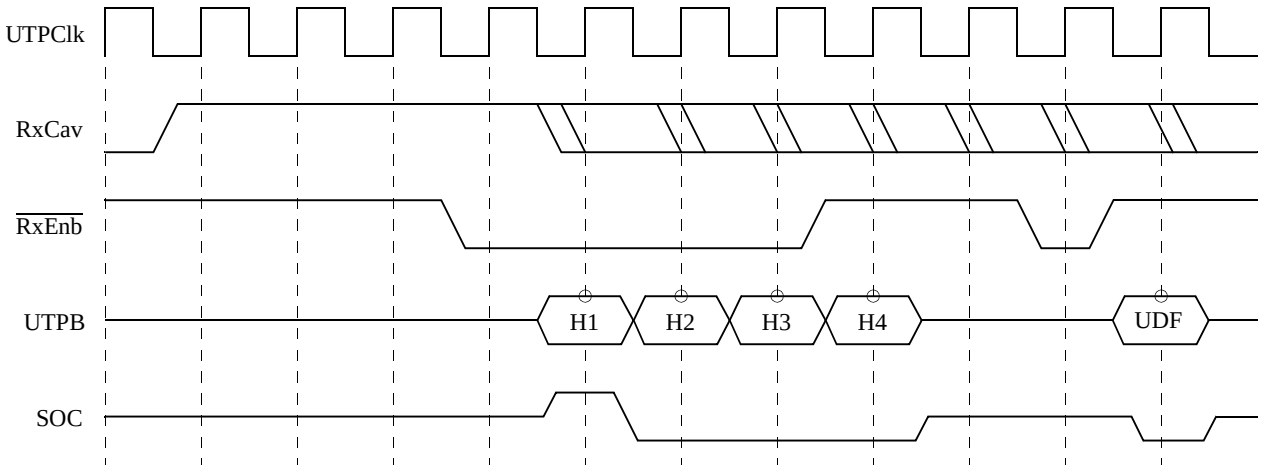


Figure 8-2. UTOPIA Receiver Start of Cell

The end-of-cell transfer timing sequence is shown in Figure 8-3. In this example the PHY was not ready with additional data and therefore deasserted RxCav. A few clocks later the PHY asserted RxCav again to indicate that data was available. If the PHY is ready to send additional data at the end of the current data tenure, the PHY can assert RxCav at any time during the data transfer and hold RxCav asserted until the first transfer the following data tenure.

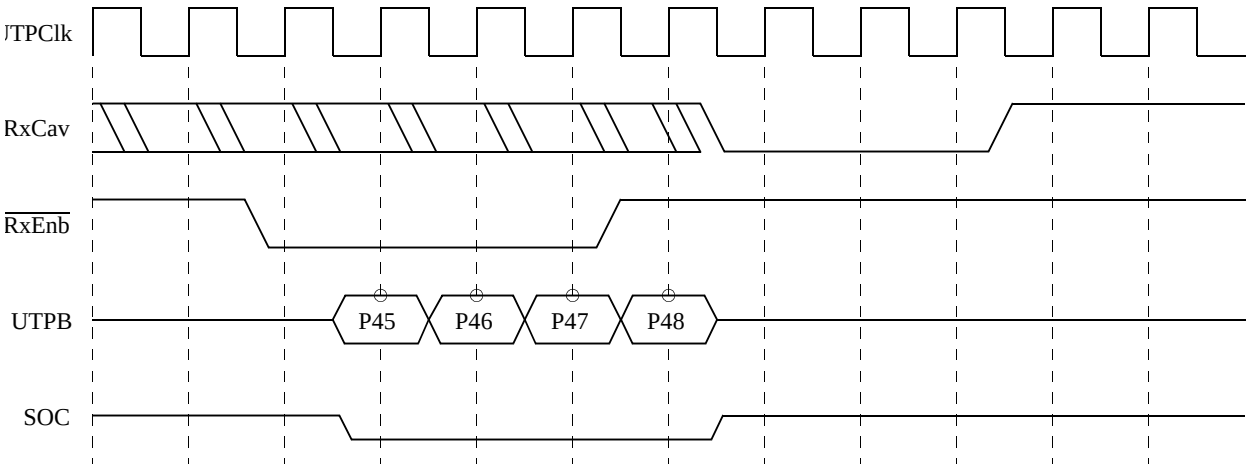


Figure 8-3. UTOPIA Receiver End of Cell

8.2.2 Transmit Cell Transfer Operation

Assertion of the TxCav signal generates a request for a cell to transmit. The 860SAR's UTOPIA interface implements the cell level handshake, and the PHY must be able to receive a whole cell upon assertion of the $\overline{\text{TxEnb}}$ signal. Note that a RxCav signal assertion generates a request that has higher priority than those caused by the assertion of the TxCav signal; transmit cell requests are granted by the CP when it has completed all the cell receive requests. The 860SAR's UTOPIA controller divides the cell transfers into 1- to 4-byte groups and uses the $\overline{\text{TxEnb}}$ signal to control the transfer. For example, a 53-byte cell transfer sequence is divided into the following UTOPIA transfers:

- Header transfer (4 octets)
- UDF (HEC) transfer (1 octet)
- Cell payload transfers (total of 48 octets)

The 860SAR asserts $\overline{\text{TxEnb}}$, TxSOC, and TxPrty signals, and drives the UTOPIA bus (through the UTPB signals) with data for each transfer. The cell header is transferred in a 4-octet group. The UDF is transferred as a single octet. The cell payload is transferred in groups of 1 to 4 octets. The UDF (HEC) is not generated by the 860SAR; during the UDF transfer, the UTPB signals will be driven with 0x00.

8.2.2.1 UTOPIA Bus and SOC Drive

The UTOPIA bus (through the UTPB signals) and SOC signal are driven by the 860SAR only when $\overline{\text{TxEnb}}$ is asserted during transmit transfers; UTPB and SOC are three-stated when $\overline{\text{TxEnb}}$ is not asserted.

The transmit start-of-cell sequence is shown in Figure 8-4. Note that the TxCav signal is not sampled during the cell transfer.

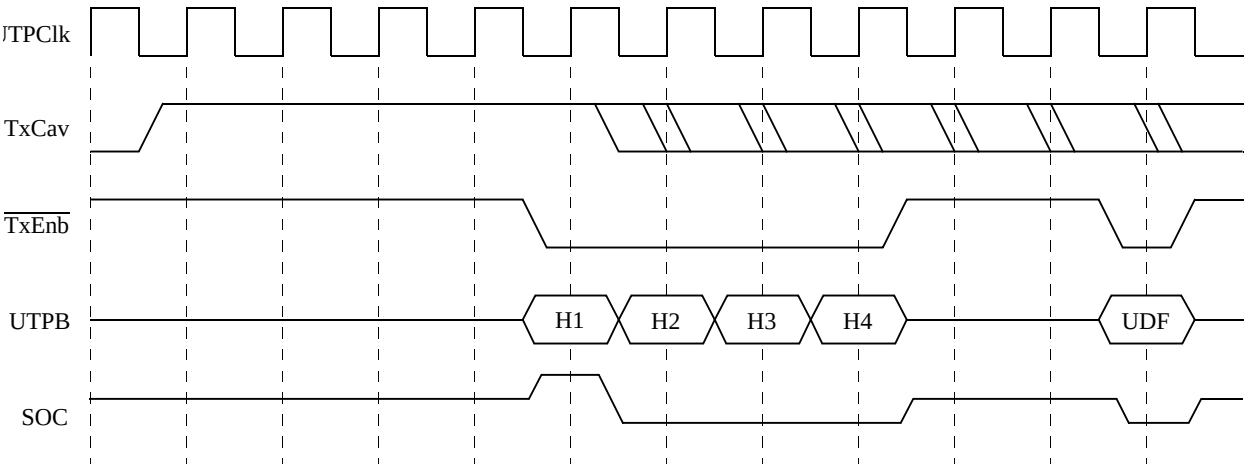


Figure 8-4. UTOPIA Transmitter Start of Cell

The transmit end-of-cell sequence is shown in Figure 8-5. In this example the PHY is ready for the next cell transfer and has asserted TxCav immediately at the end of the cell transfer. The TxCav signal should be kept asserted until the TxEnb signal is asserted by the 860SAR to indicate the transfer start of a new cell.

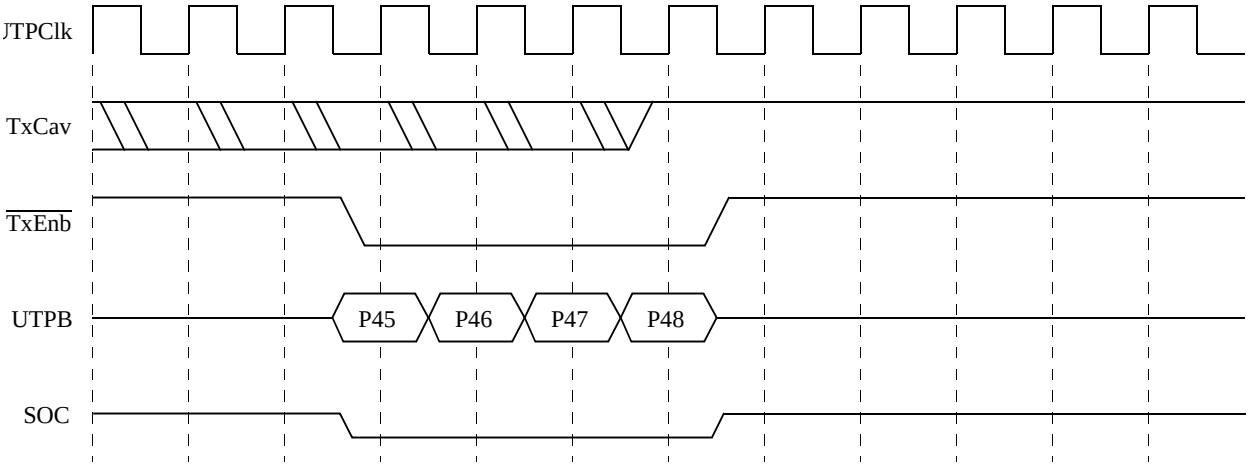


Figure 8-5. UTOPIA Transmitter End of Cell

8.3 UTOPIA Multi-PHY Operations

The 860SAR supports a multi-PHY interface through the use of PHY addressing signals. The following are guidelines for Multi-PHY operation:

- Up to 4 PHYS may be supported.
- Supports using additional PHY addressing signals - PHREQ and PHSEL.

- PHREQ indicates the receive requesting (available) PHY (i.e., PHREQ identifies the PHY requesting that the 860SAR receive its data). PHSEL is used to select the PHY that is to receive or transmit data.
- For the transmit side, Upon TxCav the 860SAR may chose to deliver the next cell to any of the available PHYs. Therefore, TxCav should be asserted only when **all** the PHYs are available.
- If additional port B pins are used as a general purpose output pins, a dedicated semaphore (PBF) should be used to prevent collision between Host and CP writes. (see PBF bit in STSTATE parameter ram field).
- PHSEL and PHREQ timing is with reference to the system clock.

8.3.1 Setting up PHSEL and PHREQ Pins

To drive a MPHY address, PHREQ (driven through the PB16 and PB17 signals) and PHSEL (driven through the PB20 and PB21signals) must be set by the user to be general purpose signals. PHREQ should be programmed as input signals and PHSEL programmed as output signals through the associated bits in the PBPAR and PBDIR registers. Both PHSEL and PHREQ are read or written directly through port B synchronously with the system clock; refer to the *MPC860 PowerQUICC User's Manual* for additional information about system clocking and port read and write operations.

Program PBPAR pins PB16, PB17, PB20 and PB21 to zero, that is, as general purpose I/O pins. Then program PBDIR pins PB16 and PB17 to zero (as inputs) and PBDIR pins PB20 and PB21 to one (as outputs). PB16 and PB17 will be used for PHREQ where PB16 is the most significant bit, PB20 and PB21 will be used for PHSEL where PB20 is the most significant bit.

NOTE: The 850SAR UTOPIA MPHY operations require the use the port B PHREQ[0–1] and PHSEL[0–1] signals. These signals are configured by clearing PBPAR[16–17], PBPAR[19] and PBPAR[22] and PBDIR[16–17], and setting PBDIR[19] and PBDIR[22].

8.3.2 Receive Cell Transfer Operation

The multi-PHY UTOPIA cell transfer protocol is basically the same as that used for single-PHY transfers, except that prior to the assertion of $\overline{\text{RxEnb}}$ the 860SAR reads the PHY address through PHREQ. The PHY address is then written to PHSEL for use during the address match process.

The 860SAR RxCav input pin may be asserted together with a valid PHY number on the PHSEL pins. The assertion of RxCav will generate a request to the CP. As soon as the request is accepted by the CP (after at least several UTOPIA clocks) PHREQ will be read by the CP. If PBF bit is 0, the 860SAR will write the selected PHY# to the PHSEL pins and only after several UTOPIA clocks the RxEnb will be asserted and cell reception will start. If PBF is set, the CP will keep reading PHREQ, waiting for PBF to be cleared by the HOST

(see PBF bit in STSTATE parameter ram field).

PHREQ must remain valid from the assertion of RxCav until $\overline{\text{RxEnb}}$ is asserted. PHSEL is driven by the 860SAR, and remains valid from the cycle the 860SAR has selected a PHY until the end of the cell transfer through the UTOPIA interface, as shown in Figure 8-7.

Note: During RxCav assertion, PHSEL still may be changed dynamically if a higher priority PHY asserted its cell available pin. The 860SAR PHSEL will be sampled at the rising edge of the system clock.

8.3.3 Transmit Cell Transfer Operation

When transmitting, the 860SAR writes the PHY address to PHSEL to select the currently addressed PHY prior to the assertion of $\overline{\text{TxEnb}}$. The 860SAR TxCav input pin may be asserted only when all the PHYs are ready to accept a cell. The assertion of TxCav will generate a request to the CP. As soon as the request is accepted by the CP, PHSEL will be updated to select the current PHY and only after several UTOPIA clocks the $\overline{\text{TxEnb}}$ will be asserted and cell transfer will start.

Note that requiring TxCav to be asserted only when all PHYs are ready to receive a cell does not mean that the transmission rate is governed by the slowest PHY. The scheduler (APC using PHY programmed transmission rate) will place more cells in the transmit queue for faster PHYs. You can think of the transfers and subsequent assertions of TxCav by the PHYs as instantaneous because the UTOPIA interaface transfer is faster compared to the line rate and the use of cell FIFOs by the PHYs. If any of the PHYs malfunction (die) all transmission of cells is halted since TxCav won't be asserted. External logic is needed to detected and correct this condition and deactivation of the impacted channels should be carried out by the 860SAR application software.

PHSEL is driven by the 860SAR, and remains valid from the cycle the 860SAR has selected a PHY until the end of the cell transfer through the UTOPIA interface, as shown in Figure 8-8.

8.3.4 Example MPHY Implementation

Figure 8-6 is an overview example for implementing a Multi PHY system using the 860SAR. The TxCav will be asserted when all PHYS are ready to accept a cell. PhSel decode is used to select the PHY several clocks before TxEnb or RxEnb are asserted. The priority mux (Priority encode) is a "box" which prioritizes among the PHYs in the Rx direction. RxCav should be asserted when at least one of the PHYs is ready to deliver a cell.

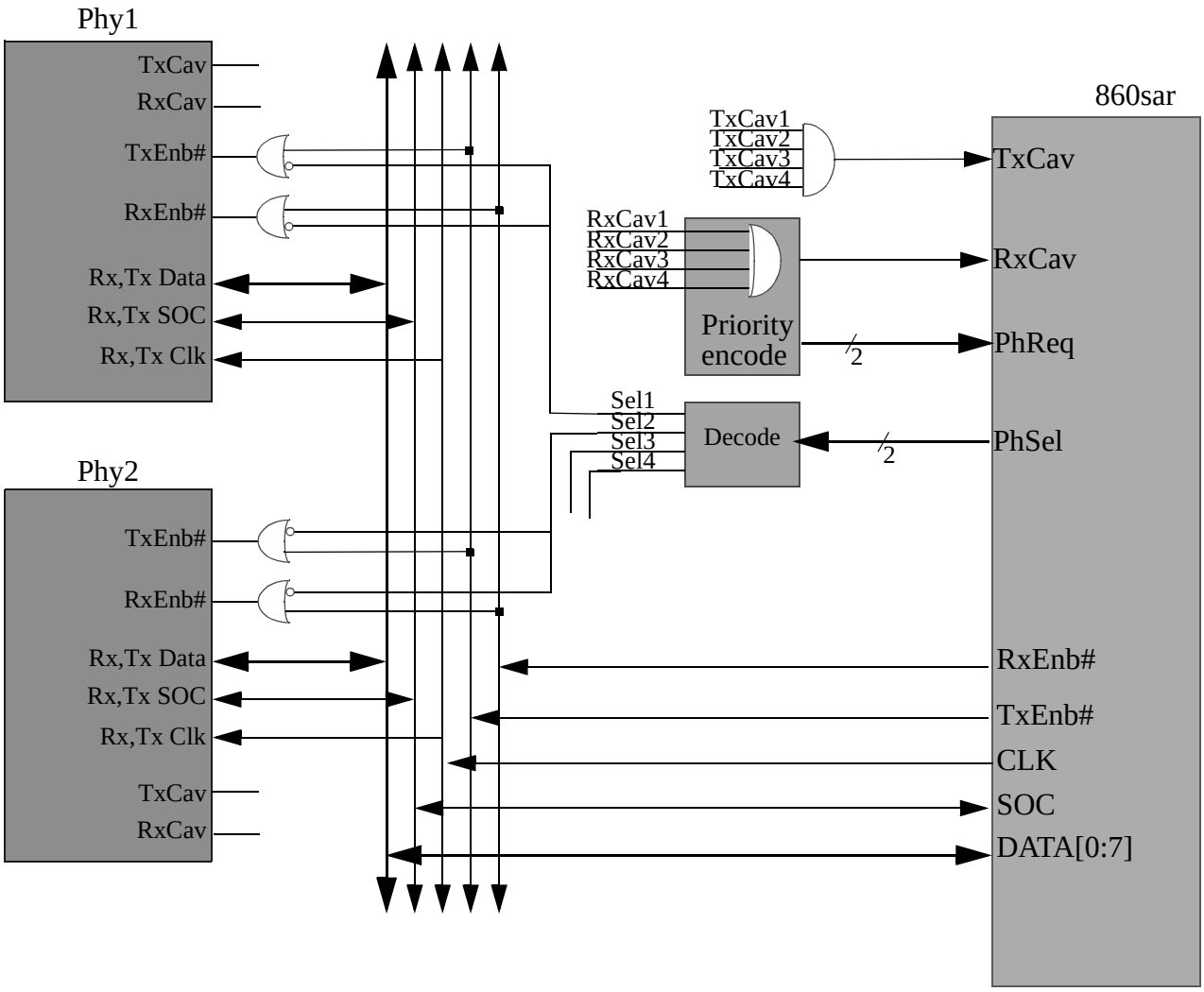


Figure 8-6. Multi-PHY Implementation Example

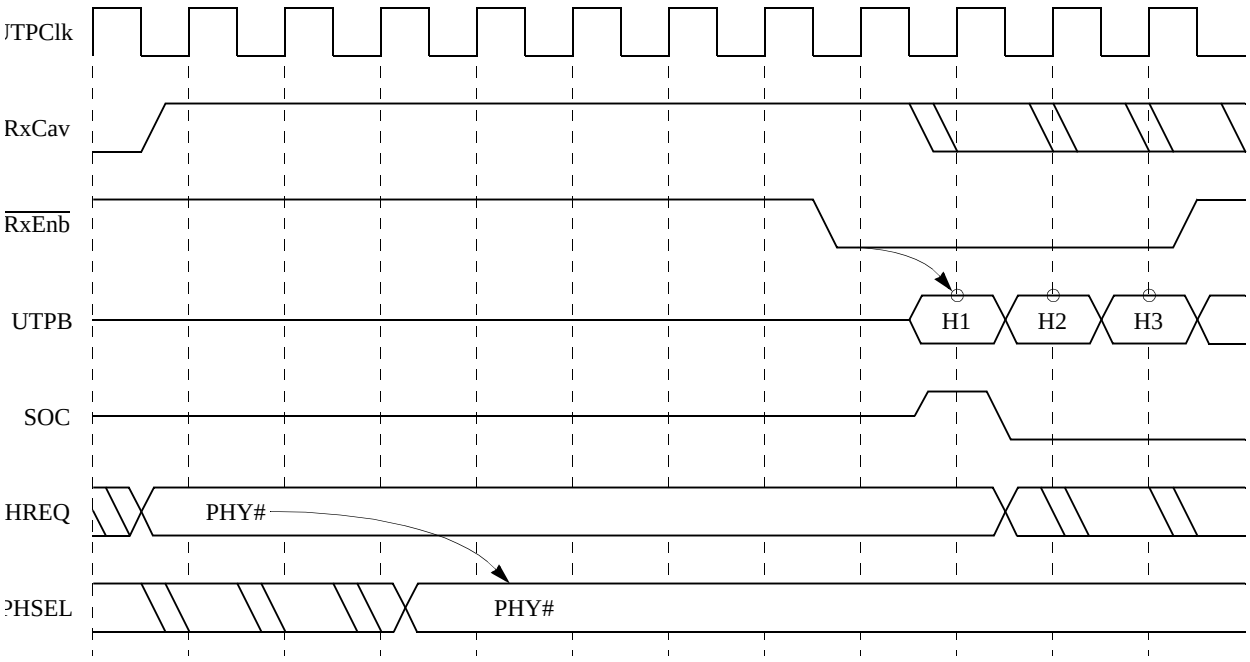


Figure 8-7. UTOPIA Receiver Multi-PHY Example

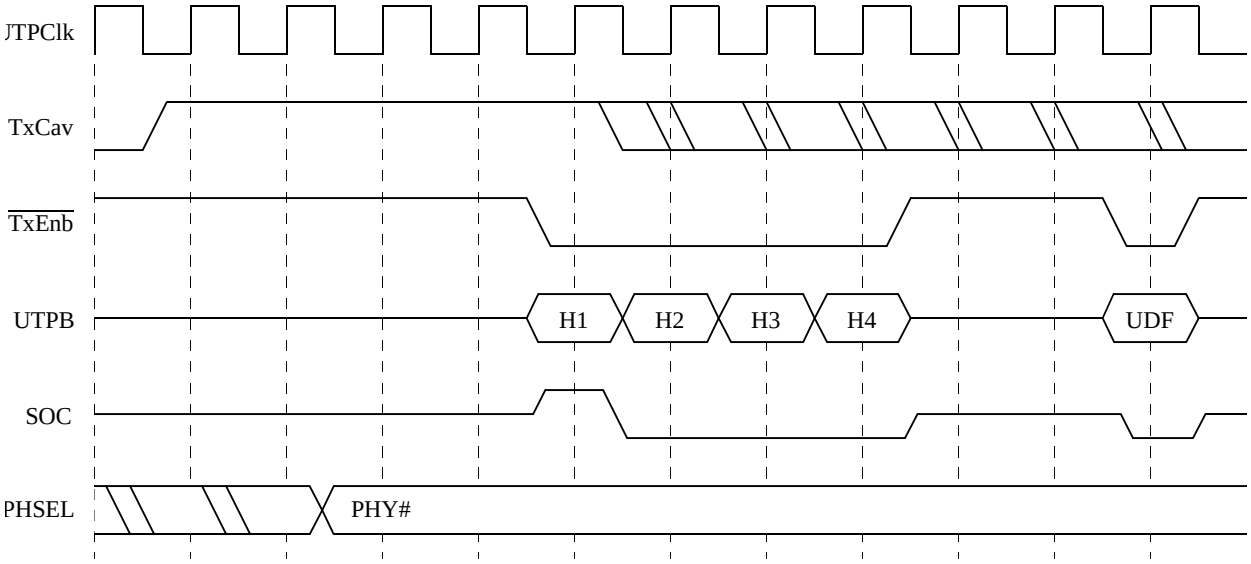


Figure 8-8. UTOPIA Transmitter Multi-PHY Example

8.4 UTOPIA Interface Transfer Timing

Table 8-3 describes the UTOPIA interface timing for data transfers and receive and

transmit transitions.

Table 8-3. UTOPIA Interface Transfer Timing

UTOPIA Transfer Type	Clock Ratio	Transition Time
Interval between $\overline{\text{RxEnb}}$ negation and $\overline{\text{RxEnb}}$ assertion, or $\overline{\text{TxEnb}}$ negation and $\overline{\text{TxEnb}}$ assertion for successive data blocks (payload bytes 5-8 and 9-12).	UTPCLK/SYSCLK = 1	8 UTPCLKs minimum
	UTPCLK/SYSCLK = 1/2	4 UTPCLKs minimum
	1/3 < UTPCLK/SYSCLK < 1/5	0-3 UTPCLKs minimum
Interval between $\overline{\text{RxEnb}}$ negation and $\overline{\text{TxEnb}}$ assertion.	—	50 SYSCLKs minimum
Interval between $\overline{\text{TxEnb}}$ negation and $\overline{\text{RxEnb}}$ assertion.	—	20 SYSCLKs minimum
Interval between $\overline{\text{RxEnb}}$ negation and subsequent $\overline{\text{RxEnb}}$ assertion for header transfers.	—	6 SYSCLKs minimum
Interval between $\overline{\text{TxEnb}}$ negation and subsequent $\overline{\text{TxEnb}}$ assertion for header transfers.	—	4 SYSCLKs minimum

8.5 UTOPIA AC Electrical Specifications

Table 8-4 below shows the AC electrical specifications for the UTOPIA interface.

Table 8-4. UTOPIA AC Electrical Specifications

Num	Signal Characteristic	25 MHz		Up to 66 MHz		Unit
		Min	Max	Min	Max	
1	UtpClk rise/fall time	—	3.5	—	3.5	ns
2	$\overline{\text{RxEnb}}$ and $\overline{\text{TxEnb}}$ active delay	- 5	7	- 5	7	ns
3	UTPB, SOC setup time	8	—	8	—	ns
4	UTPB, SOC hold time	1	—	1	—	ns
5	UTPB, SOC active delay	- 5	7	- 5	7	ns

NOTE:

1. The TxCav and RxCav signals are asynchronous, and are recognized by the 860SAR within two clock cycles.

2. The PhReq and PhSel signals are asynchronous. PhReq should be valid 1 clock time after RxCav assertion. Phsel must be asserted at least 1 clock before $\overline{\text{RxEnb}}$ or $\overline{\text{TxEnb}}$ assertion.

Figure 8-9 below shows signal timing during UTOPIA receive operations. **NOTE:** All timing is relative to 1/2 (50 %) VCC transition points.

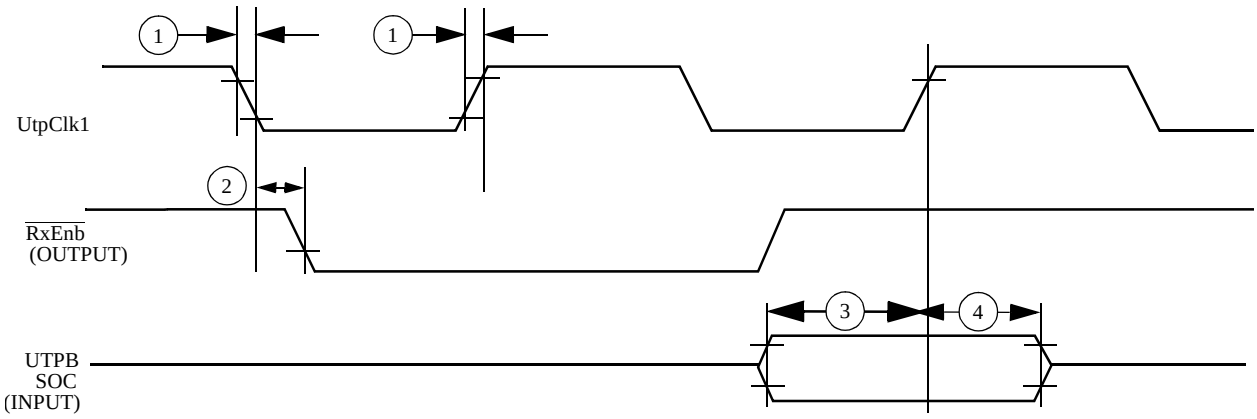


Figure 8-9. UTOPIA Receive Timing

Figure 8-10 below shows signal timing during UTOPIA transmit operations. **NOTE:** All timing is relative to 1/2 (50 %) VCC transition points.

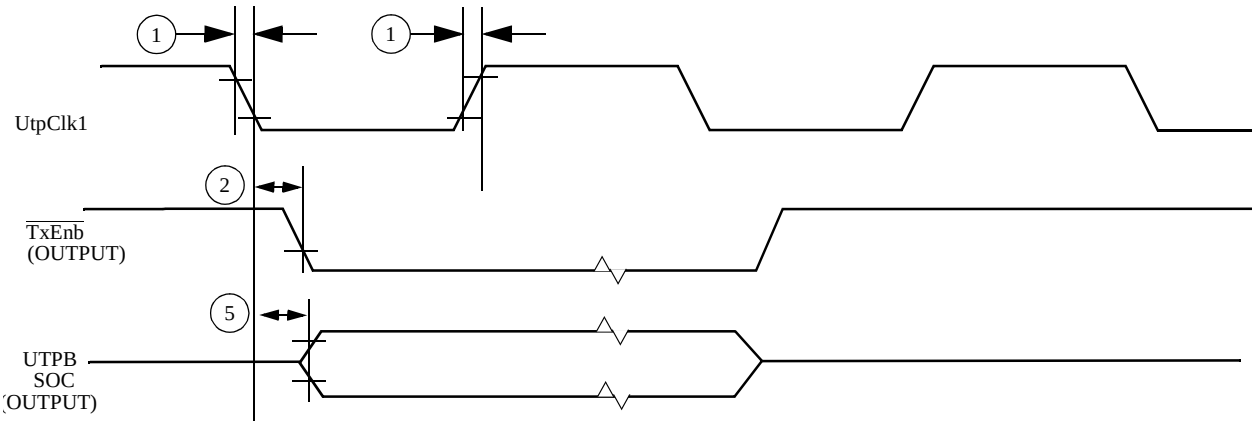


Figure 8-10. UTOPIA Transmit Timing

Appendix A
Performance

This appendix provides receiver and transmitter performance information for the 860SAR.

A.1 Receiver

Table A-1 shows the UTOPIA and serial mode receiver performance of the 860SAR when configured with internal and external connection tables.

Table A-1. Receiver Performance (with 50MHz System Clock)

Mode	Condition	Mbit	
		UTOPIA	Serial (3)
Internal connection tables	AAL5, large frame(4), lookup table (1)	67 Mbps	27/19 Mbps
	AAL0, lookup table (1)	50 Mbps	24/17.5 Mbps
External connection tables	AAL5, large frame(4), Address compression	56 Mbps	23/18 Mbps
	AAL0, Address compression	44 Mbps	21/17 Mbps
	AAL5, large frame(4), CAM(2)	60 Mbps	27/19 Mbps
	AAL0, CAM(2)	47 Mbps	24/17.5 Mbps
External AAL5 + MPHY	AAL5, large frame(4), Address compression	52 Mbps	N/A

Notes:

1. Cell header located in the middle of the lookup table (16th place)
2. Expected
3. No scrambler / With Scrambler and coset
4. ‘Large frame’ implies an average frame size of approximately 200 bytes. As the size of the AAL5 frames decrease, the AAL5 channels will approach the AAL0 performance.

A.2 Transmitter

Table A-2 shows the UTOPIA and serial mode transmitter performance of the 860SAR when configured with internal and external connection tables.

Table A-2. Transmitter (Including 1 Priority APC) Performance (with 50MHz System Clock)

Mode	Condition	Mbit	
		UTOPIA(4)	Serial(5)
Internal connection tables	AAL5, large frame(6) + APC	53/56 Mbps	32/23 Mbps
	AAL0 +APC	45/48 Mbps	28/20.5 Mbps
External connection tables	AAL5, large frame(6) + APC	48/51 Mbps	27/20 Mbps
	AAL0 + APC	39/42 Mbps	24/19 Mbps
External AAL5 + MPHY	2 MPHYs with similar bit rate	44/48 Mbps	N/A
	1 fast MPHY and 1 slow (1)	43 Mbps	N/A
	1 fast MPHY and 1 slow (2)	41 Mbps	N/A
	1 fast MPHY and 3 slow (3)	38 Mbps	N/A

Notes:

1. In case of one 25 Mbps PHY and 1 XDSL 1 Mbps. This example is for NCITS = 4 for the first PHY and NCITS = 0.16 for the second.
2. In case of one 25 Mbps PHY and 1 XDSL 1/2 Mbps. This example is for NCITS = 1 for the first PHY and NCITS = 0.02 for the second.
3. In case of one 25 Mbps PHY and 3 XDSL 1/2 Mbps. This example is for NCITS = 1 for the first PHY and NCITS = 0.02 for the second.
4. APC(NCITS = 1)/APC(NCITS = 4)
5. No scrambler/with scrambler and coset
6. ‘Large frame’ implies an average frame size of approximately 200 bytes. As the size of the AAL5 frames decrease, the AAL5 channels will approach the AAL0 performance.

The performance information provided is based on the following assumptions:

- AAL5—Buffer (data) size > 1/5Kbyte
- AAL0—Interrupt per BD. No CRC10 generation
- System memory is DRAM with 5-2-2-2 performance at 50MHz
- Average load on external bus

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