MPC850SARDB

Revision ENG

User's Manual

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ISSUE 1- Release 0.1

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1 - General Information

1•1 Introduction

This document is the operation guide for the MPC8XXFADS Daughter Board for the MPC850 - named the MPC850SARDB.

The daughter board holds the evaluated MPC850SAR along with some necessary logic, which is required to be in the nearest vicinity of the MPC850SAR as well as peripherals, that are dedicated to the MPC850SAR and are not required for any other member of the MPC8XX family.

The daughter board has 2 sets of matching connectors - one on the print[A] side and one on the component[B] side. Those on the print side connect to a matching set found on the MPC8XXFADS while those on the component side, are to serve hardware expansion via a dedicated adaptor.

In addition, a set of logic analyzer connector is featured, matching the new high density HP16500 logic analyzer adaptors, in order to provide fast connection to logic analyzer while saving on board's space and reducing EMI.

1•2 Abbreviations' List

- FADS[C] - the MPC8XXFADS, to which this board connects.
- UPM - User Programmable Machine
- GPCM - General Purpose Chip-select Machine
- GPL - General Purpose Line (associated with the UPM)
- I/R - Infra-Red
- DB, D/B or 850SARDB - the MPC850SARDB, the subject of this document.
- M/B - MPC8xxFADS Mother Board.
- BSCR - Board Control & Status Register.
- ZIF - Zero Input Force
- BGA - Ball Grid Array
- Spec - engineering Specification Document.
- MPC850 - Refers to either MPC850 or MPC850SAR.
- SAR-PHY - Refers to the ATM/E1/T1 Tool board made for the MPC860/850SAR.

1•3 Related Documentation

- MPC850 User's Manual.
- ADI Board Specification.
- MPC8XXFADS Engineering Specification
- PHILIPS's PDIUSBP11 Data Sheet. May be obtained from http://www.semiconductors.philips.com/acrobat/4417.pdf

A. Board's bottom.
B. Board's top.
C. Not to be mistaken for the M683XX Family Ads

1•4 SPECIFICATIONS

The MPC850SARDB specifications are given in TABLE 1-1.

TABLE 1-1. MPC850SARDB Specifications

CHARACTERISTICS	*SPECIFICATIONS*
Microprocessor	MPC850SAR @ 50 MHz
Addressing Total address range:	 4 GBytes Internal 64 MByte External[a]
Operating temperature	0°C - 30°C
Storage temperature	-25°C to 85°C
Relative humidity	5% to 90% (non-condensing)
Dimensions: Length Width Thickness	 5.87" (149 mm) 4.37" (111 mm) 0.063" (1.6 mm)

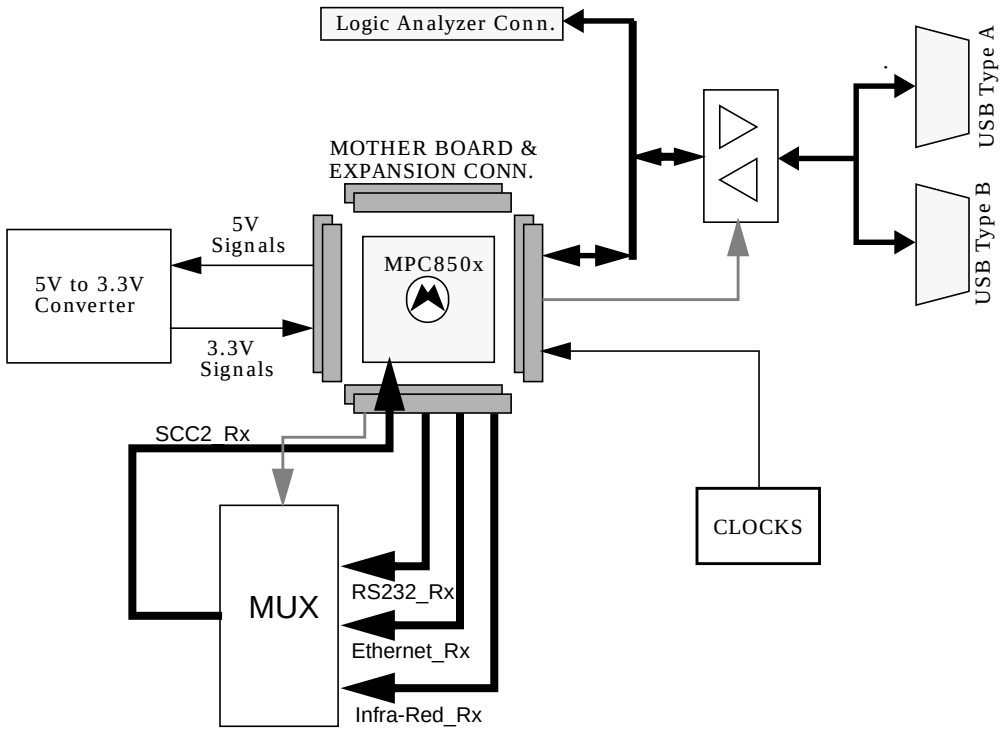
a. This is the maximum contiguous block of memory that may be accessed. It may reside however, anywhere within the 4 GBytes of addressing space.

1•5 MPC850SARDB Features

- ❏ MPC850 running upto 50 MHz
- ❏ USB Port with shutdown option - BCSR controlled. Support for both type A and Type B USB connectors.
- ❏ USB Port Speed control, BCSR driven.
- ❏ 5V supply for USB port, BCSR controlled.
- ❏ Selectable KAPWR source: 3.3V or externally supplied
- ❏ Selectable clock source: 32768Hz crystal resonator or 4[A] MHz Clock generator.
- ❏ On-Board Expansion connectors, including all MPC pins and MPC8XXFADS control / status signals.
- ❏ On-Board High Density Logic Analyzer connectors, supporting fast connection to HP 16500 logic analyzer.
- ❏ SAR-PHY Tool Support.

A. May be easily changed to any 3.3V powered oscillator oscillating in 3 - 5 MHz frequency range.

FIGURE 1-1 MPC850SARDB Block Diagram



1•6 MPC850SARDB Rev. ENG to MPC850FADSDB Rev. PILOT Changes

Changes were made to support the SAR-PHY tool board on P8 on the MPC8xxFADS board. Due to these changes, the DB no longer supports any other tool which was previously used with earlier revisions. This is due to re-routing of the I/O signals on the DB.

2 - Hardware Preparation and Installation

2•1 INTRODUCTION

This chapter provides unpacking instructions, hardware preparation, and installation instructions for the MPC850SARDB.

2•2 UNPACKING INSTRUCTIONS

NOTE

If the shipping carton is damaged upon receipt, request carrier's agent to be present during unpacking and inspection of equipment.

Unpack equipment from shipping carton. Refer to packing list and verify that all items are present. Save packing material for storing and reshipping of equipment.

CAUTION

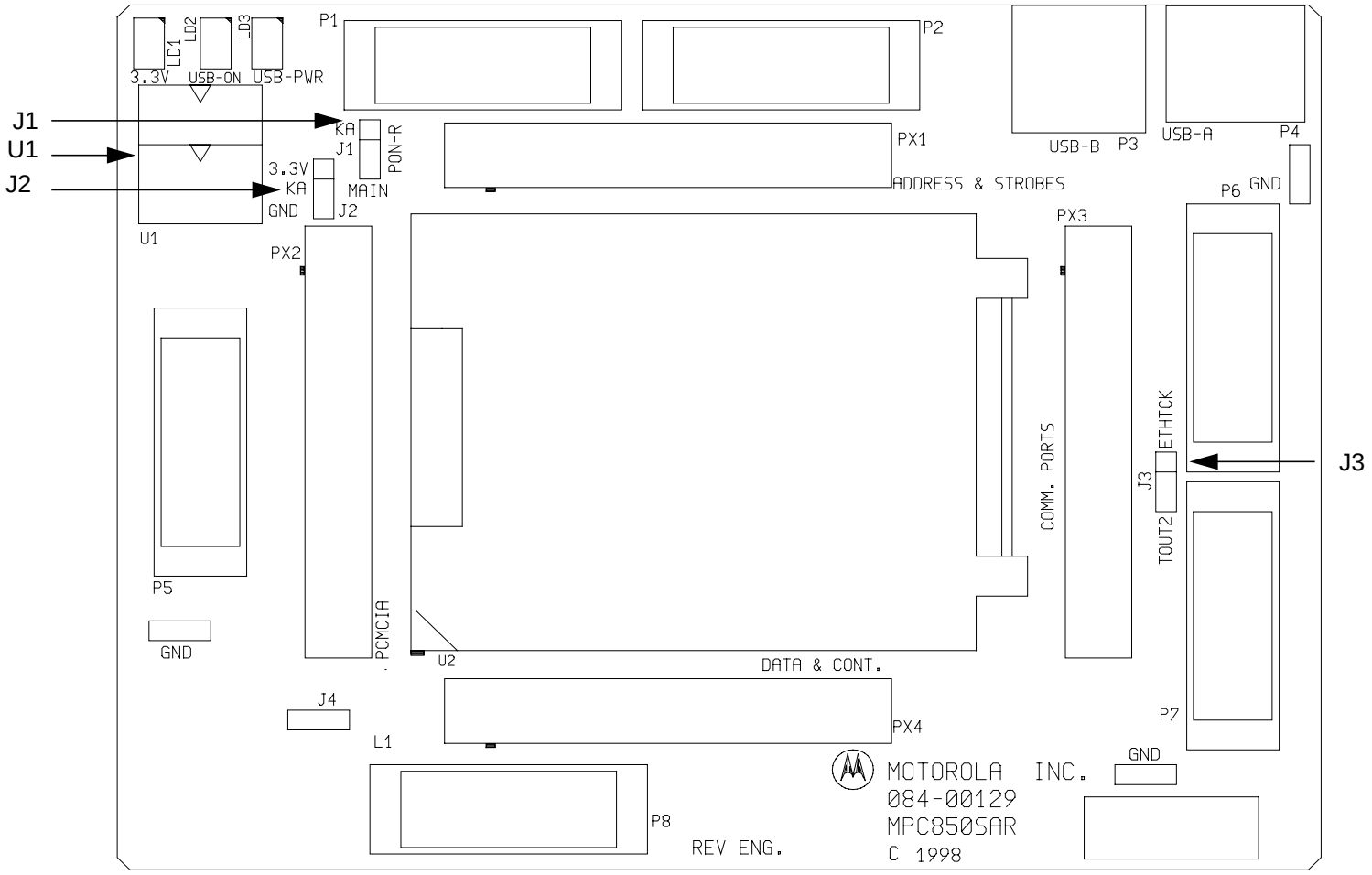
AVOID TOUCHING AREAS OF INTEGRATED CIRCUITRY; STATIC DISCHARGE CAN DAMAGE CIRCUITS.

2•3 HARDWARE PREPARATION

To select the desired configuration and ensure proper operation of the MPC850SARDB board, changes of the jumpers settings may be required before installation. The location of the jumpers, LEDs, and connectors is illustrated in FIGURE 2-1 "MPC850SARDB Top Side Part Location diagram" on page 5. The board has been factory tested and is shipped with settings as described in the following paragraphs. Parameters can be changed for the following conditions:

- Clock generator.
- Power-On Reset Source.
- MPC Keep Alive Power Source

FIGURE 2-1 MPC850SARDB Top Side Part Location diagram

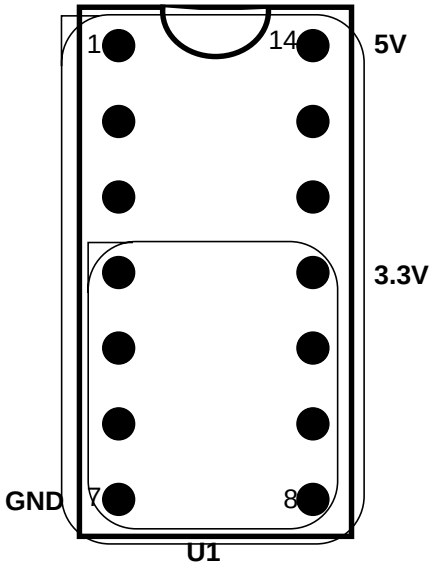


2•3•1 Clock Generator Replacement - U1

When replacing U1 with another clock generator it should be noticed that there are 2 supply level available at U1:

1) 5V supply at pin 14.
2) 3.3V supply available at pin 11.

FIGURE 2-2 U1 Power Sources



From looking at FIGURE 2-2 "U1 Power Sources" above, we see that 5V (with 3.3V output only!) oscillator may be used with 14 pins only form-factor while 3.3V oscillators may be used with 8 pins only form-factor.

WARNING

IF A 14 Pin Form-Factor, 3.3V Clock Generator is inserted to U1, PERMANENT DAMAGE Might Be Inflicted To The Device.

WARNING

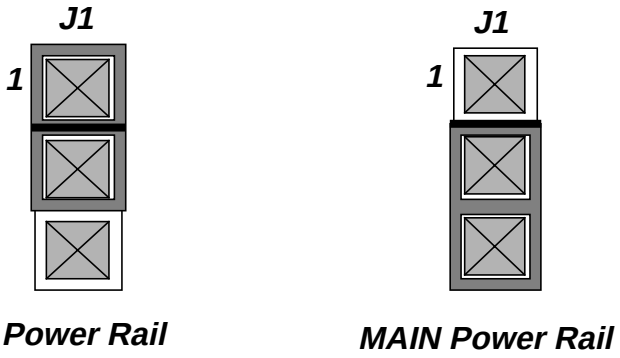
Since the MPC clock input is NOT 5V TOLERANT, any clock generator inserted to U1, MUST HAVE 3.3V compatible output. If a 5V output clock generator is inserted to U1, PERMANENT DAMAGE might be inflicted to the MPC.

2•3•2 Power-On Reset Source Selection

As there are differences between MPC revisions regarding the functionality of the Power-On Reset logic, it is therefore necessary to select different sources for Power-ON reset generation.

J1 on the 850DB is used to select Power-On Reset source: when a jumper is placed between positions 1 - 2 of J1, Power-On reset to the MPC is generated by the Keep-Alive power rail. I.e., When KAPWR goes below 2.005V - Power-On reset is generated. When a jumper is place between position 2 - 3 of J1, Power-On reset to the MPC is generated from the MAIN 3.3V power rail. I.e, when the MAIN 3.3V power rail goes below 2.805V Power-On reset is generated.

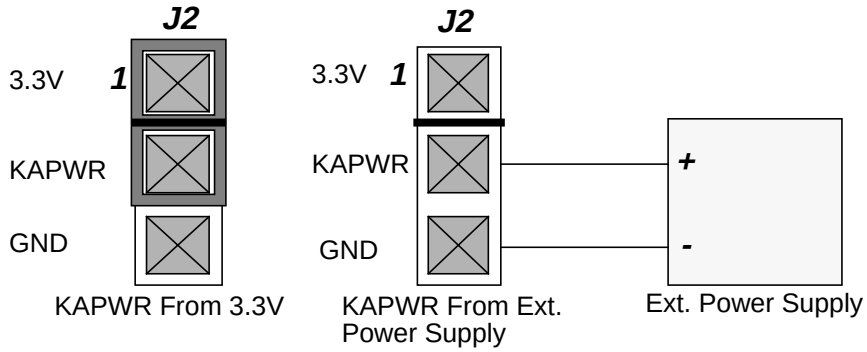
FIGURE 2-3 Power-On Reset Source Selection



2•3•3 Keep Alive Power Source Selection

J2 selects the Keep Alive power source of the MPC. When a jumper is placed between positions 1 - 2 of J2, the Keep Alive power is fed from the main 3.3V bus. When an external power source[A] is to be connected to the Keep Alive power rail, it should be connected between positions 2 (the positive pole) and position 3 (GND) of J2.

FIGURE 2-4 Keep Alive Power Source Selection

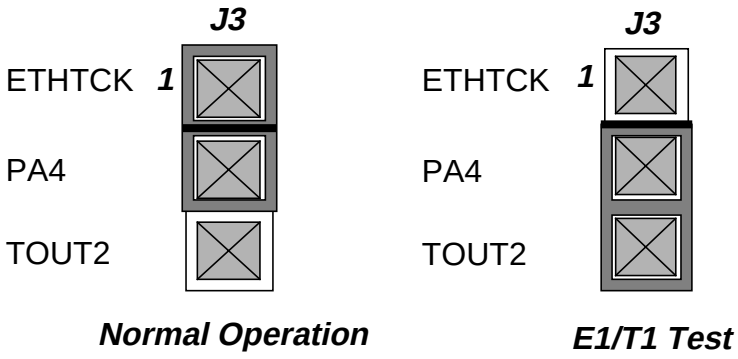


2•3•4 Port A Pin 4 Function Selection

J3 selects the functionality that pin PA4 takes. In normal operation it should be connected to ETHTCK; pins 1 - 2 of jumper J3. The jumper should be placed on pins 2 - 3 only when the E1/T1 channel is tested with an external loop (see the SAR-PHY User Manual for more details).

A. E.g., a battery.

FIGURE 2-5 PA4 Function Selection



Normal Operation *E1/T1 Test*

2•4 INSTALLATION INSTRUCTIONS

The MPC850SARDB should be plugged into the MPC8XXFADS Mother Board. This should be done when the FADS is disconnected from any power supply. The 850DB should be placed over the mother board connectors in a way that the mother board connectors of the 850DB, PM1 - PM4 match the daughter connectors of the FADS and than pressed gently into position.

The connectors are arranged in a non symmetrical form, so miss-insertion is not possible.

3 - OPERATING INSTRUCTIONS

3•1 INTRODUCTION

This chapter provides necessary information to use the MPC850SARDB

3•2 CONTROLS AND INDICATORS

The MPC850SARDB does not have any switches but has few indicators - described below:.

3•2•1 GND Bridges

There are 3 GND bridges on the MPC850SARDB. They are meant to assist general measurements and logic-analyzer connection.

Warning

The GND bridges on board, physically resemble J4. Do not mistake J4 to be a GND jumper, otherwise, permanent damage might be inflicted to the MPC850SARDB and or to the MPC8XXFADS.

Warning

When connecting to a GND bridge, use only INSULATED GND clips. Failure in doing so, might result in permanent damage to the MPC850SARDB.

3•2•2 3.3V Indicator - LD1

The yellow 3.3V led LD1 indicates that the 3.3V power bus is powered from the MPC8XXFADS.

3•2•3 USB - On Indicator - LD2

When the yellow USB-ON indicator led LD2 is lit, it designates that the USB transceiver is enabled for USB reception, i.e., the receive buffer is driven towards the MPC. When it is darkened, the receive buffer is tri-stated and the USB pins may be used for any alternate function. See also TABLE 4-23. "BCSR4 Description" on page 57 of the MPC8XXFADS User's Manual.

3•2•4 USB-PWR - LD3

When the yellow USB-PWR led is lit, it indicates that 5V power is driven to pin 1 of the USB connectors P3 & P4. When darkened, it indicates that pin 1 of these connectors is floating and the MPC850SARDB may be connected to external USB Master. See also TABLE 4-23. "BCSR4 Description" on page 57 of the MPC8XXFADS User's Manual.

3•3 MEMORY MAP

The memory map is identical to all daughter boards, therefore described in the MPC8XXFADS User's Manual - section 3•3 "MEMORY MAP" on page 16.

3•4 MPC Registers' Programming

See 3•4 "MPC Registers' Programming" on page 9 of the MPC8XXFADS User's Manual.

4 - Functional Description

In this chapter the various modules combining the MPC850SARDB are described to their design details.

4•1 Reset & Reset - Configuration

There are 3 reset sources for the MPC:

1) Power-On Reset[A]
2) Hard Reset
3) Soft Reset

4•1•1 Power-On Reset

The Power - On Reset on the MPC850SARDB is generated out of 2 alternative power buses:

1) The keep alive power bus
2) The MAIN power bus.

Selection between the 2 options is done by means of jumper.

When option (1) above is selected, the power-on reset is generated by a dedicated voltage detector made by Seiko the S-8051HN-CD-X with detection voltage range of 1.795 to 2.005V. During keep alive power-on or when there is a voltage drop of that input into the above range Power-On Reset is generated, i.e., PORESET* input of the MPC is asserted for a period of approximately 4 sec.

When option (2) above is selected, the power-on reset is generated by a dedicated voltage detector made by Seiko the S-8052ANY-NH-X with detection voltage range of 2.595V to 2.805V. During MAIN 3.3V bus power-on or when there is a voltage drop of that input into the above range Power-On Reset is generated, i.e., PORESET* input of the MPC is asserted for a period of approximately 4 sec. The MAIN power on reset also generates power-on reset to all logic located on the motherboard.

When PORESET* is asserted to the MPC, the Power-On reset configuration is made available to MPC. See 4•1•6•1 "Power - On Reset Configuration" on page 29 of MPC8XXFADS User's Manual.

4•1•2 Hard Reset

Hard Reset is generated to the MPC850 by the following sources:

1) The MAIN power-on reset
2) Manual Hard Reset generated on the mother board
3) The debug port Hard reset
4) and by MPC850's internal sources.

When the open-drain signal Hard Reset is asserted, Hard reset configuration is driven on the data bus by logic on the motherboard. See 4•1•6•2 "Hard Reset Configuration" on page 29 on MPC8XXFADS User's Manual.

4•1•3 Soft Reset

Soft Reset is generated to the MPC850 by the following sources:

1) The debug port controller located on the motherboard
2) Manual Soft Reset generated on the motherboard

A. In fact generated on the daughter board.

3) and by MPC850 internal sources.

When Soft reset is generated to the MPC850, Soft Reset configuration is made available to the MPC by logic residing over the motherboard. See 4•1•6•3 "Soft Reset Configuration" on page 29 on MPC8XXFADS User's Manual.

4•2 Interrupts

The two external interrupts which are applied to the MPC via its interrupt controller is the ABORT (NMI), which is generated by a push-button & logic residing over the motherboard, and the IRQ2 which is generated by the SAR-PHY board.

4•3 Clock Generator

Although most of clock generator logic is found on this board, it is documented within the motherboard User's Manual, since, it is common to all daughter boards. See 4•3 "Clock Generator" on page 30 of the MPC8XXFADS User's Manual.

4•4 PCMCIA Port

The MPC850 has only one PCMCIA port which resides on PCMCIA port B[A] pins. It is routed to the PCMCIA port on the MPC8XXFADS. The default Hard Reset Configuration of the FADS, sets these pins as PCMCIA port B pins.

The PCMCIA port on the FADS is meant to reside on PCMCIA port A of the MPCs. Therefore, there is a "cross" between PCMCIA ports A and B on the mother board connectors, i.e., port B's signals are connected also over places reserved for PCMCIA port A pins.

For further information see 4•10 "PCMCIA Port" on page 43 of the MPC8XXFADS User's Manual.

NOTE

I/O pin PC15 which is used as $\overline{\text{BINPAK}}$ is also used as RXCAC for the UTOPIA port. When the ATM channel on the SAR-PHY tool is active, the PCMCIA port can't be used and therefore must be disabled.

4•5 Communication Ports

The MPC850 has the following communication ports:

1) USB Port which is connected on board to a USB transceiver.
2) SCC2 which may be operated either as an Ethernet port or as an Infra/Red port or as RS232 Port #2.
3) SMC1 which is connected to RS232 Port #1 of the MPC8XXFADS.
4) SMC2 which supports TDM only and will not be used on board.
5) SPI, which is used for programming the E1/T1 Framer on the SAR-PHY board.

All communication ports may be enabled / disabled by S/W via BCSR1 or BCSR4. See TABLE 4-10. "BCSR1 Description" on page 49 and TABLE 4-23. "BCSR4 Description" on page 57 - both in MPC8XXFADS User's Manual.

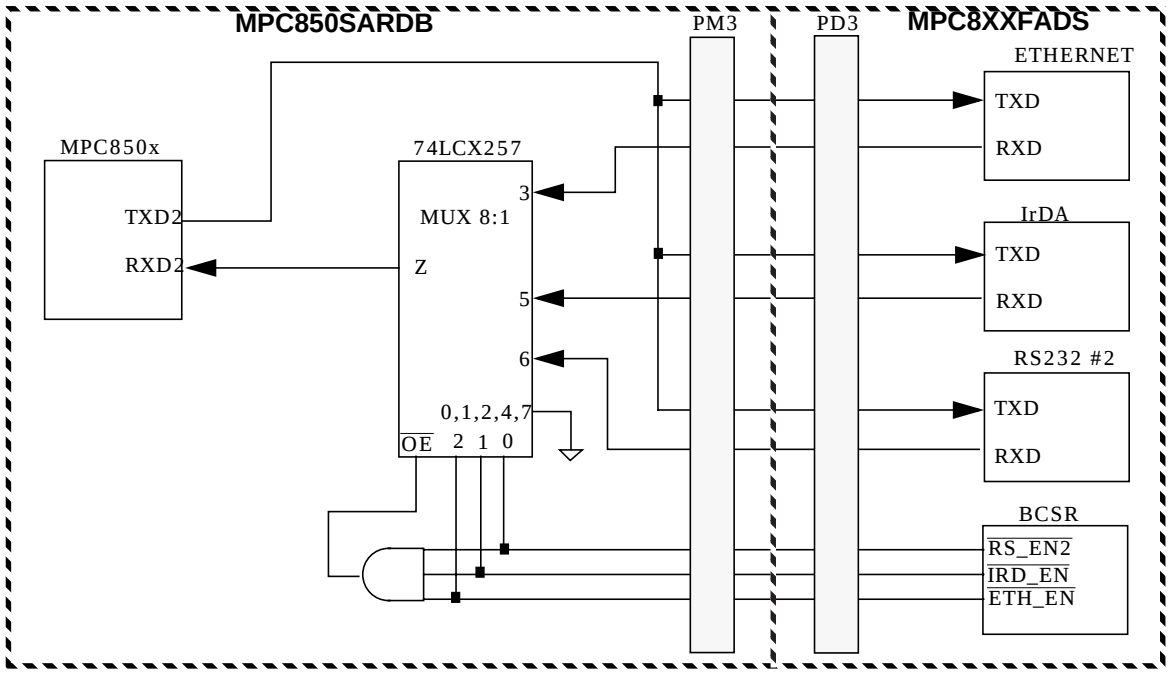
To protect against possible contention, the RxD lines of the Ethernet port, IrDA port and RS232 Port #2 of the MPC8XXFADS, are multiplexed to RXD2 input. The selection between the 3 RxD lines is done according to their respective enable bits in BCSR1. When ETH_EN~, IRD_EN~ or RS_EN2~ bits in BCSR1 are

A. In MPC821 Terms.

mutually exclusive enabled, their respective comm. port RxD line is driven to RXD2 of the MPC. If 2 or more of these lines are simultaneously enabled, '0' is driven to RXD2. When neither of them is asserted, the output of the mux is tri-stated, and RXD2 line of the MPC may be used for any alternate function.

The connection scheme of the Ethernet, IrDA and Serial Port #2 to SCC2 is shown in FIGURE 4-1 "SCC2 Connection Scheme" below:

FIGURE 4-1 SCC2 Connection Scheme



4•5•1 USB Port

The USB port resides on the MPC850SARDB and is driven by the USB port of the MPC850. A dedicated USB transceiver - the PDIUSBP11 by PHILIPS is provided, along with a tri-state buffer, separating this port from the MPC's USB port, this to allow Port disable option and off-board use of MPC USB pins.

To correctly support the 2 speed modes of the USB, detachable pull-up resistors (3.3V) are provided over D+ and D- lines of the USB, controlled by the USB_SPD bit of BCSR4. When USB_SPD is in low-speed level (low) D- is pulled-up while D+ remains floating. When USB_SPD bit is in high-speed level, D+ is being pulled-up and D- floats. USB_SPD is connected to the SPEED input of the USB transceiver, setting it to the desired operation range.

Also, 5V power is optionally provided for the USB connector, controlled by USB_VCC0 in BCSR4. When USB_VCC0 is driven low, a 5V supply is connected to pin 1 of the USB connectors.

To support both physical connection types, two USB connectors are provided in parallel - one of Type A and the other of Type B.

For additional information on USB port control see TABLE 4-23. "BCSR4 Description" on page 57 of the MPC8XXFADS User's Manual.

NOTE

In order to configure the devices on the SAR-PHY board, the USB port should be disabled due to dual functionality of I/O pins (see table 4.1). After the configuration is done, USB can be enabled and operated concurrently with the SAR-PHY board.

4•5•2 Ethernet Port

SCC2 of the MPC may be operated as an Ethernet port. Its may be connected to the ethernet transceiver on the MPC8XXFADS, provided that the ETH_EN bit in BCSR1 is asserted and both IRD_EN and RS_EN2 bits in the same register are inactive. See 4•9•1 "Ethernet Port" on page 41 and TABLE 4-10. "BCSR1 Description" on page 49 of MPC8XXFADS User's Manual.

NOTE

I/O pin PA4 which is used as ETHTCK is also used as TOUT2 for the E1/T1 port in a specific configuration. This is when L1TCLKA and L1TSYNCA are generated locally on the SAR-PHY board (see the SAR-PHY User manual). In this case, the Ethernet port can't be used and therefore must be disabled.

4•5•3 Infra-Red Port

SCC2 of the MPC may be operated as Fast IrDA port. Its may be connected to the Fast IrDA transceiver on the MPC8XXFADS, provided that the IRD_EN bit in BCSR1 is asserted and both ETH_EN and RS_EN2 bits in the same register are inactive. See 4•9•2 "Infra-Red Port" on page 41 and TABLE 4-10. "BCSR1 Description" on page 49 of MPC8XXFADS User's Manual.

4•5•4 RS232 Ports

There may be 2 RS232 ports with this application - RS232 Port #1 of the MPC8XXFADS is connected to SMC1 of the MPC850 while RS232 Port #2 of the FADS is optionally connected to SCC2 of the MPC850, this, when the RS_EN2 bit in BCSR1 is asserted while both ETH_EN and IRD_EN bits in the same register are inactive.

Both ports may be enabled / disabled at any time via BCSR1. See 4•9•3 "RS232 Ports" on page 42 and TABLE 4-10. "BCSR1 Description" on page 49 of the MPC8XXFADS.

NOTE

RS232 Port#2 DTR signal is used as an ALE signal on the SAR-PHY board (see table 4.1) so when the user configures one of the ATM modules on the SAR-PHY board, RS232 Port#2 must be disabled. After configuration is done, the port can be used concurrently with the SAR-PHY board.

4•6 E1/T1 Port

An E1/T1 channel can be implemented when using the SAR-PHY board. The channel is implemented with the serial - interface TDM channel of the MPC850x. The E1/T1 channel on the SAR-PHY board is configured using the SPI Port.

NOTE

One of the options when using the E1/T1 port on the SAR-PHY board is to generate L1TCLKA and L1TSYNCA locally using U12 (see the SAR-PHY User Manual). In this case, PA4 is used as TOUT2 and therefor the Ethernet port must be disabled.

4•7 Board Control & Status Register - BCSR

Most BCSR control signals and some of BCSR's status signals are available on the motherboard connectors and on the expansion connectors. The BCSR control most of the functions available on the MPC850DB and on the MPC8XXFADS.

See 4•11 "Board Control & Status Register - BCSR" on page 45 of MPC8XXFADS User's Manual.

4•8 Debug Port

The MPC850 is connected to the FADS's debug port controller through the mother board connectors. See 4•12 "Debug Port Controller" on page 58 of the MPC8XXFADS User's Manual.

The debug Port on the DB resides over the MPC850 JTAG port. No support is given for debug port to reside over PCMCIA port B pins.

Since VFLS(0:1) that are usually required by the debug port controller, to monitor for Run / Debug Mode status, are being used for PCMCIA port B, use is done with the FRZ signal which is connected to debug port controller on the MPC8XXFADS.

4•9 Communication Ports Expansion

On the MPC821/860ADS, all MPC821 or MPC860 communication ports' pins were available on a 96 pins DIN 41612 connector - designated as P13. Connector P8 of the MPC8XXFADS is compatible with this connector when MPC821FADSDB or MPC860FADSDB daughter boards are connected to the MPC8XXFADS. With the MPC850 however, which has different and partial comm. ports the pin assignment of this connector (P8) is different and any tool made for this connector, should be examined carefully prior to being connected to the MPC8XXFADS, having the MPC850SARDB connected to it.

4•10 Special Considerations

Special care must be observed when configuring the MPC850SAR. Some of the I/O pins have dual functionality (see table 4.1) and the correct functionality has to be according to the desired configuration. The details are as followed:

- Ethernet, InfraRed and RS232 Port2 are multiplexed. **Only one can be functional at a given time**. The selection is done with the BCSR.
- When using the E1/T1 port, there is an option on the SAR-PHY board to generate L1TSYNCA and L1TCLKA locally using the U12 clock generator (see the SAR-PHY user manual). In this case, U12 generates L1TCLKA and L1TSYNCA is generated internally by the MPC850 and output through TOUT2 (which is PA4). This I/O pin is also used as the ETHTCK so the Ethernet port must be disabled when utilizing this option. Pay attention that this is different than how it was done in the previous revision of the DaughterBoard. In the previous revision, U12 clock was inserted to the MPC850 through a dedicated I/O pin (TIN2 - PA5) and it was used to generate TOUT2. That would require the use of jumpers J8 and J9 on the SAR-PHY board. **In this revision, the option of TIN2 is not available so L1TCLKA or L1RCLKA are used to generate TOUT2**. Therefor, only jumper J8 is used on the SAR-PHY board. For a detailed explanation on the option look at the SAR-PHY board User Manual.
- **When configuring the SAR-PHY board, RS232 Port2 and the USB port must be disabled** since they share I/O pins with the SAR-PHY board. Those pins are used only for configuring the

SAR-PHY board so after the configuration is done (it should be a one time process), those pins can take the appropriate functionality to serve for the USB and RS232 port2. Because of the above, **I/O pins PB27 and PB26 (SAR-PHY board Chip Select and Reset respectively) must be disabled after the configuration of the SAR-PHY board is over** in order to avoid contention problems.

- When activating the ATM channel on the SAR-PHY tool, I/O pin PC15 functions as RXCAV of the UTOPIA port and therefore it can't function as $\overline{\text{BINPAK}}$ for the PCMCIA port. **The PCMCIA port must be disabled when operating the ATM channel on the SAR-PHY tool**.
- It should be noted that **the assignments of the I/O pins for the Ethernet port is different than the assignments on the previous revision of the Daughter Board**. For the new assignments,

see table 4.1 below.

TABLE 4-1. I/O Signals Functionality Assignments with the SAR-PHY Board

I/O Signal	USB	Ethernet	Infra-Red	RS232_1	RS232_2	PCMCIA	UTOPIA	E1/T1
PORT A								
PA15	RxD							
PA14	$\overline{OE}$							
PA13		RxD2	RxD2		RxD2			
PA12		TxD2	TxD2		TxD2			
PA9								L1TxDA
PA8								L1RxDA
PA7								L1RCLKA
PA6		RxCLK						
PA5								L1TCLKA
PA4		TxCLK						TOUT2
PORT B								
PB31								$\overline{E1/T1CS}$
PB30								SPI_CLK
PB29								SPI_IN
PB28								SPI_OUT
PB27							$\overline{PHYCS}$	
PB26							$\overline{RST\_BRD}$	
PB25				TxD1				
PB24				RxD1				
PB23				$\overline{DTR1}$				
PB22					$\overline{DTR2}$		PHYALE	
PB19							PHYAD0	
PB18		TENA						
PB17							PHYAD5	
PB16							PHYAD4	
PORT C								
PC15						$\overline{BINPAK}$	RxCAV	
PC14							$\overline{PHYWR}$	

TABLE 4-1. I/O Signals Functionality Assignments with the SAR-PHY Board

I/O Signal	USB	Ethernet	Infra-Red	RS232_1	RS232_2	PCMCIA	UTOPIA	E1/T1
PC13							$\overline{\text{PHYRD}}$	
PC12							TxCAV	
PC11	RxP						PHYAD7	
PC10	RxN						PHYAD3	
PC9		CLSN						
PC8		RENA						
PC7	TxP						PHYAD2	
PC6	TxN						PHYAD6	
PC5								L1TSYNCA
PC4								L1RSYNCA
PORT D								
PD15							UTPB0	
PD14							UTPB1	
PD13							UTPB2	
PD12							UTPB3	
PD11							$\overline{\text{RxENB}}$	
PD10							$\overline{\text{TxENB}}$	
PD9							UTPCLK	
PD8							PHYAD1	
PD7							UTPB4	
PD6							UTPB5	
PD5							UTPB6	
PD4							UTPB7	
PD3							UTPSOC	

5 - Support Information

In this chapter all information needed for support, maintenance and connectivity to the MPC850SARDB is provided.

5•1 Interconnect Signals

The MPC850SARDB interconnects with external devices via the following set of connectors:

1) P1, P2, P5, P6, P7 and P8 - Logic Analyzer connectors
2) P3 and P4 - USB connectors
3) PM1, PM2, PM3 and PM4 - Mother Board Connectors
4) PX1, PX2, PX3 & PX4 - Expansion Connectors
5) MPC8XXFADS's P8 - Serial Ports' Expansion Connector[A]

5•1•1 P1, P2, P5, P6, P7 and P8 - Logic Analyzer Connectors

These connectors are 38 pin, receptacle MICTOR connectors made by AMP. Each connector connects to a dedicated adaptor for HP 16500 series of logic analyzer, which interconnects to two 16 bit pods.

Since all the signals that appear on these connectors appear also on the mother-board connectors and on

TABLE 5-1 P1 - Interconnect Signals

Pin #	*Signal Name*	*Pin #*	*Signal Name*
1	N.C.	2	N.C.
3	GND	4	
5	N.C.	6	
7	SDRMCS~	8	BSWE0~
9	CS5~	10	BSWE1~
11	CE1B~	12	BSWE2~
13	CE2B~	14	BSWE3~
15	BR~	16	DRM_W~
17	BG~	18	EDOOE~
19	BB~	20	GPL2~
21	BI~	22	GPL3~
23	BURST~	24	GPL4A~
25	N.C.	26	GPL4B~
27		28	GPL5A~
29	BVS2	30	GPL5B~

A. This connector is located on the Mother Board. It is documented here since its contents depends on the Daughter Board.

Support Information

TABLE 5-1 P1 - Interconnect Signals

Pin #	*Signal Name*	*Pin #*	*Signal Name*
31	BVS1	32	F_CS~
33	BWP	34	BCSRCS~
35	BCD2~	36	DRMCS1~
37	BCD1~	38	DRMCS2~

TABLE 5-2. P2 - Interconnect Signals

Pin #	*Signal Name*	*Pin #*	*Signal Name*
1	N.C.	2	N.C.
3	GND	4	
5	N.C.	6	
7	TA~	8	A16
9	TS~	10	A17
11	TEA~	12	A18
13	R_W~	14	A19
15	REG_A~	16	A20
17	TSIZ1	18	A21
19	A6	20	A22
21	A7	22	A23
23	A8	24	A24
25	A9	26	A25
27	A10	28	A26
29	A11	30	A27
31	A12	32	A28
33	A13	34	A29
35	A14	36	A30
37	A15	38	A31

the expansion connectors, they are described there.

TABLE 5-3. P5 - Interconnect Signals

Pin #	*Signal Name*	*Pin #*	*Signal Name*
1	N.C.	2	N.C.
3	GND	4	
5	N.C.	6	
7	DSCK	8	DSDI
9	BBVD2	10	N.C.
11	BBVD1	12	DSDO
13	BRDY	14	FRZ
15	ALE_B	16	NMI~
17	SPKROUT	18	IRQ1~
19	MODCK1	20	IRQ2~
21	MODCK2	22	IRQ7~
23	WAIT_B~	24	N.C.
25	RSTCNF~	26	EXTCLK
27	TEXP	28	N.C.
29	HRESET~	30	DP0
31	SRESET~	32	DP1
33	PORST~	34	DP2
35	N.C.	36	DP3
37		38	V3.3

TABLE 5-4. P6 - Interconnect Signals

Pin #	*Signal Name*	*Pin #*	*Signal Name*
1	N.C.	2	N.C.
3	GND	4	
5	N.C.	6	
7	USBRXD	8	SYSCLK
9	USBOE~	10	N.C.
11	USBRXP	12	
13	USBRXN	14	
15	USBTXP	16	PC12

Support Information

TABLE 5-4. P6 - Interconnect Signals

Pin #	*Signal Name*	*Pin #*	*Signal Name*
17	USBTXN	18	TPSQEL~
19	TXD2	20	PC14
21	RXD2	22	BINPAK~
23	TMS	24	N.C.
25	PB27	26	SPARE2
27	PB26	28	N.C.
29	PB28	30	RSDTR1~
31	PB29	32	N.C.
33	PB30	34	RSDTR2~
35	PB31	36	RSRXD1
37	TRST~	38	RSTXD1

TABLE 5-5. P7 - Interconnect Signals

Pin #	*Signal Name*	*Pin #*	*Signal Name*
1	N.C.	2	N.C.
3	GND	4	
5	N.C.	6	
7		8	PD3
9	TOUT2	10	N.C.
11	ETHTCK	12	
13	PA5	14	PD4
15	ETHRCK	16	PD5
17	PA7	18	PD6
19	PA8	20	PD7
21	PA9	22	PD8
23	ETHLOOP	24	PD9
25	TPFLDL~	26	PD10
27	E_RENA	28	PD11
29	E_CLSN	30	PD12
31	PB16	32	PD13
33	PB17	34	PD14
35	E_TENA	36	PD15

TABLE 5-5. P7 - Interconnect Signals

Pin #	*Signal Name*	*Pin #*	*Signal Name*
37	PB19	38	SPARE3

TABLE 5-6. P8 - Interconnect Signals

Pin #	*Signal Name*	*Pin #*	*Signal Name*
1	N.C.	2	N.C.
3	GND	4	
5	N.C.	6	
7	D0	8	D16
9	D1	10	D17
11	D2	12	D18
13	D3	14	D19
15	D4	16	D20
17	D5	18	D21
19	D6	20	D22
21	D7	22	D23
23	D8	24	D24
25	D9	26	D25
27	D10	28	D26
29	D11	30	D27
31	D12	32	D28
33	D13	34	D29
35	D14	36	D30
37	D15	38	D31

5•1•2 P3 & P4 - USB connectors

The 850SARDB supports both Type-A and Type-B USB connectors. P3 is Type - B, P4 is Type - A, both made by AMP. Their pinto is identical. Their signals are described in TABLE 5-7. "P3 & P4 Interconnect

Signal" below:

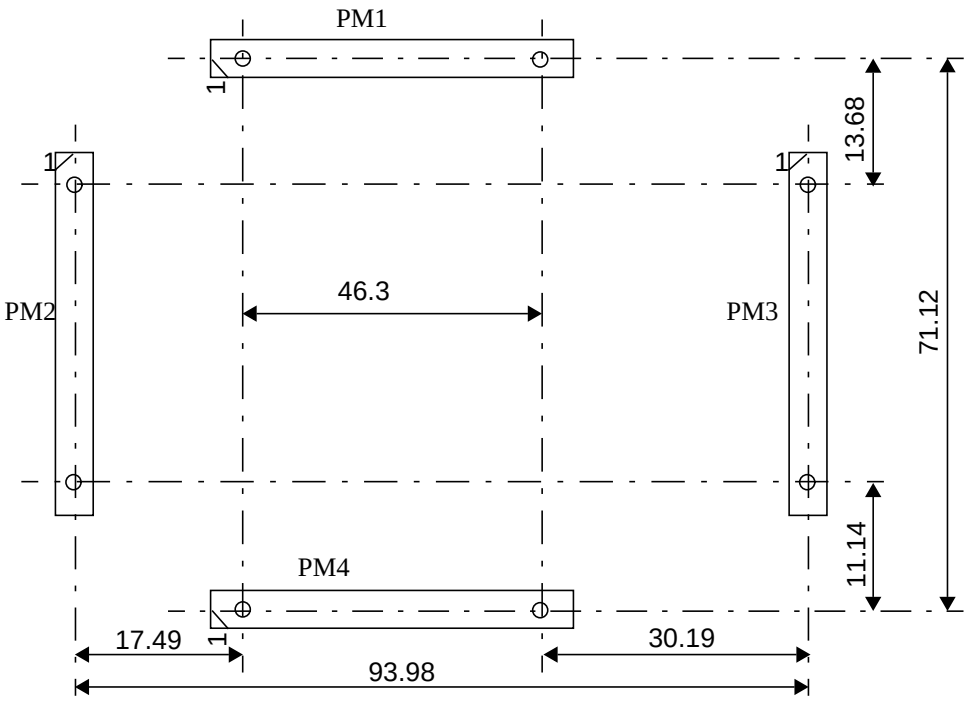
TABLE 5-7. P3 & P4 Interconnect Signal

Pin No.	*Signal Name*	*Attribute*	*Description*
1	USBPWR	O	USB Power. To support USB Host function, this pin may be driven with 5V BCSR controlled. See TABLE 4-23. "BCSR4 Description" on page 57 in the FADS User's Manual. When the 850DB is configured as a USB Slave, power should be turned-off for that pin.
2	D-	I/O	USB negative (differential) data line.
3	D+	I/O	USB positive (differential) data line.
4	GND	-	850DB Ground plane.

5•1•3 PM1 - PM4, Mother Board Connectors

These connectors which connect to their mates on the motherboard (hence their name) are 140 pin inter-board, male connectors made by Molex. These connectors are arranged in a quadratic shape, this to provide the shortest PCB routes as possible. As can be seen from their mechanical assembly shown in FIGURE 5-1 "Motherboard Connectors Mechanical Assembly" below - the connectors are not set in a perfect symmetric shape, this, to prevent the possibility of daughter-board's miss-insertion.

FIGURE 5-1 Motherboard Connectors Mechanical Assembly[A] [B]



The motherboard connectors's signals are described in TABLE 5-8. "PM1 Interconnect Signals" on page 25, TABLE 5-9. "PM2 Interconnect Signals" on page 30, TABLE 5-10. "PM3 Interconnect Signals" on page

A. Top View (from Component side)
B. All measures are in mm.

38 and TABLE 5-11. "PM4 Interconnect Signals" on page 45.

TABLE 5-8. PM1 Interconnect Signals

Pin No.	*Signal Name*	*Attribute*	*Description*
1	BB~	I/O, L	MPC's Bus Busy signal. Pulled - up on the FADS.
2	VCC		
3	DRM_W~	I,L	MPC's GPL0~ lines used as R/W~ signal for the DRAM simm or as A10 line for the SDRAM.
4	VCC	-	5V Bus.
5	TEA~	I/O, L, O.D.	Transfer Error Acknowledge. Pulled-up, not driven on board.
6	VCC		
7	BR~	I/O,L	MPC's Bus Request signal. Pulled - up on the FADS, but otherwise unused.
8	VCC		
9	BURST~	I/O, L	MPC's Burst indication. Pulled - up on the FADS, but otherwise unused.
10	VCC		
11	GPL4A~	X,L	UPMA general purpose line 4. Not used on the FADS.
12	VCC		
13	TA~	I/O, L	MPC's transfer Acknowledge signal. Indicates end of bus cycle, used with FADS logic.
14	VCC		
15	TS~	I/O, L	MPC's Transfer Start indication. Pulled - up, but otherwise unused on the FADS.
16	VCC		
17	GPL5B~	O, L	General Purpose Line 5 of UPMB. Not used on the FADS.
18	VCC		
19	BG~	I/O, L	MPC's Bus grant signal. Pulled - up on the FADS, but otherwise unused.
20	VCC		
21	GPL4B~	O, L	General Purpose Line 4 of UPMB. Not used on the FADS.
22	VCC		
23	R_W~	I/O, L	MPC's Read/Write~ indication. Pulled - up on the FADS and used by FADS logic.
24	VCC		
25	BCSRCS~	I/O, L	In fact CS1~ of the MPC. Used as chip-select for the BCSRs. Pulled - up. When BCSR is removed from the local map, may be used off-board via the expansion connectors.

Support Information

TABLE 5-8. PM1 Interconnect Signals

Pin No.	*Signal Name*	*Attribute*	*Description*
26	VCC	O	5V Bus.
27	GPL5A~	X,L	UPMA general purpose line 5. Not used on the FADS.
28	VCC	O	5V Bus.
29	BI~	I/O,L	MPC's Burst Inhibit input. Pulled - up, but otherwise unused on the FADS.
30	N.C.	-	Not Connected. Reserved.
31	CE2B~	O,L	MPC850's PC-Card Enable 2. Enables ODD address bytes. Connected to the FADS PC-Card control logic.
32	GND	-	FADS Ground plane.
33	CS5~	O, L	MPC's Chip Select line 5. Unused on the FADS.
34	GND		
35	CE1B~	I, L	PC-Card Enable 1 for PCMCIA slot B. Enables the EVEN address bytes. Connected to the FADS's PC-Card control logic.
36	GND		
37	F_CS~	I/O, L	In fact MPC's chip-select line 0. Used as chip-select for the Flash Simm on FADS. Pulled - up on the M/B. When the Flash is disabled via BCSR, may be used off-board via the expansion connectors.
38	GND		
39	CE1B~	O, L	See pin 35. Duality exists since the MPC850 uses slot B controls for the FADS's PC-Card, originally residing over slot-A.
40	GND		
41	CE2B~	O, L	See pin 31. Duality exists since the MPC850 uses slot B controls for the FADS's PC-Card, originally residing over slot-A
42	GND		
43	DRMCS2~	I/O, L	In fact MPC's chip-select line 3. Used as chip-select line for the 2'nd bank of the Dram Simm. Pulled - up on the M/B. When the Dram is disabled via BCSR or when a single-bank Dram Simm is being used - may be used off-board via the expansion connectors.
44	GND		
45	DRMCS1~	I/O, L	In fact MPC's chip-select line 2. Used as chip-select line for the 1'st bank of the Dram Simm. Pulled - up on the M/B. When the Dram is disabled via BCSR - may be used off-board via the expansion connectors.
46	GND		

Support Information

TABLE 5-8. PM1 Interconnect Signals

Pin No.	*Signal Name*	*Attribute*	*Description*
47	SDRMCS~	I/O, L	In fact MPC's chip-select line 4. Used as chip-select for the Synchronous Dram. Pulled - up on the M/B. When the SDRAM is disabled via BCSR, may be used off-board via the expansion connectors.
48	GND		
49	GPL3~	O, L	UPMA or UPMB general purpose line 3. Used as WR~ signal for the SDRAM.
50	GND		
51	GPL2~	O, L	General Purpose Line 2 for UPMA or UPMB. Used with the SDRAM, as a CAS~ signal.
52	GND		
53	BSWE3~	O, L	UPM Byte Select 3 or GPCM Write Enable 3 or PCMCIA WE~. Selects the LSB within a word for the SDRAM, EDO DRAM and Flash Simm or qualifies Writes for the PC-Card.
54	GND		
55	BSWE2~	O, L	UPM Byte Select 2, GPCM Write Enable 2 or PCMCIA OE~. Selects the offset 2 Byte within a word for the SDRAM, EDO DRAM and Flash Simm or open data buffers for read from PC-Card.
56	GND		
57	BSWE1~	O, L	UPM Byte Select 1 or GPCM Write Enable1 or PCMCIA I/O Write. Selects the offset 1 Byte within a word for the SDRAM, EDO DRAM and Flash Simm or functions as I/O Write for the PCMCIA channel.
58	GND		
59	BSWE2~	O, L	See pin 55. The duality due to separation of BS(0:3)_A~ from WE(0:3)~/BS(0:3)_B~ with other members of the 8xx family.
60	GND		
61	BSWE0~	O, L	UPM Byte Select 0 or GPCM Write Enable 0 or PCMCIA I/O Read. Selects the offset 0 Byte within a word for the SDRAM, EDO DRAM and Flash Simm or functions as I/O Reads from PC-Card.
62	GND		
63	N.C.		
64	GND		
65	EDOOE~	O,L	In fact UPMA or UPMB General Purpose Line 1. Used for Output Enable with EDO Dram simms, which have this input (most of them don't). Used also as RAS signal for the SDRAM.
66	GND		

Support Information

TABLE 5-8. PM1 Interconnect Signals

Pin No.	*Signal Name*	*Attribute*	*Description*
67	BSWE0~	O, L	See pin 61. The duality due to separation of BS(0:3)_A~ from WE(0:3)~/BS(0:3)_B~ with other members of the 8xx family.
68	GND		
69	BSWE3~	O, L	See pin 53. The duality due to separation of BS(0:3)_A~ from WE(0:3)~/BS(0:3)_B~ with other members of the 8xx family.
70	GND		
71	A31	O, T.S.	MPC's Address line 31.
72	GND		
73	BSWE1~	O, L	See pin 57. The duality due to separation of BS(0:3)_A~ from WE(0:3)~/BS(0:3)_B~ with other members of the 8xx family.
74	GND		
75	TSIZ1	O, T.S.	Transfer Size 1. Used in conjunction with TSIZ0 to indicate the number of bytes remaining in an operand transfer. Not used on the FADS.
76	GND		
77	REG_A~	O, T.S., L	In fact TSIZ0/REG~. Transfer Size 0 or PCMCIA REG~. Used with the PCMCIA port as Attribute memory select or I/O space select.
78	GND		
79	A30	O, T.S.	MPC's Address line 30.
80	GND		
81	A21	O, T.S.	MPC's Address line 21.
82	GND		
83	A20	O, T.S.	MPC's Address line 20.
84	GND		
85	A7	O, T.S.	MPC's Address line 7.
86	GND		
87	A15	O, T.S.	MPC's Address line 15.
88	GND		
89	A14	O, T.S.	MPC's Address line 14.
90	GND		
91	A13	O, T.S.	MPC's Address line 13.
92	GND		
93	A6	O, T.S.	MPC's Address line 6.

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TABLE 5-8. PM1 Interconnect Signals

Pin No.	*Signal Name*	*Attribute*	*Description*
94	GND		
95	A12	O, T.S.	MPC's Address line 12.
96	GND		
97	A11	O, T.S.	MPC's Address line 11.
98	GND		
99	A19	O, T.S.	MPC's Address line 19.
100	GND		
101	A9	O, T.S.	MPC's Address line 9.
102	GND		
103	A18	O, T.S.	MPC's Address line 18.
104	GND		
105	A10	O, T.S.	MPC's Address line 10.
106	GND		
107	A17	O, T.S.	MPC's Address line 17.
108	GND		
109	A16	O, T.S.	MPC's Address line 16.
110	GND		
111	A8	O, T.S.	MPC's Address line 8.
112	GND		
113	A29	O, T.S.	MPC's Address line 29.
114	GND		
115	A27	O, T.S.	MPC's Address line 27.
116	GND		
117	A28	O, T.S.	MPC's Address line 28.
118	GND		
119	A26	O, T.S.	MPC's Address line 26.
120	GND		
121	A25	O, T.S.	MPC's Address line 25.
122	GND		
123	A24	O, T.S.	MPC's Address line 24.
124	GND		

TABLE 5-8. PM1 Interconnect Signals

Pin No.	*Signal Name*	*Attribute*	*Description*
125	A22	O, T.S.	MPC's Address line 22.
126	GND		
127	N.C.		
128	GND		
129	A23	O, T.S.	MPC's Address line 23.
130	GND		
131	N.C.		
132	GND		
133	N.C		
134	GND		
135	N.C.		
136	GND		
137	N.C.		
138	GND		
139	N.C.		
140	GND		

TABLE 5-9. PM2 Interconnect Signals

Pin No.	*Signal Name*	*Attribute*	*Description*
1	V12	O	10V output from voltage doubler. Used to switch TMOS gates on both mother and daughter boards. Should not be used for any other purpose.
2			
3			
4			
5	N.C.		
6			
7	DSDI	I, X	DSDI/TDI. Debug Port Serial Data Input or JTAG port serial Data Input. Used on the FADS as debug port serial data, driven by the debug-port controller. If the ADI bundle is not connected to the FADS, may be driven by external debug / JTAG[a] port controller.
8	GND		
9			

Support Information

TABLE 5-9. PM2 Interconnect Signals

Pin No.	*Signal Name*	*Attribute*	*Description*
10	DSCK	I, X	DSCK/TCK. Debug Port Serial Clock input or JTAG port serial clock input. Used on the FADS as debug port serial clock, driven by the debug-port controller. If the ADI bundle is not connected to the FADS, may be driven by an external debug / JTAG[a] port controller.
11	DSDO	O, X	DSDO/TDO. Debug Port Serial Data Output or JTAG port Data Output. Used on the FADS as debug port serial data. If the ADI bundle is not connected to the FADS, may be used by an external debug / JTAG[a] port controllers.
12	GND		
13			
14	BWP	I/O	In fact IP_B2/IOIS16~/AT2. PCMCIA slot B Input Port 2 or PCMCIA 16 bit I/O capability indication or Address Type 2. Configured as IP_B2 and functions as PC-Card's Write Protect signal. If the PCMCIA channel is disabled, may be configured to alternate function.
15	GND		
16	BCD2~	I/O	IP_B3/IWP2/VF2. PCMCIA slot B Input Port 3 or Instruction Watch-Point 2 or Visible Instruction Queue Flushes Status 2. Configured as IP_B3 to function as PC-Card Detect 2 signal. If the PCMCIA channel is disabled, may be configured to alternate function.
17	GND		
18	BCD1~	I/O	IP_B4/LWP0/VF0. PCMCIA slot B Input Port 4 or Data Watch-Point 0 or Visible Instruction Queue Flushes Status 0. Configured as IP_B4 to function as PC-Card Detect 1 signal. If the PCMCIA channel is disabled, may be configured to alternate function.
19	GND		
20			
21			
22	N.C.		
23	GND		
24	FRZ	I/O, X	Freeze / IRQ6~. MPC debug state indication or Interrupt request line 6. Used by the debug port controller as debug state indication. May be configured to alternate function provided that VFLS(0:1) function as VFLS and J1 is moved to position 1-2.
25	GND		
26	IRQ2~	I/O, L	RSV~/IRQ2~. Reservation or Interrupt Request 2. Pulled - up on the M/B but otherwise unused on the FADS.

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TABLE 5-9. PM2 Interconnect Signals

Pin No.	*Signal Name*	*Attribute*	*Description*
27	GND		
28			
29			
30	BRDY	I/O, X	IP_B7/PTR/AT3. PCMCIA slot B Input Port 7 or Program Trace (instruction fetch indication or Address Type 3. Configured as IP_B7 to function as PC-Card Ready indication. If the PCMCIA channel is disabled, may be configured to alternate function.
31	GND		
32	N.C.		
33	GND		
34	BVS1	I/O, X	IP_B0/IWP0/VFLS0. PCMCIA slot B Input Port 0 or Instruction Watchpoint 0 or Visible history Flushes Status 0. Configured as IP_B0 to function as PC-Card's Voltage Sense 1. If the PCMCIA channel is disabled, may be configured to alternate function.
35	GND		
36	SPKROUT	I/O, X	KR~/IRQ4~/SPKROUT. Kill Reservation input or Interrupt Request 4 input or PCMCIA Speaker Output. Configured SPKROUT. If the PCMCIA channel is disabled, may be configured to alternate function.
37	GND		
38	BVS2	I/O, X	IP_B1/IWP1/VFLS1. PCMCIA slot B Input Port 1 or Instruction Watchpoint 1 or Visible history Flushes Status 1. Configured as IP_B1 to function as PC-Card Voltage Sense 2. If the PCMCIA channel is disabled, may be configured to alternate function.
39	GND		
40			
41			
42	BBVD2	-	IP_B5/IWP1/VF1. PCMCIA slot B Input Port 5 or Load/Store Watch-Point 1 or Visible Instruction Queue Flushes Status 1. Configured as IP_B5 to function as Battery Voltage Detect 2. If the PCMCIA channel is disabled, may be configured to alternate function.
43	GND		
44	ALE_B	I/O, X	ALE_B/DSCK/AT1. Address Latch Enable for PCMCIA slot B or Debug Serial Clock or Address Type 1. Configured as ALE_B. If the PCMCIA channel is disabled, may be configured to alternate function.
45	GND		

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TABLE 5-9. PM2 Interconnect Signals

Pin No.	*Signal Name*	*Attribute*	*Description*
46	BBVD1	I/O, X	IP_B6/DSDI/AT0. Input Port B 6 or Debug Serial Data Input or Address Type 0. Configured as IP_B6 to function as PC-Card's Battery Voltage Detect 1. May be used for alternate function. If the PCMCIA channel is disabled, may be configured to alternate function.
47	GND		
48	MODCK2	I/O, L	MODCK2/OP1. Upon Power On reset determines along with MODCK1 the clock operation mode for the MPC. After PON reset, serves as OE~ for the PCMCIA port.
49	GND		
50			
51			
52	N.C.		
53	GND		
54	ALE_B	I/O, H	See pin 44. The duality since the MPC850's PCMCIA port B is connected to PCMCIA port on the M/B, normally residing on PCMCIA port A of the MPC8XXs.
55	GND		
56	N.C.		
57	GND		
58	AS~	I, L	Asynchronous external master Address Strobe signal. When asserted (L) by the external master, the MPC recognizes an asynchronous cycle in progress. Pulled - up but otherwise unused on the FADS.
59	GND		
60	MODCK1	I/O	OP2/MODCK1/STS~. PCMCIA Output Port 2 or Mode Clock 1 input or Special Transfer Start output. Used at Power-On reset as MODCK1. Configured afterwards as a OP2 to function as PC-Card Reset.
61	GND		
62	MODCK1	I,H	See pin 60. The duality since the MPC850's PCMCIA port B is connected to PCMCIA port on the M/B, normally residing on PCMCIA port A of the MPC8XXs.
63	GND		
64			
65			
66	N.C.		
67	GND		

Support Information

TABLE 5-9. PM2 Interconnect Signals

Pin No.	*Signal Name*	*Attribute*	*Description*
68	TEXP	O, H	MPC Timer Expired. Not used on the FADS.
69	GND		
70	WAIT_B~	I/O, L	This signal is PCMCIA slot B wait signal. Pulled-up but otherwise not used on the FADS.
71	GND		
72	MODCK2	I/O, X	See pin 48. The duality since the MPC850's PCMCIA port B is connected to PCMCIA port on the M/B, normally residing on PCMCIA port A of the MPC8XXs.
73	GND		
74			
75			
76	N.C.		
77	GND		
78			
79			
80	SRESET~	I/O, L, O.D.	MPC Soft Reset. Driven by M/B logic and may be driven by off-board logic with Open-Drain gate only.
81	GND		
82	PORST~	O, L	Power On reset for the MPC. Not used on the FADS.
83	GND		
84	HRESET~	I/O, L, O.D.	MPC Hard Reset. Driven by M/B logic and may be driven by off-board logic with Open-Drain gate only.
85	GND		
86	RSTCNF~	I, L	Hard Reset Configuration input. Driven by M/B logic during Hard Reset to the MPC, to signal the MPC that it should sample Hard Reset configuration from the data bus.
87	GND		
88	R_PORI~	I, L	Main battery power-on reset. Generated by M/B logic as a result of main 3.3V bus going through power up or power-down. Drives M/B's logic as well either HARD-RESET or Power-On reset to the MPC.
89	GND		
90			
91			
92	WAIT_B~	I/O, L	See pin 70. The duality since the MPC850's PCMCIA port B is connected to PCMCIA port on the M/B, normally residing on PCMCIA port A of the MPC8XXs.

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TABLE 5-9. PM2 Interconnect Signals

Pin No.	*Signal Name*	*Attribute*	*Description*
93	GND		
94	BWP	I/O, H	See pin 14. The duality since the MPC850's PCMCIA port B is connected to PCMCIA port on the M/B, normally residing on PCMCIA port A of the MPC8XXs.
95	GND		
96	BVS1	I/O,X	See pin 34. The duality since the MPC850's PCMCIA port B is connected to PCMCIA port on the M/B, normally residing on PCMCIA port A of the MPC8XXs.
97	GND		
98	BRDY	I/O, H	See pin 30. The duality since the MPC850's PCMCIA port B is connected to PCMCIA port on the M/B, normally residing on PCMCIA port A of the MPC8XXs.
99	GND		
100			
101			
102	DP3	I/O, X	DP3/IRQ6~. Data Parity line 3 or Interrupt Request 6. May generate and receive parity data for D(24:31) bits connected to the DRAM SIMM. May be configured as IRQ6~ input for the MPC only if the DRAM is disabled on the M/B.
103	GND		
104	BVS2	I/O, X	See pin 38. The duality since the MPC850's PCMCIA port B is connected to PCMCIA port on the M/B, normally residing on PCMCIA port A of the MPC8XXs.
105	GND		
106	BCD1~	I/O, L	See pin 18. The duality since the MPC850's PCMCIA port B is connected to PCMCIA port on the M/B, normally residing on PCMCIA port A of the MPC8XXs.
107	GND		
108	MODIN	I, X	This signal selects between clock generator and the 32768 Hz crystal as clock sources for the MPC. Its is driven by DS2/4 of the M/B. See 2•3•2 "Clock Source Selection" on page 7 of the MPC8XXFADS User's Manual.
109	GND		
110	BBVD1	O, X	Buffered PCMCIA slot A Battery Voltage Detect 1. In fact IP_A6. Used in conjunction with BBVD2 to determine the battery status of a PC-Card. In case of MPC850 or MPC850 daughter boards, connected to IP_B6 signal of the MPC.
111	GND		

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TABLE 5-9. PM2 Interconnect Signals

Pin No.	*Signal Name*	*Attribute*	*Description*
112	BCD2~	I/O, L	See pin 16. The duality since the MPC850's PCMCIA port B is connected to PCMCIA port on the M/B, normally residing on PCMCIA port A of the MPC8XXs.
113	GND		
114	BBVD2	I/O, X	See pin 42. The duality since the MPC850's PCMCIA port B is connected to PCMCIA port on the M/B, normally residing on PCMCIA port A of the MPC8XXs.
115	GND		
116			
117	N.C.		
118	DP0	I/O, X	DP0/IRQ3~. Data Parity line 0 or Interrupt Request 3. May generate and receive parity data for D(0:7) bits connected to the DRAM SIMM. May be configured as IRQ3~ only if the DRAM is disabled on the M/B.
119	V3.3		
120	DP2	I/O, X	DP2/IRQ5~. Data Parity line 2 or Interrupt Request 5. May generate and receive parity data for D(16:23) bits connected to the DRAM SIMM. May be configured as IRQ5~ only if the DRAM is disabled on the M/B.
121	V3.3		
122	DP1	I/O, X	DP1/IRQ4~. Data Parity line1 or Interrupt Request 4. May generate and receive parity data for D(8:15) bits connected to the DRAM SIMM. May be configured as IRQ4~ only if the DRAM is disabled on the M/B.
123	V3.3		
124	N.C.		
125	V3.3		
126	IRQ1~	I/O, L	Interrupt Request 1.Pulled-up on the M/B, but otherwise not used on the FADS.
127	V3.3		
128	SPARE3	I/O, X	MPC's spare line 3. Pulled - up but otherwise unused on the FADS.
129	V3.3		
130	IRQ7~	I/O, L	Interrupt Request 7. The lowest priority interrupt request line. Pulled - up but otherwise not used on the FADS.
131	V3.3		
132	N.C.		
133	V3.3		

Support Information

TABLE 5-9. PM2 Interconnect Signals

Pin No.	*Signal Name*	*Attribute*	*Description*
134	NMI~	I, L	Non-Makable Interrupt. In fact IRQ0~ of the MPC. Driven by M/B logic by O.D. gate. Pulled - up. May be driven off-board by O.D. gate only.
135	V3.3		
136	N.C.		
137	V3.3		
138	N.C.		
139	V3.3		
140	N.C.		

a. Be aware that TRST~ is connected to GND with a zero ohm resistor.

TABLE 5-10. PM3 Interconnect Signals

Pin No.	Signal Name	Attribute	Description
1	ETHRX	O, X	Ethernet port Receive Data. When the ethernet port is disabled via BCSR1 - tri-stated. Appears also at P8 of the M/B as PA13 when Ethernet port is selected.
2	GND		
3			
4	USBEN~	O, L	Usb Port Enable Generated by BCSR4 on the M/B. See TABLE 4-23. "BCSR4 Description" on page 57.
5	TXD2	O, X	SCC2's TXD output. Connected to the Ethernet, IrDA and RS232 #2 ports on the M/B. Appears also at P8 of the M/B as PA12 when Ethernet, or RS232#2 or InfraRed port is selected.
6	GND		
7			
8	PD8	I/O,X	MPC port D 8/SAR-PHY Address/Data line 1. Appears twice at P8 of the M/B - first place as PD8 and second place as SAR-PHY Address/Data line 1.
9	IRDRXD	I, X	InfraRed Port Receive Data. When the I/R port is disabled via BCSR1 - tri-stated. Appears also at P8 of the M/B as PA13 when InfraRed port is selected.
10	GND		
11	TXD2	O, X	See pin 5. Appears on 3 different pins since for the 850DB - the Ethernet, IrDA and RS232 port #2 are connected to the same SCC (2).
12	GND		
13			
14	PB19	I/O,X	SAR-PHY tool Address/Data line 0.
15	PA9	I/O, X	Appears also as L1TXDA at P8 of the M/B to support the E1/T1 Port on the SAR-PHY Tool.
16	GND		
17	PA8	I/O, X	Appears also as L1RXDA at P8 of the M/B to support the E1/T1 Port on the SAR-PHY Tool.
18	GND		
19			
20	PC5	I/O, X	Appears also as L1TSYNCA at P8 of the M/B to support the E1/T1 Port on the SAR-PHY Tool.

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TABLE 5-10. PM3 Interconnect Signals

Pin No.	Signal Name	Attribute	Description
21	USBRXP	O, X	MPC850's PC 11/USBRXP/SAR-PHY AD7. One of USB transceiver's receive signals. Appears also at P8 of the M/B as SAR-PHY Address/Data Line 7 as support to the SAR-PHY tool.
22	GND		
23	USBTXN	I/O, X	MPC PC6. When the USB port is enabled, serves as negative differential transmit data. Appears also at P8 of the M/B as SAR-PHY Address/Data Line 6 as support to the SAR-PHY tool.When the USB port is disabled via BCSR1, may used for any alternate function.
24	GND		
25			
26	PB31	I/O, X	MPC PI/O port B 31. Appears also at P8 of the M/B as E1/T1 Chip Select for the SAR-PHY Tool.
27	ETHTCK	I/O, X	MPC PI/O port A 4 / E1/T1 L1TSYNCA. Ethernet port Transmit Clock. Appears also at P8 of the M/B E1/T1 L1TSYNCA TOUT2 signal.
28	GND		
29	ETHRCK	O, X	MPC PI/O port A 6. Ethernet port Receive Clock. When the ethernet port is disabled via BCSR1 - tri-stated. Appears also at P8 of the M/B.
30	GND		
31			
32	USBSPD	I, X	Usb port Speed control. Controls the speed of the USB transceiver, while changing pull-up resistors between USB D+ and D- lines. See also TABLE 4-23. "BCSR4 Description" on page 57 of the MPC8XXFADS User's Manual.
33	N.C.		
34	BINPAK~	I/O, X	PC15/$\overline{\text{BINPAK}}$/RXCAV. PCMCIA port Input Port Acknowledge. When the PCMCIA port is disabled via BCSR1, it may be used as RXCAV for the UTOPIA port or off-board for any alternate function.
35	PB30	I/O, X	MPC PI/O port B 30. Appears also at P8 of the M/B as E1/T1 SPI_CLOCK for the SAR-PHY tool.
36	GND		
37	PB29	I/O, X	MPC PI/O port B 29. Appears also at P8 of the M/B as E1/T1 SPI_IN for the SAR-PHY tool.
38	RSTXD1	I/O, X	In fact PB25/SMTXD1. RS232 Port 1 Transmit Data. When RS232 port 1 is disabled via BCSR1, may be used for any alternate function. Appears also at P8 of the M/B.

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TABLE 5-10. PM3 Interconnect Signals

Pin No.	*Signal Name*	*Attribute*	*Description*
39	RSRXD1	I/O, X	In fact PB24/SMRXD1. RS232 Port 1 Receive Data. When RS232 port 1 is disabled via BCSR1 - tri-stated and may be used for any alternate function. Appears also at P8 of the M/B.
40	RSDTR1~	I/O, L	In fact PB23/SDACK1~. RS232 port 1 DTR~ signal. When RS232 port 1 is disabled via BCSR1 - tri-stated and may be used for any alternate function. Appears also at P8 of the M/B.
41	GND		
42	TXD2	I/O, X	See pins 5 & 11.
43	RSRXD2	I/O, X	Rs232 port 2 Receive Data. When the IRS232 port is disabled via BCSR1 - tri-stated. Appears also at P8 of the M/B as PA13 when RS232 port 2 is selected.
44	RSDTR2~	I/O, L	PB22/RS232 port 2 DTR~ signal. When RS232 port 2 is disabled via BCSR1 - tri-stated and may be used for any alternate function. Appears also at P8 of the M/B.
45	N.C.		
46	GND		
47	N.C.		
48	GND		
49			
50	PB27	I/O, X	Appears also at P8 of the M/B as $\overline{\text{PHYCS}}$ for the SAR-PHY tool.
51	PB28	I/O, X	MPC PI/O port B 28. Appears also at P8 of the M/B as E1/T1 SPI_OUT for the SAR-PHY tool.
52	GND		
53	PC14	I/O, X	MPC PI/O port C 14. Appears also at P8 of the M/B as $\overline{\text{PHYWR}}$ for the SAR-PHY tool.
54	PB26	I/O, X	Also MPC PI/O port B 26. Appears also at P8 of the M/B as $\overline{\text{RST\_BRD}}$ for the SAR-PHY tool.
55	GND		
56			
57	N.C.		
58	GND		
59			
60	TOUT2	I/O, X	MPC PI/O port A 4. Appears also at P8 of the M/B as TOUT2 for the SAR-PHY tool. Selected with J3.
61	E_CLSN	I/O, H	Ethernet Port Collision indication signal. Also PC9/CTS2. Connected to the SCC2's CTS~ signal. When the Ethernet port is disabled via BCSR1, may be used off-board for any alternate function. Appears also on P8 of the M/B.

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TABLE 5-10. PM3 Interconnect Signals

Pin No.	*Signal Name*	*Attribute*	*Description*
62	E_RENA	I/O, H	Ethernet Receive Enable. Also PC8/CD2~. Connected to the SCC2's CD~ signal. Active when there is network activity. When the Ethernet port is disabled via BCSR1, may be used off-board for any alternate function. Appears also on P8 of the M/B.
63	SPARE2	I/O, X	MPC spare line 2. Pulled - up but otherwise unused on the FADS.
64	VDOEN~	I, L	Reserved. Not used with this board.
65	GND		
66			
67	SYSCLK	I, X	System Clock. In fact the CLKOUT of the MPC.
68	GND		
69			
70			
71	USBRXN	O, X	MPC850's PC 10/USBRXN/SAR-PHY AD3. One of USB transceiver's receive signals. Appears also at P8 of the M/B as Address/Data Line 3 for the SAR-PHY tool.
72	GND		
73			
74	PA7	I/O, X	MPC850 port a 7/L1RCLKA. Appears also at P8 of the M/B as E1/T1 L1RCLKA for the SAR-PHY tool.
75	PB17	I/O, X	MPC850's PB17/SAR-PHY AD 5. Appears also at P8 of the M/B as Address/Data Line 5 for the SAR-PHY tool.
76	PC13	I/O, X	MPC850 PC13/SAR-PHY $\overline{\text{READ}}$.Appears also at P8 of the M/B as SAR-PHY $\overline{\text{READ}}$ as support to the SAR-PHY tool.
77	E_TENA	I/O, H	Ethernet port Transmit Enable. Also PB18/RTS2. Connected to the SCC2's RTS~ signal. When active, transmit is enabled via the MC68160 EEST on the M/B. When the ethernet port is disabled via BCSR1, may be used off-board for any alternate function. Appears also at P8 of the M/B.
78	GND		
79	N.C.		
80			
81			
82	ETHEN~	O, L	Ethernet Port Enable. Connected to BCSR1. See TABLE 4-10. "BCSR1 Description" on page 49 of the MPC8XXFADS User's Manual.
83	N.C.		

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TABLE 5-10. PM3 Interconnect Signals

Pin No.	*Signal Name*	*Attribute*	*Description*
84	IRD_EN~	O, L	Infra-Red Enable. Connected to BCSR1. See TABLE 4-10. "BCSR1 Description" on page 49 of the MPC8XXFADS User's Manual.
85	USBTXP	I/O, X	USBTXP/SAR-PHY AD2. USB Positive transmit signal (differential) also MPC PI/O port C 7. Appears also at P8 of the M/B as SAR-PHY Address/Data Line 2 to support the SAR-PHY tool.
86	GND		
87			
88	N.C.		
89	PA5	I/O, X	MPC PI/O port A 5/SAR-PHY L1TCLKA. Appears also at P8 as E1/T1 L1TCLKA.
90	GND		
91			
92	TMS	I, X	JTAG port Test Mode Select input. Used to select test through the JTAG port. Pulled-up on the M/B but otherwise not used on the FADS.
93	PB16	I/O, X	MPC PI/O port B 16/SAR-PHY AD4. Appears also at P8 of the M/B as SAR-PHY Address/Data Line 4 for the SAR-PHY tool.
94	TRST~	O, L	JTAG port Reset. Pulled down on the M/B with a zero ohm resistor, so that the JTAG logic is constantly reset. Otherwise unused on the FADS.
95	PC12	I/O, X	MPC PI/O port C 12/SAR-PHY TXCAV. Appears also at P8 of the M/B as UTOPIA TXCAV for the SAR-PHY tool.
96	RS_EN1~	I, L	RS232 port 1 Enable. Connected to BCSR1. See TABLE 4-10. "BCSR1 Description" on page 49 in the MPC8XXFADS User's Manual.
97	RSDTR2~	I/O, X	MPC PI/O port B 22/SAR-PHY ALE. Appears also at P8 of the M/B as ALE for the SAR-PHY tool (see pin no. 44).
98	N.C.		
99	N.C.		
100	PC4	I/O, X	MPC PI/P port C 4/SAR-PHY L1RSYNCA. Appears also at P8 of the M/B as E1/T1 L1RSYNCA for the SAR-PHY tool.
101	GND		
102	RS_EN2~	O, L	RS232 port 2 Enable. Generated by BCSR1. Used in conjunction with IRD_EN~ and ETH_EN~ to select and enable a multiplexer over RXD2 signal. See TABLE 4-10. "BCSR1 Description" on page 49 of the M/B and FIGURE 4-1 "SCC2 Connection Scheme" on page 12.

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TABLE 5-10. PM3 Interconnect Signals

Pin No.	*Signal Name*	*Attribute*	*Description*
103	PD3	I/O, X	MPC's PD3. Appears also at P8 of the M/B as UTOPIA SOC for the SAR-PHY tool.
104	GND		
105			
106	PD4	I/O, X	MPC850's PD4. Appears also at P8 of the M/B as UTOPIA Data Bus bit 7 for the SAR-PHY tool.
107	PD5	I/O, X	MPC850's PD5. Appears also at P8 of the M/B as UTOPIA Data Bus bit 6 for the SAR-PHY tool.
108	GND		
109			
110	PD6	I/O, X	MPC850's PD6. Appears also at P8 of the M/B as UTOPIA Data Bus bit 5 for the SAR-PHY tool.
111	VDORST~	I,X	Reserved. Unused with this daughter board.
112	VDOEXTCK	I, X	Reserved. Unused with this daughter board.
113	PD7	I/O, X	MPC850's PD7. Appears also at P8 of the M/B as UTOPIA Data Bus bit 4 for the SAR-PHY tool.
114	PD8	I/O, X	See pin no. 8.
115	PD9	I/O, X	MPC's PD9. Appears also at P8 of the M/B as UTOPIA CLOCK for the SAR-PHY tool.
116	PD10	I/O, X	MPC's PD10. Appears also at P8 of the M/B as UTOPIA $\overline{\text{TXENB}}$ for the SAR-PHY tool.
117	PD11	I/O, X	MPC's PD11. Appears also at P8 of the M/B as UTOPIA $\overline{\text{RXENB}}$ for the SAR-PHY tool.
118	PD12	I/O, X	MPC850's PD12. Appears also at P8 of the M/B as UTOPIA Data Bus bit 3 for the SAR-PHY tool.
119	PD13	I/O, X	MPC850's PD13. Appears also at P8 of the M/B as UTOPIA Data Bus bit 2 for the SAR-PHY tool.
120	PD14	I/O, X	MPC850's PD14. Appears also at P8 of the M/B as UTOPIA Data Bus bit 1 for the SAR-PHY tool.
121	PD15	I/O, X	MPC850's PD15. Appears also at P8 of the M/B as UTOPIA Data Bus bit 0 for the SAR-PHY tool.
122	GND		
123			
124	ETHLOOP	I, H	Ethernet Transceiver Diagnostic Loop-Back Control. Generated by BCSR4. See TABLE 4-23. "BCSR4 Description" on page 57 of the MPC8XXFADS User's Manual. Not used on this D/B, just passed on to the expansion connectors.

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TABLE 5-10. PM3 Interconnect Signals

Pin No.	*Signal Name*	*Attribute*	*Description*
125	TPFLDL~	I, L	Twisted Pair Full Duplex. Allows for full-duplex operation over the Ethernet Twisted-Pair channel. See TABLE 4-23. "BCSR4 Description" on page 57 of the MPC8XXFADS User's Manual. Not used on this D/B, just passed on to the expansion connectors.
126	TPSQEL~	I, L	Twisted Pair Signal Quality Error Test Enable. See TABLE 4-23. "BCSR4 Description" on page 57 of the MPC8XXFADS User's Manual. Not used on this D/B, just passed on to the expansion connectors.
127	MDM_AUD~	I, L	Not used on this board.
128	MODEMEN~	I, L	Not used on this board.
129	N.C.		
130	GND		
131	N.C.		
132			
133	VCC		
134			
135			
136			
137			
138			
139			
140			

TABLE 5-11. PM4 Interconnect Signals

Pin No.	*Signal Name*	*Attribute*	*Description*
1	GND		
2	D31	I/O, X	MPC's Data line 31.
3	GND		
4	D30	I/O, X	MPC's Data line 30.
5	GND		
6	D29	I/O, X	MPC's Data line 29.
7	GND		
8	D28	I/O, X	MPC's Data line28.
9	GND		
10			
11			
12	D27	I/O, X	MPC's Data line 27.
13	GND		
14	D26	I/O, X	MPC's Data line 26.
15	GND		
16	D25	I/O, X	MPC's Data line 25.
17	GND		
18	D24	I/O, X	MPC's Data line 24.
19	GND		
20			
21			
22	D23	I/O, X	MPC's Data line 23.
23	GND		
24	D22	I/O, X	MPC's Data line 22.
25	GND		
26	D21	I/O, X	MPC's Data line 21.
27	GND		
28	D20	I/O, X	MPC's Data line 20.

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TABLE 5-11. PM4 Interconnect Signals

Pin No.	*Signal Name*	*Attribute*	*Description*
29	GND		
30			
31			
32	D19	I/O, X	MPC's Data line 191.
33	GND		
34	D18	I/O, X	MPC's Data line 18.
35	GND		
36	D17	I/O, X	MPC's Data line 17.
37	GND		
38	D16	I/O, X	MPC's Data line 16.
39	GND		
40			
41			
42	D15	I/O, X	MPC's Data line 15.
43	GND		
44	D14	I/O, X	MPC's Data line 14.
45	GND		
46	D13	I/O, X	MPC's Data line 13.
47	GND		
48	D12	I/O, X	MPC's Data line 12.
49	GND		
50			
51			
52	D11	I/O, X	MPC's Data line 11.
53	GND		
54	D10	I/O, X	MPC's Data line 10.
55	GND		
56	D9	I/O, X	MPC's Data line 9.
57	GND		
58	D8	I/O, X	MPC's Data line 8.

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TABLE 5-11. PM4 Interconnect Signals

Pin No.	Signal Name	Attribute	Description
59	GND		
60			
61			
62	D7	I/O, X	MPC's Data line 7.
63	GND		
64	D6	I/O, X	MPC's Data line 6.
65	GND		
66	D5	I/O, X	MPC's Data line 5.
67	GND		
68	D4	I/O, X	MPC's Data line 4.
69	GND		
70			
71			
72	D3	I/O, X	MPC's Data line 3.
73	GND		
74	D2	I/O, X	MPC's Data line 2.
75	GND		
76	D1	I/O, X	MPC's Data line 1.
77	GND		
78	D0	I/O, X	MPC's Data line 0.
79	GND		
80			
81	DRMH_W~	I, L	Dram Half Word. Sets the Dram to 16 bit data bus width. Not used on this D/B, just passed on to the expansion connectors. See TABLE 4-10. "BCSR1 Description" on page 49 of the MPC8XXFADS User's Manual.
82	DRAMEN~	O, L	Dram Enable. Enables Dram to the FADS memory map. Not used on this D/B, just passed on to the expansion connectors. See TABLE 4-10. "BCSR1 Description" on page 49 of the MPC8XXFADS User's Manual.
83	FCFGEN~	O, L	Flash Configuration Enable. Allows for Hard Reset Configuration to be obtained from the Flash memory provided that this option is supported by the MPC. Not used on this D/B, just passed on to the expansion connectors. See TABLE 4-10. "BCSR1 Description" on page 49 of the MPC8XXFADS User's Manual.

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TABLE 5-11. PM4 Interconnect Signals

Pin No.	Signal Name	Attribute	Description
84	F_EN~	I, L	Flash Enable. Enables the Flash memory to the FADS memory map. Not used on this board, just passed on to PX4. See TABLE 4-10. "BCSR1 Description" on page 49 of the MPC8XXFADS User's Manual.
85	SDRAMEN	I, H	Sdram Enable. Enables the Synchronous Dram to the FADS memory map. Not used on this board, just passed on to PX4. See TABLE 4-10. "BCSR1 Description" on page 49 of the MPC8XXFADS User's Manual.
86	BCSREN~	I, L	BCSR Enable. Enables the BCSR to the FADS memory map. Not used on this board, just passed on to the PX4. See TABLE 4-10. "BCSR1 Description" on page 49 of the MPC8XXFADS User's Manual.
87	USBVCC0	I, X	USB Power. Drives VCC on the USB bus when the MPC850 functions as USB host. Available also on PX4. See TABLE 4-23. "BCSR4 Description" on page 57 of the MPC8XXFADS User's Manual.
88	PCCEN~	I, L	PC- Card Enable. Enables the PC-Card to be accessed by the FADS. Available also on PX4. See TABLE 4-10. "BCSR1 Description" on page 49 of the MPC8XXFADS User's Manual.
89	EXTOLI0	O, X	External Tool Identification 0. Connected to BCSR2. Not used on this board, just passed from PX4. See TABLE 4-13. "BCSR2 Description" on page 52 of the MPC8XXFADS User's Manual.
90	SGLAMP~	I, L	Signaling Lamp. Used for misc. s/w signaling purpose. Not used on this board, just passed on to the PX4. See TABLE 4-23. "BCSR4 Description" on page 57 of the MPC8XXFADS User's Manual.
91	EXTOLI2	O, X	External Tool Identification 2. Connected to BCSR2. Not used on this board, just passed from PX4. See TABLE 4-13. "BCSR2 Description" on page 52 of the MPC8XXFADS User's Manual.
92	USBVCC1	O, X	Reserved Signal for USB Power control. Not used on this board, just passed on to the PX4. See TABLE 4-23. "BCSR4 Description" on page 57 of the MPC8XXFADS User's Manual.
93	DBREV0	O, X	Daughter Board Revision Code Signal 0. The MSB of the D/B revision Code. Available also on PX4. see TABLE 4-13. "BCSR2 Description" on page 52 of the MPC8XXFADS User's Manual.
94	EXTOLI1	O, X	External Tool Identification 1. Connected to BCSR2. Not used on this board, just passed from PX4. See TABLE 4-13. "BCSR2 Description" on page 52 of the MPC8XXFADS User's Manual.
95	DBREV2	O, X	Daughter Board Revision Code Signal 2. The LMSB of the D/B revision Code. Available also on PX4. See TABLE 4-13. "BCSR2 Description" on page 52 of the MPC8XXFADS User's Manual.

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TABLE 5-11. PM4 Interconnect Signals

Pin No.	*Signal Name*	*Attribute*	*Description*
96	EXTOLI3	O, X	External Tool Identification 3. Connected to BCSR2. Not used on this board, just passed from PX4. See TABLE 4-13. "BCSR2 Description" on page 52 of the MPC8XXFADS User's Manual.
97	BCSR3R1	O, X	Reserved signal 1 in BCSR3. Available also on PX4. See TABLE 4-19. "BCSR3 Description" on page 55 of the MPC8XXFADS User's Manual.
98	DBREV1	O, X	Daughter Board Revision Code Signal 1. Available also on PX4. See TABLE 4-13. "BCSR2 Description" on page 52 of the MPC8XXFADS User's Manual.
99	DBID1	O, X	Daughter Board ID Code 1. Part of the field which designates the type of daughter board connected. Available also on PX4. See TABLE 4-19. "BCSR3 Description" on page 55 of the MPC8XXFADS User's Manual.
100	BCSR3R0	O, X	Reserved signal 0 in BCSR3. Available also on PX4. See TABLE 4-19. "BCSR3 Description" on page 55 of the MPC8XXFADS User's Manual.
101	DBID3	O, X	Daughter Board ID Code 3. Part of the field which designates the type of daughter board connected. Available also on PX4. See TABLE 4-19. "BCSR3 Description" on page 55 of the MPC8XXFADS User's Manual.
102	DBID0	O, X	Daughter Board ID Code 0. Part of the field which designates the type of daughter board connected. Available also on PX4. See TABLE 4-19. "BCSR3 Description" on page 55 of the MPC8XXFADS User's Manual.
103	DBID5	O, X	Daughter Board ID Code 5. Part of the field which designates the type of daughter board connected. Available also on PX4. See TABLE 4-19. "BCSR3 Description" on page 55 of the MPC8XXFADS User's Manual.
104	DBID2	O, X	Daughter Board ID Code 2. Part of the field which designates the type of daughter board connected. Available also on PX4. See TABLE 4-19. "BCSR3 Description" on page 55 of the MPC8XXFADS User's Manual.
105	BCSR3R13	O, X	Reserved signal 13 in BCSR3. Available also on PX4. See TABLE 4-19. "BCSR3 Description" on page 55 of the MPC8XXFADS User's Manual.
106	DBID4	O, X	Daughter Board ID Code 4. Part of the field which designates the type of daughter board connected. Available also on PX4. See TABLE 4-19. "BCSR3 Description" on page 55 of the MPC8XXFADS User's Manual.
107	CHINS~	O, L	Chip In Socket. When this signal is active (low), FADS logic is being noticed that the evaluated MPC8XX resides in its socket. If inactive, either the MPC is out of socket or a daughter board is not connected, in which case the FADS becomes a debug station. Available also on PX4.

Support Information

TABLE 5-11. PM4 Interconnect Signals

Pin No.	*Signal Name*	*Attribute*	*Description*
108	GND		
109			
110	N.C.		
111			
112	GND		
113			
114	N.C.		
115			
116	GND		
117			
118	N.C.		
119			
120	GND		
121			
122	N.C.		
123			
124	GND		
125			
126	N.C.		
127			
128	GND		
129			
130	N.C.		
131			
132	GND		
133			
134	N.C.		
135			
136	GND		
137			

Support Information

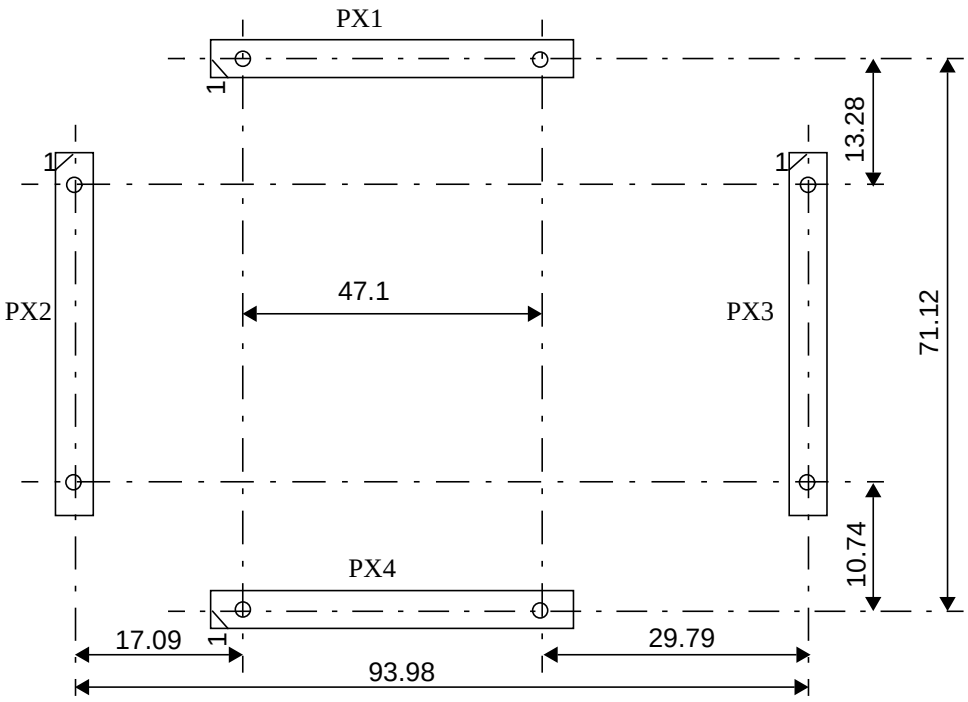
TABLE 5-11. PM4 Interconnect Signals

Pin No.	Signal Name	Attribute	Description
138	N.C.		
139			
140	GND		

5•1•4 PX1 - PX4 Hardware Expansion Connectors

These connectors are receptacle inter-board connectors made by Molex. They are identical to those exist on the MPC8XXFADS mother board. Their mechanical assembly is similar as well and is shown in FIGURE 5-2 "Expansion Connectors Mechanical Assembly" below:

FIGURE 5-2 Expansion Connectors Mechanical Assembly



In principle, the expansion connectors are identical in signals‘ assignment to the mother boards connectors. However, there is a difference mainly between PM3 and PX3, resulting from the difference between the various members of the 8XX family. Therefore, in the following tables only the differences are docu-

mented per each connector pair - PM1 - PX1...

TABLE 5-12. PX1 - PM1 Interconnect Signals' Differences

Pin No.	*Signal Name*	*Attribute*	*Description*
			No Difference

TABLE 5-13. PX2 - PM2 Interconnect Signals' Differences

Pin No.	*Signal Name*	*Attribute*	*Description*
76	EXTCLK	O, X	External Clock. 4MHz clock generator output, the input clock to the MPC.

TABLE 5-14. PX3 - PM3 Interconnect Signals' Differences

Pin No.	*Signal Name*	*Attribute*	*Description*
1	USBRXD	O, X	USB port receive data. PA15/USBRXD. This place on the connectors is reserved for SCC1's RXD line, which is this signal for MPC850. When the USB port is disabled via BCSR4, may be used for any alternate function.
5	USBOE~	O, L	USB Port Output Enable. PC14/USBOE~. This place is reserved for SCC1's TXD output, normally residing on PA14. When this signal is active (low) the USB transceiver is open to the USB bus. When inactive, the transceiver is in receive mode.
8	USBRXP	I,X	One of the USB receive lines. PC11/USBRXP/SAR-PHY AD 7.
9	RXD2	I/O, X	PA13/RXD2. SCC2 receive data. Mux'ed between the Ethernet, InfraRed and RS232 Port #2. When neither of these port is enabled via BCSR1, may be used for any alternate function.
14	USBRXN	I,X	One of the USB receive lines. PC10/USBRXP/SAR-PHY AD3.
20	USBTXP	O,X	One of the USB transmit lines. PC7/USBTXP/SAR-PHY AD 2.
21	PA9	I/O, X	PA9/ E1/T1 L1TXDA.
23	PA8	I/O, X	PA8/ E1/T1 L1RXDA.
26	PC13	I/O, X	PC13/SAR-PHY $\overline{\text{READ}}$.
27	PA7	I/O, X	PA7/ E1/T1 L1RCLKA.
33	PB31	I/O, X	PB31/ E1/T1 Chip Select.
45	PC14	I/O, X	PC14/ SAR-PHY $\overline{\text{WRITE}}$.
53	PC12	I/O, X	PC12/ SAR-PHY UTOPIA TXCAV.
57	PA5	I/O, X	PA5/ E1/T1 L1TCLKA.
60	ETHTCK	I/O, X	PA4/ETHTCK/TOUT2.

Support Information

TABLE 5-14. PX3 - PM3 Interconnect Signals' Differences

Pin No.	*Signal Name*	*Attribute*	*Description*
76	E_TENA	I/O, X	PB18/E_TENA.
77	PB19	I/O, X	PB19/SAR-PHY AD0.
98	PC4	I/O, X	PC4/ E1/T1 L1RSYNCA.
99	PC5	I/O, X	PC5/ E1/T1 L1TSYNCA.
100	USBTXN	I/O, X	PC6/USBTXN/SAR-PHY AD6.

TABLE 5-15. PX4 - PM4 Interconnect Signals Difference

Pin No.	*Signal Name*	*Attribute*	*Description*
-		-	No Difference.

5•1•5 MPC8XXFADS's P8 - Serial Ports' Expansion Connector

P8 is a 96 pin, 90^0, DIN 41612 connector, which allows for convenient expansion of the MPC's serial ports. Although this connector resides on the mother board it is documented here, this, since it's signal assignment is unique per each MPC8XX.

Support Information

Note:

The contents of TABLE 5-16. "MPC8XXFADS's P8 - Interconnect Signals" below, might conflict with MPC8XXFADS's schematic page 14. This since, that the schematic page is named in MPC821/860 terms. In such case, this table overrides!

TABLE 5-16. MPC8XXFADS's[a] P8 - Interconnect Signals

Pin No.	*Signal Name*	*Attribute*	*Description*
A1	ETHRX	I/O	Ethernet port receive data. See PM3(1)
A2	ETHTX	I/O	Ethernet Port transmit data. See PM3(5,11,42)
A3	IRDRXD	I/O	IrDA port receive data. See PM3(9).
A4	IRDTXD	I/O	IrDA port transmit data. See PM3(5,11,42)
A5	UTOPIA $\overline{\text{RXENB}}$	I/O	UTOPIA $\overline{\text{RXENABLE}}$. See PM3(117)
A6	UTOPIA $\overline{\text{TXENB}}$	I/O	UTOPIA $\overline{\text{TXENABLE}}$. See PM3(116)
A7	UTOPIA CLOCK	I/O	UTOPIA CLOCK. See PM3(115)
A8	PD8	I/O	PD8/SAR-PHY AD1. See PM3(114)
A9	ETHTCK	I/O	Ethernet port transmit clock. See PM3(27).
A10	ETHRCK	I/O	Ethernet port receive clock. See PM3(29)
A11	N.C.	-	
A12	TOUT2	I/O	$\overline{\text{TOUT2}}$/PA4. See PM3(60)
A13	USBRXN	I/O	USBRXN/SAR-PHY AD3. See PM(71).
A14	PA7	I/O	PA7/ E1/T1 L1RCLKA. See PM3(74).
A15	USBTXP	I/O	PC7/USBTXP/SAR-PHY AD2. See PM(85).
A16	PA5	I/O	PA5/ E1/T1 L1TCLKA. See PM(89).
A17	VCC	-	
A18	PA9	I/O	PA9/ E1/T1 L1TXDA. See PM3(15).
A19	PA8	I/O	PA8/ E1/T1 L1RXDA. See PM3(17).
A20	USBRXP	I/O	PC11/USBRXP/SAR-PHY AD7. See PM3(21).
A21	USBTXN	I/O	PC6/USBTXN/SAR-PHY AD6. See PM3(23)
A22	GND	-	
A23	GND	-	
A24	IRQ7~	I, L	See PM2(130)
A25	FRZ	I/O, H	See PM2(24).
A26	ETHEN~	O, L	See PM3(82)

Support Information

TABLE 5-16. MPC8XXFADS's[a] P8 - Interconnect Signals

Pin No.	*Signal Name*	*Attribute*	*Description*
A27	N.C.	-	
A28	IRQ2~	I, L	RSV/IRQ2. See PM2(26).
A29	IRQ1~	I, L	See PM2(126).
A30	NMI~	I, L	See PM2(134).
A31	RS_EN1~	O,L	See PM3(96).
A32	GND	-	
B1	N.C.		
B2	PB30	I/O	PB30/ E1/T1 SPI_CLOCK. See PM3(35).
B3	PB29	I/O	PB29/ E1/T1 SPI_IN. See PM3(37).
B4	PB28	I/O	PB28/ E1/T1 SPI_OUT. See PM3(51).
B5	PB27	I/O	PB27/SAR-PHY CS. See PM3(50).
B6	PB26	I/O	PB26/SAR-PHY RESET_BOARD. See PM3(54).
B7	RSTXD1	I/O	PB25/RS232 port 1 TXD. See PM3(38).
B8	RSRXD1	I/O	PB24/RS232 port 1 RXD. See PM3(39).
B9	RSDTR1~	I/O	PB23/RS232 port 1 DTR. See PM3(40).
B10	RSDTR2~	I/O	PB22/RS232 port 2 DTR/SAR-PHY ALE. See PM3(44).
B11	TXD2	I/O	PA12/RS232 port 2 TXD. See PM3(5,11,42).
B12	RSRXD2	I/O	RS232 port 2 RXD. See PM3(43)
B13	E_TENA	I/O	PB18/Ethernet TENA. See PM3(77).
B14	PC13	I/O	PC13/SAR-PHY READ. See PM3(76).
B15	PB17	I/O	PB17/SAR-PHY AD5. See PM3(75).
B16	PB16	I/O	PB16/SAR-PHY AD4. See PM3(93).
B17	PC12	I/O	PC12/UTOPIA TXCAV. See PM(95).
B18	RSDTR2~	I/O	PB22/RS232 port 2 DTR/SAR-PHY ALE. See PM3(97).
B19	GND	-	
B20	BINPAK~	I/O	PC15/PCMCIA BINPAK/UTOPIA RXCAV. See PM3(34).
B21	N.C.	I/O	See PM3(45).
B22	PB31	I/O	PB31/ E1/T1 Chip Select. See PM3(26).
B23	PC14	I/O	PC14/SAR-PHY WRITE. See PM3(53).
B24	E_CLSN	I/O	PC9/Ethernet CLSN. See PM3(61).
B25	E_RENA	I/O	PC8/Ethernet RENA. See PM3(62).

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TABLE 5-16. MPC8XXFADS's[a] P8 - Interconnect Signals

Pin No.	*Signal Name*	*Attribute*	*Description*
B26	PD8	I/O	PD8/SAR-PHY AD1. See PM3(8).
B27	PB19	I/O	PB19/SAR-PHY AD0. See PM3(14).
B28	PC5	I/O	PC5/L1TSYNCA. See PM3(20).
B29	PC4	I/O	PC4/L1RSYNCA. See PM3(100).
B30	N.C.	I/O	See PM3(99).
B31	N.C.	I/O	See PM3(98).
B32	GND	-	
C1	VCC		
C2			
C3			
C4			
C5			
C6	RS_EN2~	O, L	See PM3(102).
C7	GND		
C8			
C9			
C10			
C11			
C12			
C13			
C14			
C15	PD15	I/O	PD15/UTOPIA Data bit 0. See PM3(121).
C16	PD14	I/O	PD14/UTOPIA Data bit 1. See PM3(120).
C17	PD13	I/O	PD13/UTOPIA Data bit 2. See PM3(119).
C18	PD12	I/O	PD12/UTOPIA Data bit 3. See PM3(118).
C19	PD7	I/O	PD7/UTOPIA Data bit 4. See PM3(113).
C20	PD6	I/O	PD6/UTOPIA Data bit 5. See PM3(110).
C21	VCC	-	
C22	HRESET~	I/O, L	See PM2(84).
C23	SRESET~	I/O, L	See PM2(80).
C24	N.C.	-	Not Connected

Support Information

TABLE 5-16. MPC8XXFADS's[a] P8 - Interconnect Signals

Pin No.	*Signal Name*	*Attribute*	*Description*
C25	VCC	-	
C26	PD3	I/O	PD3/UTOPIA SOC. See PM3(103)
C27	VPPIN	I/O	+12V input for PCMCIA flash programming. Parallel to P7 of the MPC8XXFADS.
C28			
C29	GND	-	
C30	PD4	I/O	PD4/UTOPIA Data bit 7. See PM3(106).
C31	GND	-	
C32	PD5	I/O	PD5/UTOPIA Data bit 6. See PM3(107).

a. When connected to this board - the MPC850SARDB.

TABLE 5-17. "MPC850SARDB Connections to the SAR-PHY Tool" on page 57 bellow shows the connections paths from P8 on the MPC8xxFADS M/B to the MPC850SAR D/B.

TABLE 5-17. MPC850SARDB Connections to the SAR-PHY Tool

I/O	DB-PXx	DB-PMx	MB-PDx	MB-P8	Description
PORT A					
PA15	PX3 - 1				USB RxD on DB
PA14	PX3 - 5				USB $\overline{OE}$ on DB
PA13	PX3 - 9				Ethernet InfraRed Rs232#2 RxD2 on DB
		PM3 - 9	PD3 - 9	A3	InfraRed RxD2 on MB
		PM3 - 1	PD3 - 1	A1	Ethernet RxD2 on MB
		PM3 - 43	PD3 - 43	B12	RS232#2 RxD2 on MB
PA12	PX3 - 11	PM3 - 5,11,42	PD3 - 11	A4	InfraRed TxD2 on MB
		PM3 - 5,11,42	PD3 - 42	B11	RS232#2 TxD2 on MB
		PM3 - 5,11,42	PD3 - 5	A2	Ethernet TxD2 on MB
PA9	PX3 - 21	PM3 - 15	PD3 -15	A18	E1/T1 L1TxDA
PA8	PX3 - 23	PM3 - 17	PD3 - 17	A19	E1/T1 L1RxDA
PA7	PX3 - 27	PM3 - 74	PD3 - 74	A14	E1/T1 L1RCLKA,
PA6	PX3 - 29	PM3 - 29	PD3 - 29	A10	Ethernet RxCLK
PA5	PX3 - 57	PM3 - 89	PD3 - 89	A16	E1/T1 L1TCLKA

TABLE 5-17. MPC850SARDB Connections to the SAR-PHY Tool

I/O	DB-PXx	DB-PMx	MB-PDx	MB-P8	Description
PA4	PX3 - 60	PM3 - 27	PD3 - 27	A9	Ethernet TxCLK
		PM3 - 60	PD3 - 60	A12	TOUT2 - E1/T1 L1TSYNCA (through J3)
PORT B					
PB31	PX3 - 33	PM3 - 26	PD3 - 26	B22	E1/T1 Chip Select
PB30	PX3 - 35	PM3 - 35	PD3 - 35	B2	E1/T1 SPI_CLK
PB29	PX3 - 37	PM3 - 37	PD3 - 37	B3	E1/T1 SPI_IN
PB28	PX3 - 51	PM3 - 51	PD3 - 51	B4	E1/T1 SPI_OUT
PB27	PX3 - 50	PM3 - 50	PD3 - 50	B5	SAR-PHY $\overline{\text{PHYCS}}$
PB26	PX3 - 54	PM3 - 54	PD3 - 54	B6	SAR-PHY $\overline{\text{RST\_BRD}}$
PB25	PX3 - 38	PM3 - 38	PD3 - 38	B7	RS232#1 TxD1
PB24	PX3 - 39	PM3 - 39	PD3 - 39	B8	RS232#1 RxD1
PB23	PX3 - 40	PM3 - 40	PD3 - 40	B9	RS232#1 $\overline{\text{DTR1}}$
PB22	PX3 - 44	PM3 - 44,97	PD3 - 44,97	B10	RS232#2 $\overline{\text{DTR2}}$, SAR-PHY ALE
PB19	PX3 - 77	PM3 - 14	PD3 - 14	B27	SAR-PHY AD0
PB18	PX3 - 76	PM3 - 77	PD3 - 77	B13	Ethernet TENA
PB17	PX3 - 75	PM3 - 75	PD3 - 75	B15	SAR-PHY AD5
PB16	PX3 - 93	PM3 - 93	PD3 - 93	B16	SAR-PHY AD4
PORT C					
PC15	PX3 - 34	PM3 - 34	PD3 - 34	B20	UTOPIA RxCAV, PCMCIA $\overline{\text{BINPAK}}$
PC14	PX3 - 45	PM3 - 53	PD3 - 53	B23	SAR-PHY $\overline{\text{PHYWR}}$
PC13	PX3 - 26	PM3 - 76	PD3 - 76	B14	SAR-PHY $\overline{\text{PHYRD}}$
PC12	PX3 - 53	PM3 - 95	PD3 - 95	B17	UTOPIA TxCAV
PC11	PX3 - 8	PM3 - 21	PD3 - 21	A20	USB RxP, SAR-PHY AD7
PC10	PX3 - 14	PM3 - 71	PD3 - 71	A13	USB RxN, SAR-PHY AD3
PC9	PX3 - 61	PM3 - 61	PD3 - 61	B24	Ethernet CLSN
PC8	PX3 - 62	PM3 - 62	PD3 - 62	B25	Ethernet RENA
PC7	PX3 - 20	PM3 - 85	PD3 - 85	A15	USB TxP, SAR-PHY AD2
PC6	PX3 - 100	PM3 - 23	PD3 - 23	A21	USB TxN, SAR-PHY AD6
PC5	PX3 - 99	PM3 - 20	PD3 - 20	B28	E1/T1 L1TSYNCA
PC4	PX3 - 98	PM3 - 100	PD3 - 100	B29	E1/T1 L1RSYNCA
PORT D					

TABLE 5-17. MPC850SARDB Connections to the SAR-PHY Tool

I/O	DB-PXx	DB-PMx	MB-PDx	MB-P8	Description
PD15	PX3 - 121	PM3 - 121	PD3 - 121	C15	UTOPIA B0
PD14	PX3 - 120	PM3 - 120	PD3 - 120	C16	UTOPIA B1
PD13	PX3 - 119	PM3 - 119	PD3 - 119	C17	UTOPIA B2
PD12	PX3 - 118	PM3 - 118	PD3 - 118	C18	UTOPIA B3
PD11	PX3 - 117	PM3 - 117	PD3 - 117	A5	UTOPIA $\overline{\text{RxENB}}$
PD10	PX3 - 116	PM3 - 116	PD3 - 116	A6	UTOPIA $\overline{\text{TxENB}}$
PD9	PX3 - 115	PM3 - 115	PD3 - 115	A7	UTOPIA CLOCK
PD8	PX3 - 114	PM3 - 8	PD3 - 8	B26	SAR-PHY AD1
PD7	PX3 - 113	PM3 - 113	PD3 - 113	C19	UTOPIA B4
PD6	PX3 - 110	PM3 - 110	PD3 - 110	C20	UTOPIA B5
PD5	PX3 - 107	PM3 - 107	PD3 - 107	C32	UTOPIA B6
PD4	PX3 - 106	PM3 - 106	PD3 - 106	C30	UTOPIA B7
PD3	PX3 - 103	PM3 - 103	PD3 - 103	C26	UTOPIA SOC

5•2 MPC850SARDB Part List

In this section the MPC850SARDB bill of material is listed according to their reference designation.

TABLE 5-18. MPC850SARDB Part List

Reference Designation	*Part Description*	*Manufacturer*	*Part #*
C1 C2 C3 C4 C5 C6 C8 C9 C10 C11 C13 C15 C16 C17 C19 C20 C21 C22 C23 C24 C25 C30 C32 C33	Capacitor 0.1µF,16V, 10%, SMD 0603, Ceramic	AVX	0603YC104KAT2A
C7 C29 C31	Capacitor 10µF, 20V, 10%, SMD Size C, Tantalum	SIEMENS	B45196-H5106-K309
C12	Capacitor 100µF, 10V, 10%, SMD Size D, Tantalum	SIEMENS	B45196-H2107-K10
C14	Capacitor 1µF, 25V, 10%, SMD Size A, Tantalum	SIEMENS	B45196-H5105-K109
C18 C26	Capacitor 10pF, 50V 10%, COG, SMD 1206, Ceramic	AVX	AV12065A100KAT00J
C27	Capacitor 4700pF, 50V, 10%, SMD 1206, Ceramic	AVX	AV12065C 472K A700J
C28	Capacitor 0.68µF, 20V, 10%, SMD, Size A, Tantalum	SIEMENS	B45196-E4684-K109

Support Information

TABLE 5-18. MPC850SARDB Part List

Reference Designation	*Part Description*	*Manufacturer*	*Part #*
D1 D2	Diode SMD	Motorola	LL4004G
H1 H2 H3	Gnd Bridge, Gold Plated	PRECIDIP	999-11-112-10
J1 J2 J3	Jumper Header, 3 Pole with Fabricated Jumper	MOLEX	87156-0303
J4	Jumper, Soldered.	PRECIDIP	999-19-310-00
L1	Inductor 8.2 mHy	BOURNS	PT12133
LD1	Led Green SMD	SIEMENS	LG T670-HK
LD2 LD3	Led Yellow SMD	SIEMENS	LY T670-HK
P1 P2 P5 P6 P7 P8	Connector 38 pin, Receptacle MICTOR.	AMP	2-767004-2
P3	Connector 4 pin, Female, USB Type B	AMP	787780-1
P4	Connector 4 pin, Female USB type A	AMP	787616-1
PM1 PM2 PM3 PM4	Connector Inter-board, 7mm Height, 140 pin, Plug, SMD	MOLEX	53481-1409
PX1 PX2 PX3 PX4	Connector Inter-board 140 pin, Receptacle, SMD	MOLEX	52760-1409
R1 R2	Resistor 1.5 kΩ, 1%, SMD 1206, 1/8W	RODERSTEIN	D25 01K5 FCS
R3 R4 R5 R23	Resistor 124 KΩ, 5%, SMD 1206, 1/8W	RODERSTEIN	D25 124K FCS
R6 R7	Resistor 150 Ω, 5% SMD 1206, 1/8W	RODERSTEIN	D25 150RFCS
R8	Resistor 75 Ω, 5%, SMD 1206, 1/8W	RODERSTEIN	D25075RJCS
R9	Resistor 47 KΩ, 1%, SMD 1206, 1/8W	RODERSTEIN	D25047KFCS
R10 R13	Resistor 10 KΩ, 1%, SMD 1206, 1/8W	RODERSTEIN	D25010KFCS
R11 R22	Resistor 0 Ω, 1%, SMD 0603, 0.1W	RODERSTEIN	D11 000RFCS
R12 R14 R15 R16 R17 R20 R21	Resistor 390 Ω, 1%, SMD 0603	RODERSTEIN	D11 390RFCS
R18	Resistor 200 KΩ, 1%, SMD 1206, 1/8W	RODERSTEIN	D25 200K FCS
R19	Resistor 20 MΩ, 5%, SMD 1206, 1/4W	RODERSTEIN	D25 020MJCS

Support Information

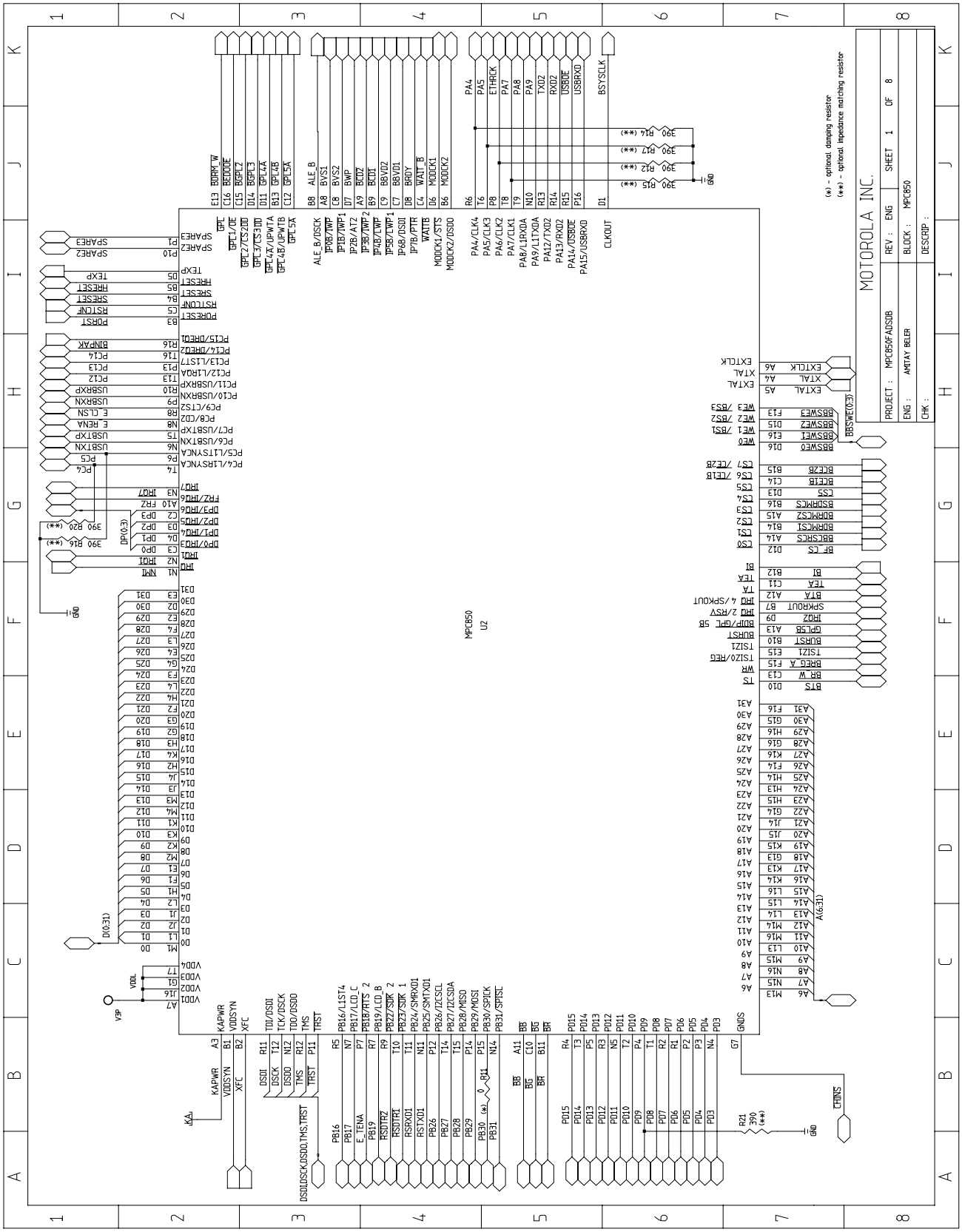
TABLE 5-18. MPC850SARDB Part List

Reference Designation	*Part Description*	*Manufacturer*	*Part #*
RN1 RN2 RN3 RN4 RN5	Resistor Network 75 Ω, 5%, 4 resistors, 8 pin.	DALE	CRA06S0803750JR
T1 T2 T3 T4 T5	Transistor TMOS, Dual, 3A	Motorola	MMDF3N03HD
U1	4 MHz Clock generator. 3.3V, CMOS levels.	M-TRON	MH14FAD 3.3V 4.00MHz
U2	MPC850, 16 X 16, 256 pin BGA.	Motorola	XPC850SRZT50A
U3	Quad Low Voltage CMOS AND Gate.	Motorola	74LCX08D
U4	8 -> 1 Mux with tri-state output.	Motorola	74ACT251D
U5	USB transceiver	PHILIPS	PDIUSBP11AD
U6 U9	Quad CMOS buffer with individual Output Enable.	Motorola	74ACT125D
U7	Voltage level detector. Range 1.795V to 2.005V. O.D. output.	Seiko	S-8051HN-CD-X
U8	High Speed CMOS QuickSwitch 8-bit Bus Switches, SOIC	Quality Semiconductor	QS3244D
Y1	Crystal resonator, 32.768 KHz, Frequency tolerance 30 ppm, Drive-level - 10µW Max, Shunt capacitance - 2pF Max., Load capacitance - 12.5pF Max., Equivalent Series Resistance - 35 KΩ Max.	RALTRON	RSM-200-32.768 KHZ
	14 pin PC Socket, SMD	PRECIDIP	110-91-314-41-105
	256 pin 16 X 16 BGA ZIF Socket	ENPLUS	BGA256(441)-1.27-05

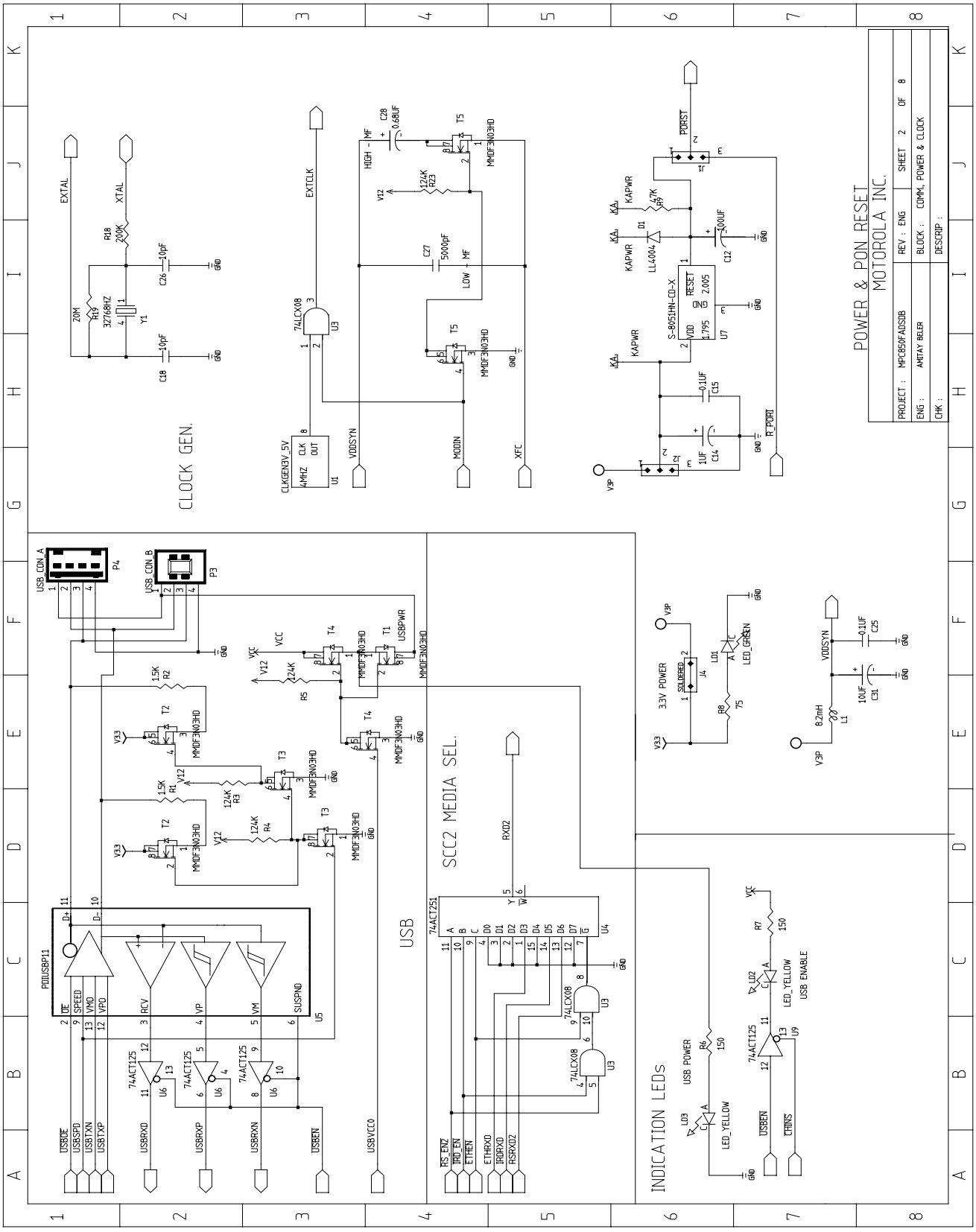
6 - MPC850SARDB Schematics

The schematics of the MPC850SARDB are shown bellow:

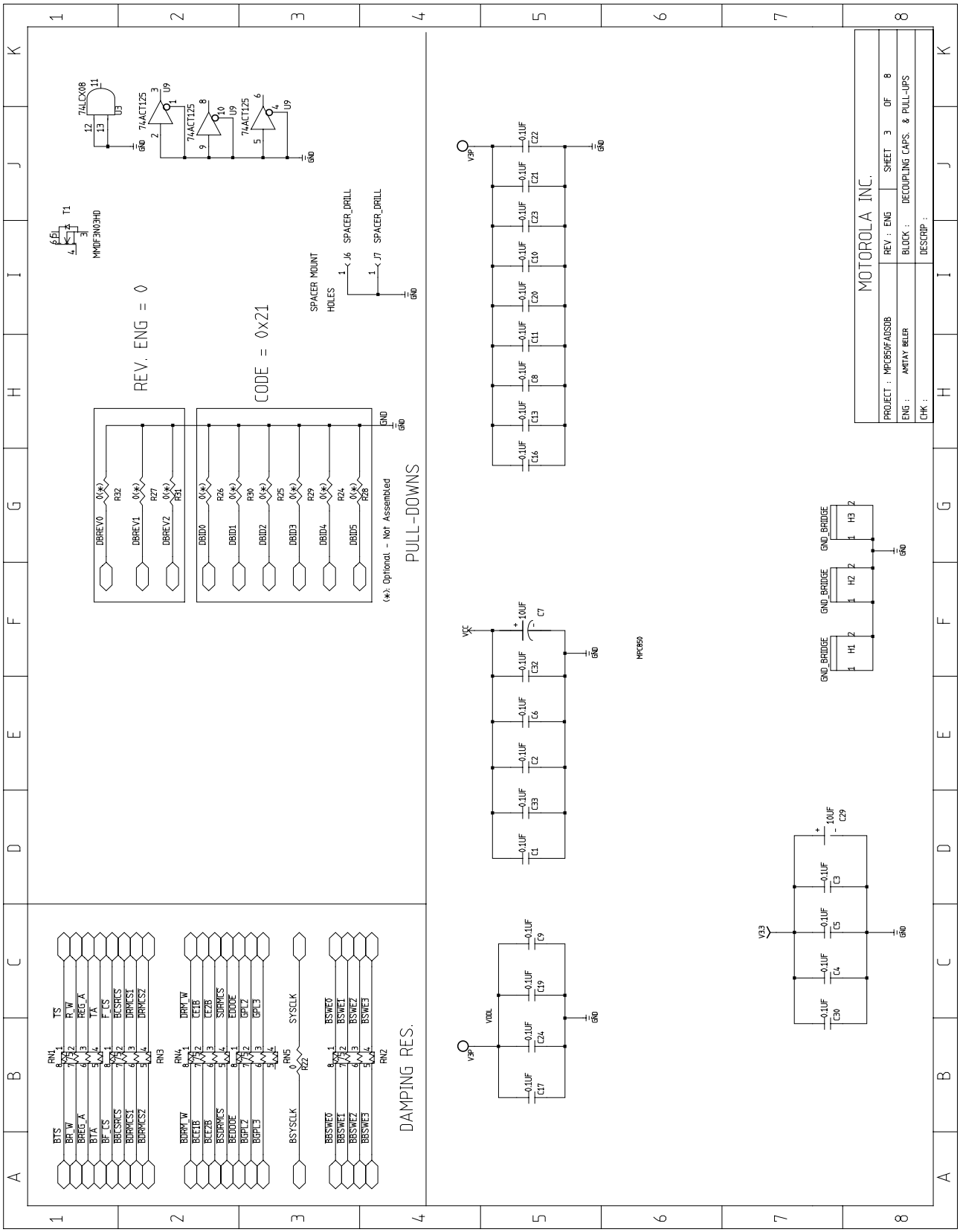
MPC850SARDB Schematics



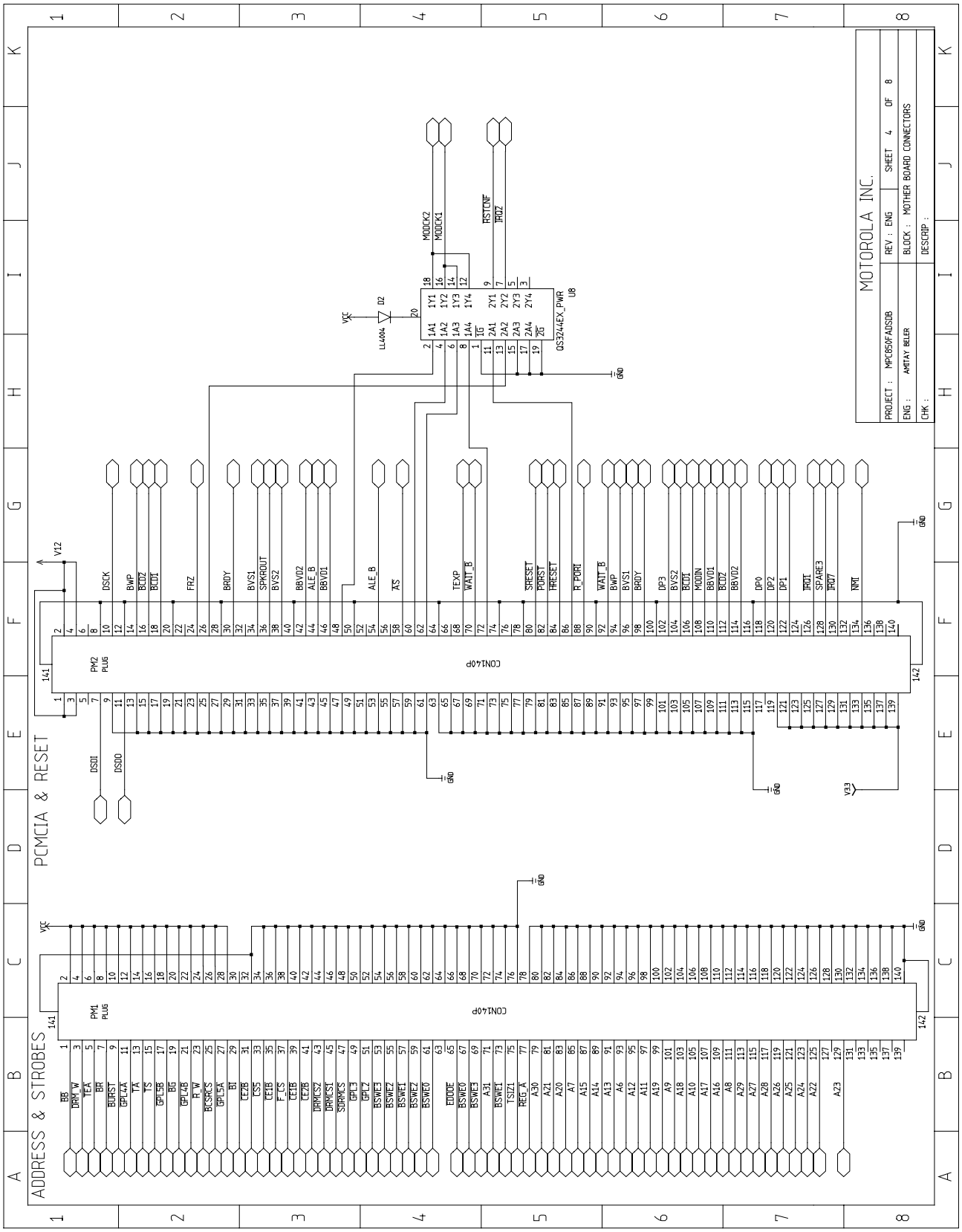
MPC850SARDB Schematics



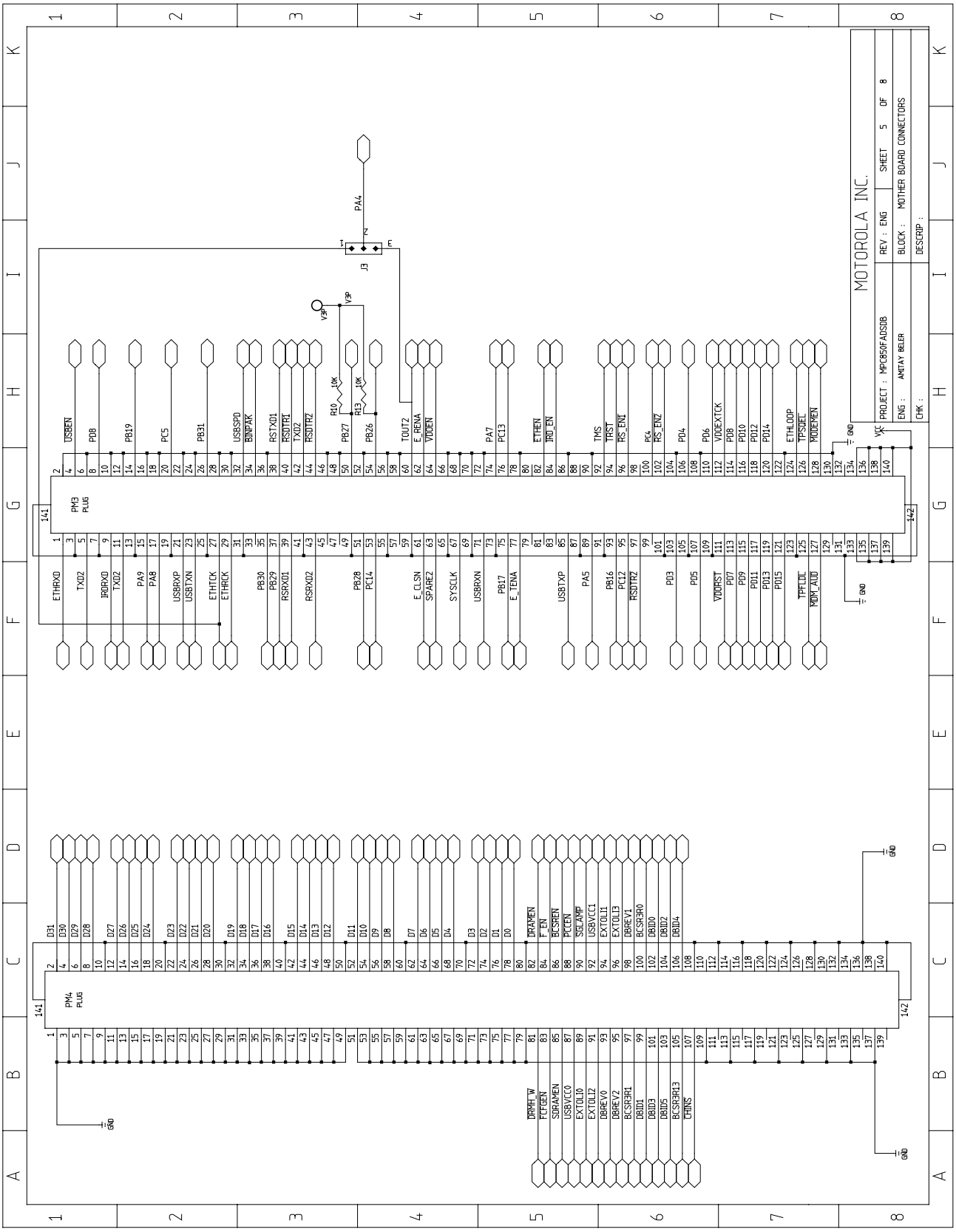
MPC850SARDB Schematics



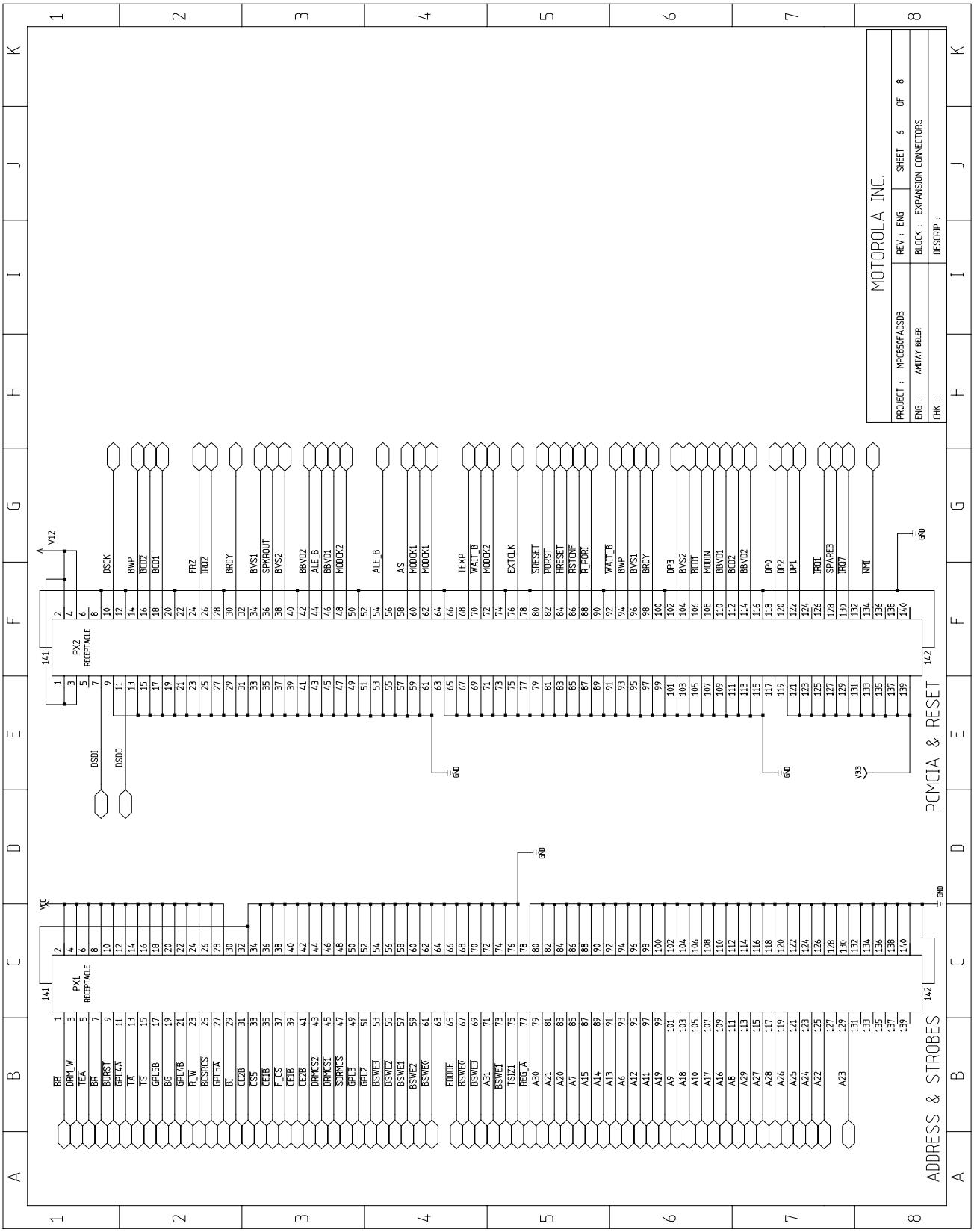
MPC850SARDB Schematics



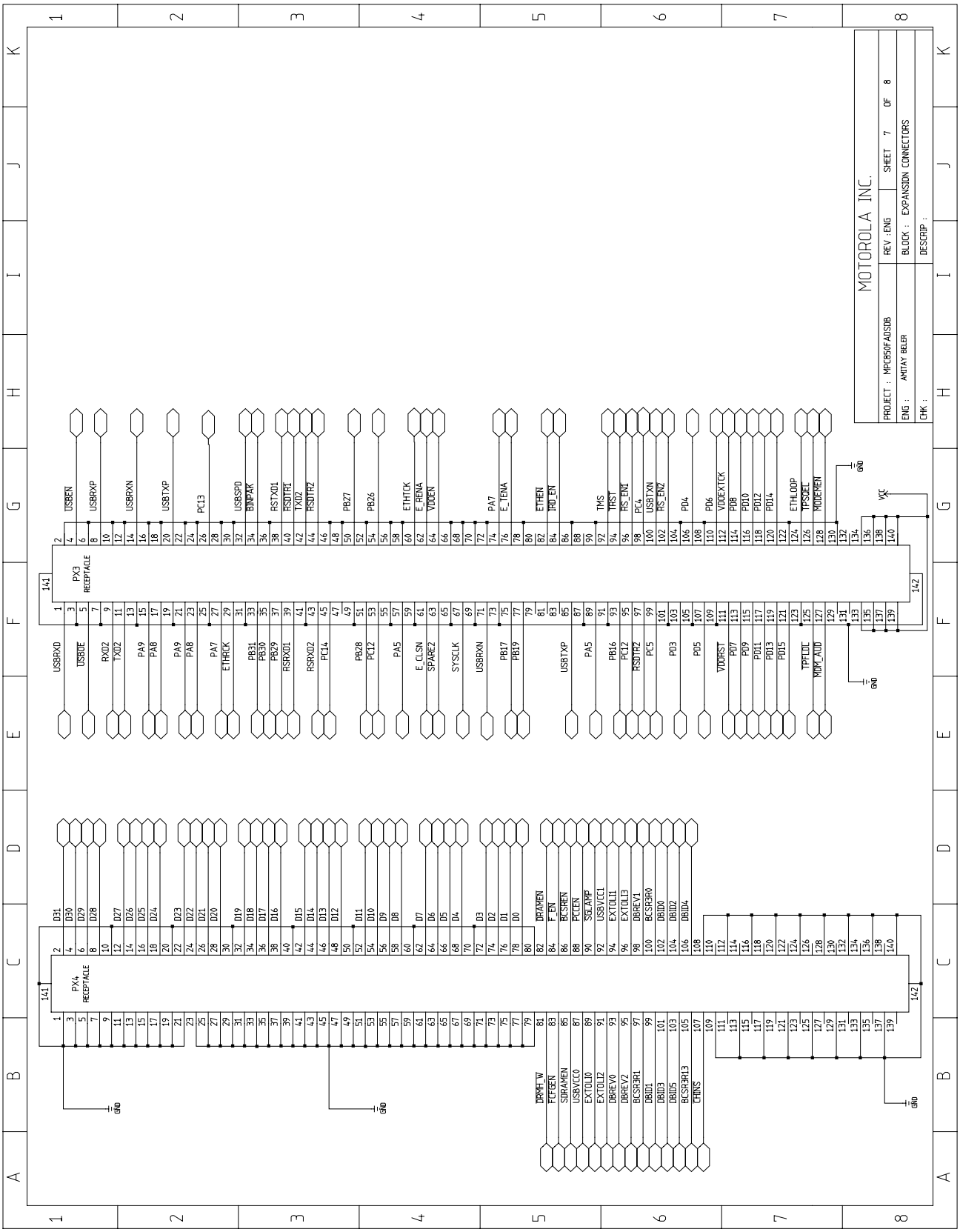
MPC850SARDB Schematics



MPC850SARDB Schematics



MPC850SARDB Schematics



MPC850SARDB Schematics