

HW Getting Started Guide



MPC8360EA MDS Processor Board

Dec 2006: Rev. E

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About This Document

This document shows how to connect the MPC8360EA MDS Processor Board and verify its basic operation, in a step by step format. Settings for switches and jumpers are shown, as well as instructions for connecting peripheral devices. Instructions for connecting the MPC8360EA MDS PB to an IDE, such as Freescale's *CodeWarrior*[®] are included, but instructions for working with the IDE are beyond the scope of this document. The MDS described here is for Ver 2.x of the MPC8360. This version of the board has a faster DDR2 (400MHz), a flash memory of 32MB, and an oscillator for IEEE 1588.

Required Reading

It is assumed that the reader is familiar with the MPC8360 chip, and the contents of the *MPC8360 Reference Manual*.

Definitions, Acronyms, and Abbreviations

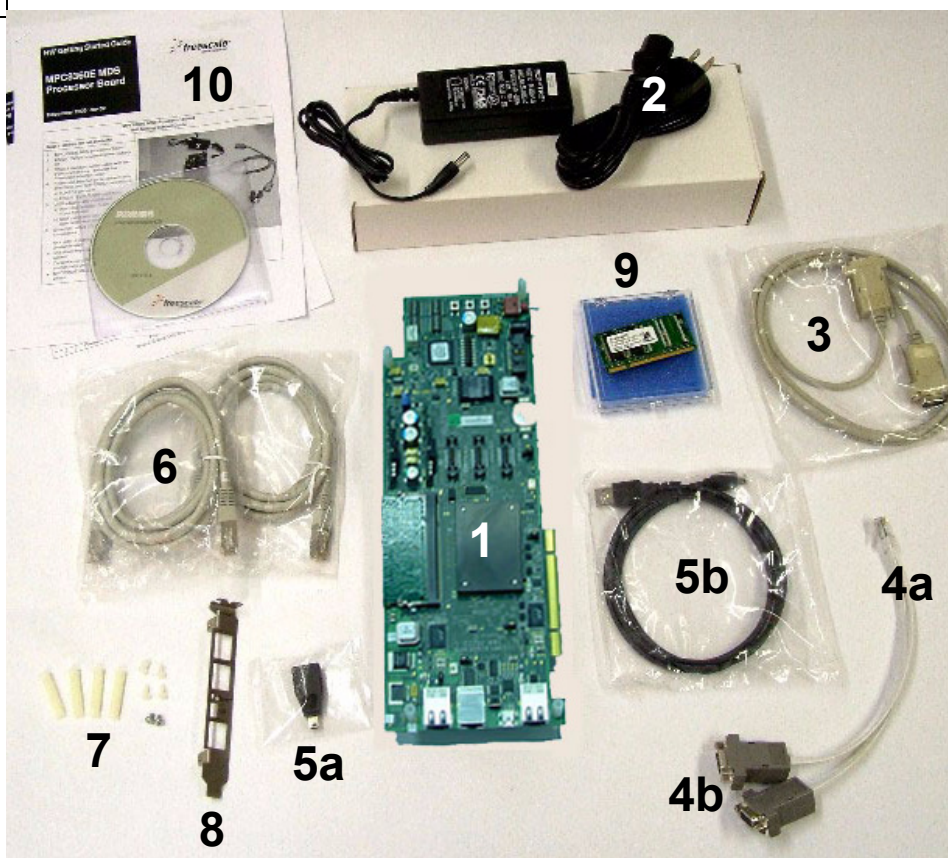
BCSR	Board Register	MDS	Modular Development System
CCB	Clock Controller parameter	PCI	Peripheral component interconnect
CEPMF	QE Lite PLL Multiplication Factor	PLL	Phase Lock Loop
CEVCOD	QE Lite PLL VCO Division	QE	Quick Engine, a block in the MPC83xx line of chips
COP	Debug port in PowerPC	SODIMM	Type of memory device
DDR	Double data rate DRAM	SPMF	System PLL Multiplication Factor
DIP	Dual In-line Package	SVCOD	System VCO Division
I2C	Philips serial port	RCW	Reset Configuration Word
LED	Light Emitting Diode	USB	Universal Serial Bus

MPC8360EA MDS Processor Board

HW Getting Started Guide

Step 1: Check HW kit contents

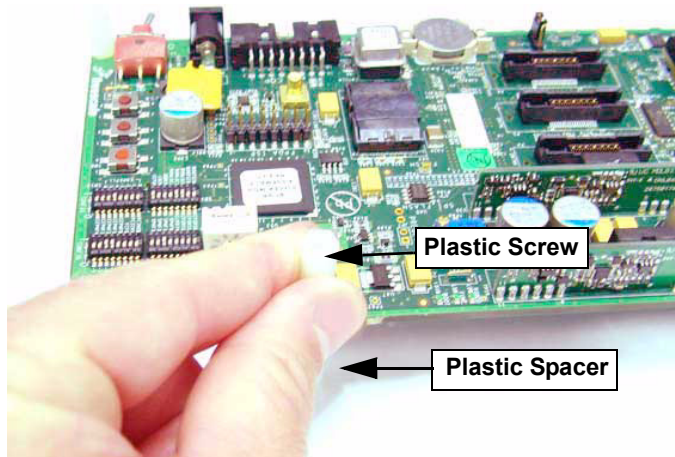
1. MPC8360EA MDS Processor Board
2. AC/DC 5V/5A universal power supply kit
3. RS232 standard serial cable with two 9-pin connectors-extends the Freescale adaptor cable
4. Freescale adaptor cable (joined) with one RJ45 and two RS232 connectors:
 - a) RJ45 10-pin plug
 - b) RS232 9-pin D-type connector
5. USB adaptor and connector:
 - a) Mini USB adaptor: 5-pin (male) and 4-pin (female)
 - b) USB cable with two connectors: standardA and miniB.
6. Ethernet cables (2) with RJ45-8 connectors
7. Four sets of plastic spacers (male/female)
8. Front panel for PC operation
9. Additional SODIMM unit
10. MPC8360EA MDS Processor Board documentation



Step 2: Connect plastic spacers

Four sets of plastic spacers screw into holes located at (approximately) the four corners of the board. The spacers raise and stabilize the board.

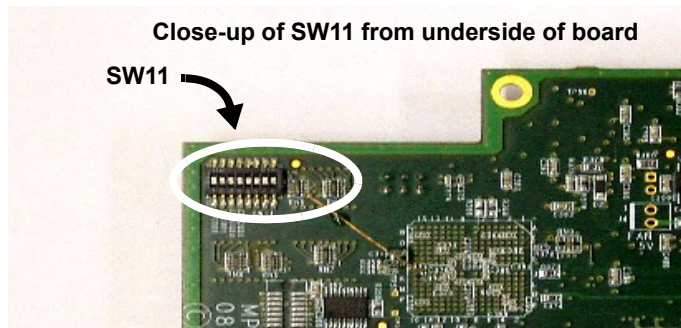
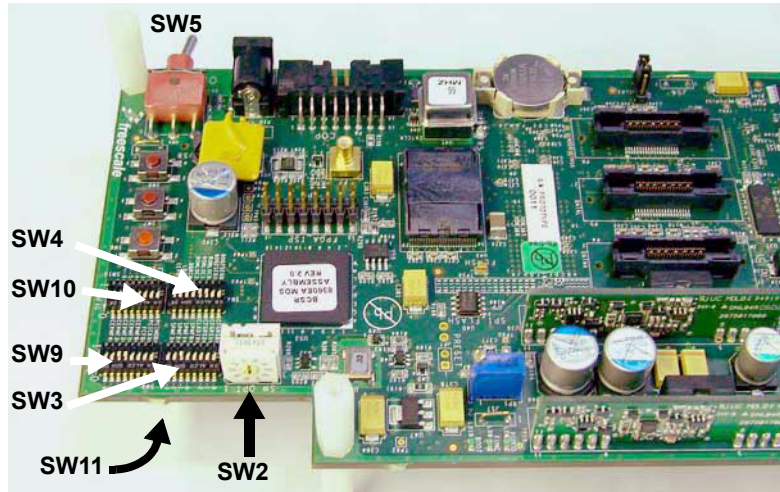
1. From under the board, insert a spacer into one of the board's four spacer holes.
2. Attach a plastic screw onto the male spacer.
3. Repeat for the three remaining spacers.



Step 3: Check Switches and Jumpers

The MPC8360EA MDS PB has two rows of Dual-In-Line Package (DIP) switches. The default DIP-switch positions set-up the MPC8360EA MDS PB clock mode as shown in the table below:

MPC8360EA MDS Processor Board Clock Mode (default values)	
e300 Core Frequency	533 MHz
CCB	266 MHz
DDR2 <i>(can be changed to 400MHz)</i>	266 MHz
Local Bus If LCRR = 0xXXXXXXXX2	133 MHz
QE	400 MHz



Step 3.a: SW3 Configuration Set 1

		1 <-	-> 0	
1:	CFG_RS0	1	<input type="checkbox"/>	ON
2:	CFG_RS1	2	<input type="checkbox"/>	
3:	CFG_RS2	3	<input type="checkbox"/>	
4:	CLKDIV	4	<input type="checkbox"/>	
5:	SPMF0	5	<input type="checkbox"/>	
6:	SPMF1	6	<input checked="" type="checkbox"/>	
7:	SPMF2	7	<input type="checkbox"/>	
8:	SPMF3	8	<input type="checkbox"/>	

The "On" DIP Switch position corresponds to a signal value of "zero".

SW3.1-SW3.3

CFG_RS sets the Reset Configuration Words Source
 ON: value of zero
 factory setting: '000' when RCW is fetched from the local bus
 DIP-switch SW9/3 FCFG: chooses between BCSR or Flash RCW source

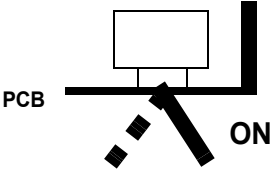
SW3.4

CLKDIV selects the relationship between CLKIN and PCI_SYNC_OUT
 if MPC8360 is configured as a PCI Agent (factory setting) then CLK_DIV is low

SW3.5-SW3.8

SPMF selects the System PLL Multiplication Factor
 factory setting: '0100'
 clock ratio: $csb_clk/CLKIN = 4$ ($csb_clk = 266MHz$) or
 $csb_clk/PCI_CLK = 4$

<p>Step 3.b: SW4 Configuration Set 2</p> <table style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th colspan="2"></th> <th style="text-align: center;">1 <-</th> <th style="text-align: center;">->0</th> <th></th> </tr> </thead> <tbody> <tr> <td>1:</td> <td>BOOTSEQ0</td> <td>1</td> <td style="background-color: black;"></td> <td rowspan="8" style="vertical-align: middle; text-align: center;">ON</td> </tr> <tr> <td>2:</td> <td>BOOTSEQ1</td> <td>2</td> <td style="background-color: black;"></td> </tr> <tr> <td>3:</td> <td>ROMLOC0</td> <td>3</td> <td style="background-color: black;"></td> </tr> <tr> <td>4:</td> <td>ROMLOC1</td> <td>4</td> <td style="background-color: black;"></td> </tr> <tr> <td>5:</td> <td>ROMLOC2</td> <td>5</td> <td style="background-color: black;"></td> </tr> <tr> <td>6:</td> <td>DDRCM</td> <td>6</td> <td style="background-color: black;"></td> </tr> <tr> <td>7:</td> <td>LBCM</td> <td>7</td> <td style="background-color: black;"></td> </tr> <tr> <td>8:</td> <td>CEPDF</td> <td>8</td> <td style="background-color: black;"></td> </tr> </tbody> </table>			1 <-	->0		1:	BOOTSEQ0	1		ON	2:	BOOTSEQ1	2		3:	ROMLOC0	3		4:	ROMLOC1	4		5:	ROMLOC2	5		6:	DDRCM	6		7:	LBCM	7		8:	CEPDF	8		<p>SW4.1-SW4.2: configuration boot sequencer boot sequencer loads configuration data from the serial ROM factory setting: '00'; disables access to I2C ROM</p> <p>SW4.3-SW4.5: boot ROM location factory setting: '110'; provides Flash boot on local bus</p> <p>SW4.6 DDR: clock mode factory setting: '0'; operates with DDR clock (identical to csb_clk)</p> <p>SW4.7: local bus clock mode factory setting: '0'; the local bus and Secondary DDR memory controller will operate with a frequency equal to csb_clk</p> <p>SW4.8: CEPDF factory setting: '0'; QE_clk = primary clock input X CEPDF</p>
		1 <-	->0																																				
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<p>Step 3.c: SW9 Configuration Set 3</p> <table style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th colspan="2"></th> <th style="text-align: center;">1 <-</th> <th style="text-align: center;">->0</th> <th></th> </tr> </thead> <tbody> <tr> <td>1:</td> <td>PCIMODE</td> <td>1</td> <td style="background-color: black;"></td> <td rowspan="8" style="vertical-align: middle; text-align: center;">ON</td> </tr> <tr> <td>2:</td> <td>PCICKDRV</td> <td>2</td> <td style="background-color: black;"></td> </tr> <tr> <td>3:</td> <td>FCFG</td> <td>3</td> <td style="background-color: black;"></td> </tr> <tr> <td>4:</td> <td>CEPMF0</td> <td>4</td> <td style="background-color: black;"></td> </tr> <tr> <td>5:</td> <td>CEPMF1</td> <td>5</td> <td style="background-color: black;"></td> </tr> <tr> <td>6:</td> <td>CEPMF2</td> <td>6</td> <td style="background-color: black;"></td> </tr> <tr> <td>7:</td> <td>CEPMF3</td> <td>7</td> <td style="background-color: black;"></td> </tr> <tr> <td>8:</td> <td>CDPMF4</td> <td>8</td> <td style="background-color: black;"></td> </tr> </tbody> </table>			1 <-	->0		1:	PCIMODE	1		ON	2:	PCICKDRV	2		3:	FCFG	3		4:	CEPMF0	4		5:	CEPMF1	5		6:	CEPMF2	6		7:	CEPMF3	7		8:	CDPMF4	8		<p>SW9.1: PCI_MODE. Sets PCI MODE if this switch is '0' factory setting: '0' (this switch should be only in '0' state)</p> <p>SW9.2: PCICKDRV Factory setting: '1'; driving for PCI clocks.</p> <p>SW9.3 FCFG: sets RCW source on local bus '0': BCSR source; settings from DIP-switches SW3-SW6 '1': Flash source factory setting: '1'; Flash boot</p> <p>SW9.4 - SW9.8: CEPMF Factory setting: '6'; '00110' If CLKDIV=0 then for 400Mhz CEPMF should be 6.</p>
		1 <-	->0																																				
1:	PCIMODE	1		ON																																			
2:	PCICKDRV	2																																					
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8:	CDPMF4	8																																					
<p>Step 3.d: SW10 Configuration Set 4</p> <table style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th colspan="2"></th> <th style="text-align: center;">1 <-</th> <th style="text-align: center;">->0</th> <th></th> </tr> </thead> <tbody> <tr> <td>1:</td> <td>COREPLL0</td> <td>1</td> <td style="background-color: black;"></td> <td rowspan="8" style="vertical-align: middle; text-align: center;">ON</td> </tr> <tr> <td>2:</td> <td>COREPLL1</td> <td>2</td> <td style="background-color: black;"></td> </tr> <tr> <td>3:</td> <td>COREPLL2</td> <td>3</td> <td style="background-color: black;"></td> </tr> <tr> <td>4:</td> <td>COREPLL3</td> <td>4</td> <td style="background-color: black;"></td> </tr> <tr> <td>5:</td> <td>COREPLL4</td> <td>5</td> <td style="background-color: black;"></td> </tr> <tr> <td>6:</td> <td>COREPLL5</td> <td>6</td> <td style="background-color: black;"></td> </tr> <tr> <td>7:</td> <td>COREPLL6</td> <td>7</td> <td style="background-color: black;"></td> </tr> <tr> <td>8:</td> <td>NC</td> <td>8</td> <td style="background-color: black;"></td> </tr> </tbody> </table>			1 <-	->0		1:	COREPLL0	1		ON	2:	COREPLL1	2		3:	COREPLL2	3		4:	COREPLL3	4		5:	COREPLL4	5		6:	COREPLL5	6		7:	COREPLL6	7		8:	NC	8		<p>SW10.1-SW10.7: core PLL setting sets the ratio between the e300 core clock and the internal csb_clk factory setting: '00001000' for fcore = 533MHz , set '00000110' for fcore = 500MHz</p>
		1 <-	->0																																				
1:	COREPLL0	1		ON																																			
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7:	COREPLL6	7																																					
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<p>Step 3.e: SW11 Configuration Set 5</p> <table style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th colspan="2"></th> <th style="text-align: center;">1 <-</th> <th style="text-align: center;">->0</th> <th></th> </tr> </thead> <tbody> <tr> <td>1:</td> <td>SVCOD0</td> <td>1</td> <td style="background-color: black;"></td> <td rowspan="8" style="vertical-align: middle; text-align: center;">ON</td> </tr> <tr> <td>2:</td> <td>SVCOD1</td> <td>2</td> <td style="background-color: black;"></td> </tr> <tr> <td>3:</td> <td>CECVOD0</td> <td>3</td> <td style="background-color: black;"></td> </tr> <tr> <td>4:</td> <td>CECVOD1</td> <td>4</td> <td style="background-color: black;"></td> </tr> <tr> <td>5:</td> <td>COREDIS</td> <td>5</td> <td style="background-color: black;"></td> </tr> <tr> <td>6:</td> <td></td> <td>6</td> <td style="background-color: black;"></td> </tr> <tr> <td>7:</td> <td></td> <td>7</td> <td style="background-color: black;"></td> </tr> <tr> <td>8:</td> <td></td> <td>8</td> <td style="background-color: black;"></td> </tr> </tbody> </table>			1 <-	->0		1:	SVCOD0	1		ON	2:	SVCOD1	2		3:	CECVOD0	3		4:	CECVOD1	4		5:	COREDIS	5		6:		6		7:		7		8:		8		<p>SW11.1 - SW11.2: SVCOD sets SVCOD to '0' factory setting: 0;</p> <p>SW11.3 - SW11.4: CEVCODE Set CECVOD to 0; factory setting: '0';</p> <p>SW11.5 - COREDIS Set COREDIS to '0';</p>
		1 <-	->0																																				
1:	SVCOD0	1		ON																																			
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6:		6																																					
7:		7																																					
8:		8																																					

<p>Step 3.f: SW5 Power Switch</p> 	<p>SW5: power switch ON: power from an external 5V power supply via the P10 power jack combined mode: powered from +5V on PIB power supply through riser connectors (regardless of SW5 position) board plugged as a PCI add-in card: PC internal power supply will provide 5V via PCI edge connector</p>
<p>Step 3.g: JP1: 3.3V/2.5V</p>	<p>GEthernet Voltage For 2.5V connect 1-2 For 3V JP1 connect 3-2</p>
<p>Step 3.h: JP1_1: ATM/USB</p>	<p>JP1_1 Select between ATM function of USB function. For USB, connect 1-2 For ATM connect 3-2</p>
<p>Step 3.i: JP2:</p>	<p>Connect jumper</p>
<p>Step 3.j: JP3:</p>	<p>Connect jumper</p>
<p>Step 3.k: JP4: TDMATXCLK/M2GTX125</p>	<p>For GMII2, connect 1-2 (M2GTX125 for GTETH2). For TDMA when using PIB, connect 3-2.</p>
<p>Step 3.l: JP5: LVDD2 3.3V/2.5V</p>	<p>8360 LVDD2 Power For LVDD2 3.3V connect 2-3. For LVDD2 2.5V connect 1-2.</p>
<p>Step 3.m: JP6: Clock source PIB(onboard)/External</p>	<p>JP6 Clock Connect 1-2 to use an external clock. Connect 2-3 to use an internal clock</p>
<p>Step 3.n: JP7: Reset.</p>	<p>JP7 reset (not connected).</p>

Step 4: Assemble and connect the power supply kit.

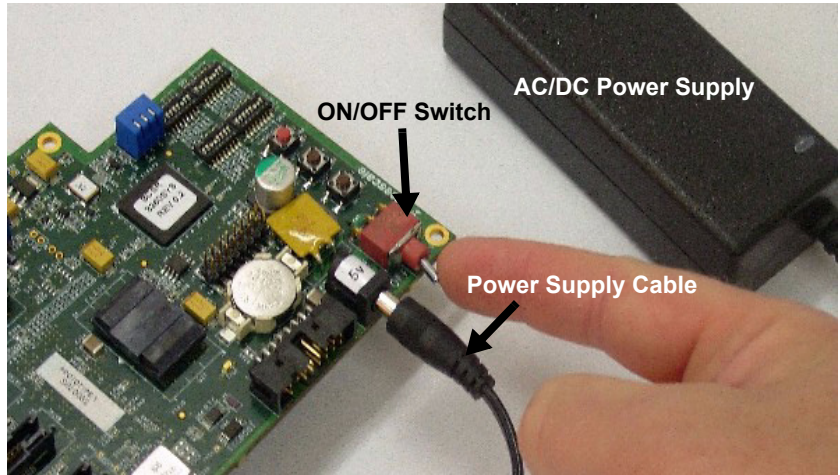
Note:
Move power switch to OFF.

Assemble the AC/DC power supply kit:

- power cable with country-specific wall outlet plug
- power supply unit and cable with jack (for board connection)

1. Connect the AC/DC power supply cable with jack to the board.
2. Plug the power cable into the wall outlet.

Note: An earlier version of the Processor Board is shown, but the principle is the same.



Step 5: Perform initial board power up.

Caution:
To prevent damage to the JTAG connectivity unit (part of the CodeWarrior SW kit) connect the unit only after initial board reset.

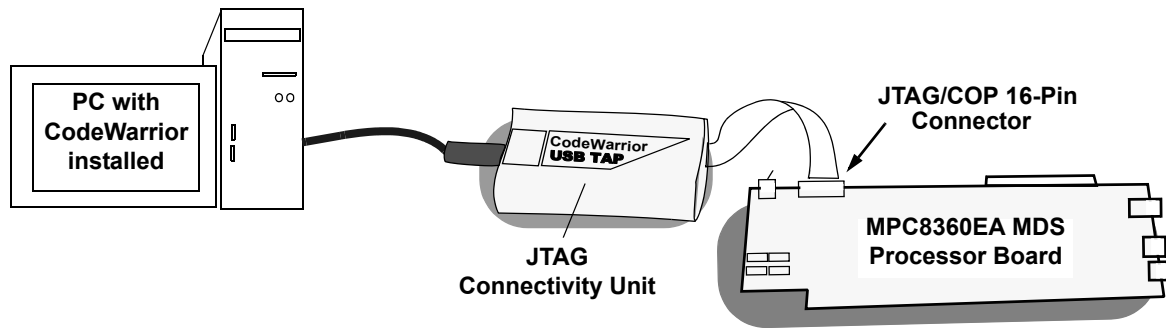
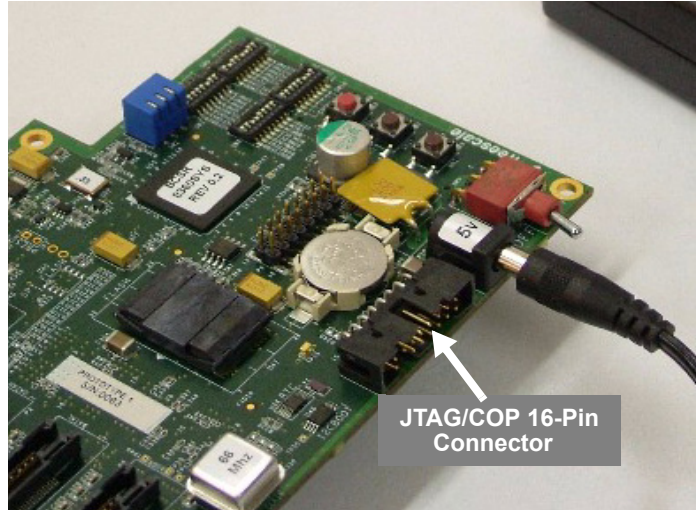
1. Move the power switch to ON. LED13 briefly displays green light.
2. Check for completion of the reset sequence—indicated by a single flash of LED1 (green) and LED2 (red). The location of LED1 and LED2 is marked in the figure of Step 7 on page 8.
3. Shut off the power—move the power switch to OFF.

Step 6: Connect the JTAG connectivity unit to the board.

The JTAG connectivity unit (included as part of the CodeWarrior SW kit) enables CodeWarrior SW work with the board.

1. Connect the JTAG connectivity unit to the JTAG/COP 16-pin connector.
2. Move the power switch to ON.
3. Check for completion of the reset sequence (see Step 5 on page 6).
4. Continue as per the instructions in the CodeWarrior SW Quick Start document.

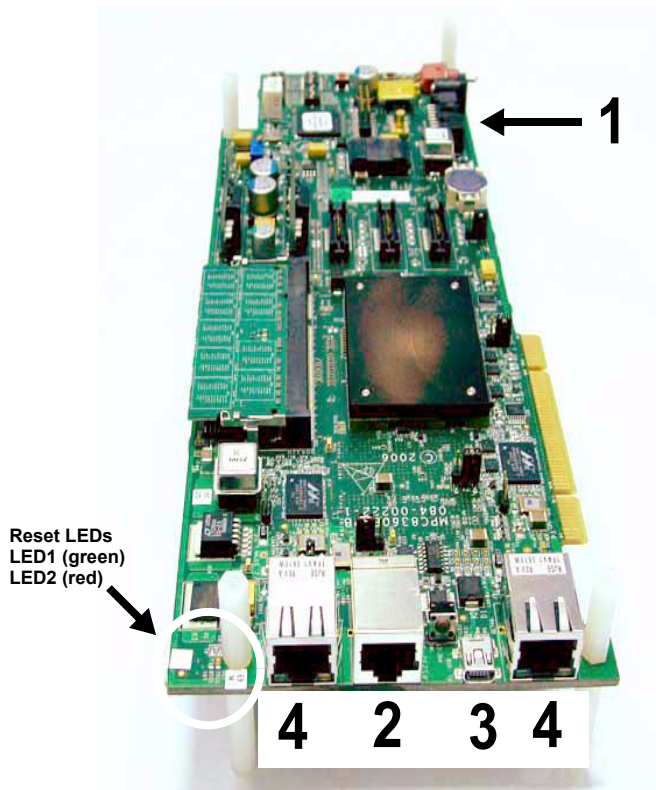
Note: An earlier version of the Processor Board is shown, but the principle is the same.



Step 7: Attach remaining cables to the board according to your development needs.

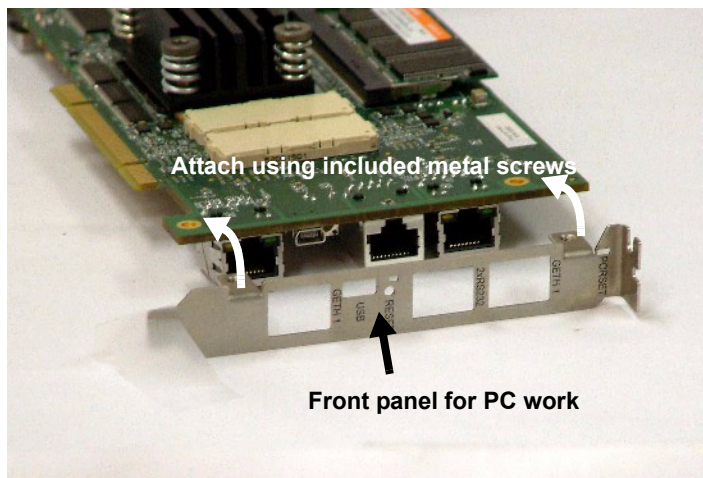
Connect the remaining cables to the board as per user development needs and planned board use:

1. JTAG/COP connector for JTAG connectivity unit-included in the CodeWarrior SW kit
2. Serial port for the joined Freescale adaptor cable with one RJ45 and two RS232 connectors:
 - a. RJ45 10-pin plug-plugs into the serial port
 - b. RS232 9-pin D-type connector
3. USB port for USB adaptor and connector:
 - a. mini USB adaptor: 5-pin (male) and 4-pin (female)
 - b. USB cable with two connectors: standardA and miniB.
4. Ethernet ports for the two Ethernet cables with RJ45-8 pin connectors.



Step 8: (Optional) If inserting the board in a PC, attach the front panel as shown

Use the two metal screws, included in the kit.



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