KE17ZDTSIUG

KE17Z Dual Touch Sensing Interface (TSI) User Guide

Rev. 2 — 7 May 2024 **User guide**

Document information

Information	Content
Keywords	KE17ZDTSIUG, KE17Z, KE1xZ, TSI, touch, touch sensing, touch electrode, touchpad
Abstract	Touch Sensing Interface (TSI) provides touch sensing detection on capacitive touch sensors.

1 Introduction

Touch Sensing Interface (TSI) provides touch sensing detection on capacitive touch sensors. The external capacitive touch sensor is typically formed on a PCB. The sensor electrodes are connected to TSI input channels through the I/O pins in the device.

1.1 TSI model support of KE1xZ family

Figure 1 shows the KE1xZ family category according to TSI module support.

- KE17Z family includes the KE17Z512 series with up to 96 MHz frequency, and the KE17Z256 series with up to 72 MHz frequency. For the KE17Z family, KE17Z parts support two TSI modules, KE13Z parts support one TSI module, and KE12Z parts do not support TSI.
- For KE15Z family and KE16Z family, the KE15Z256/128 parts, KE16Z64/32 parts, KE15Z64/32 parts support one TSI module, KE14Z parts do not support TSI.

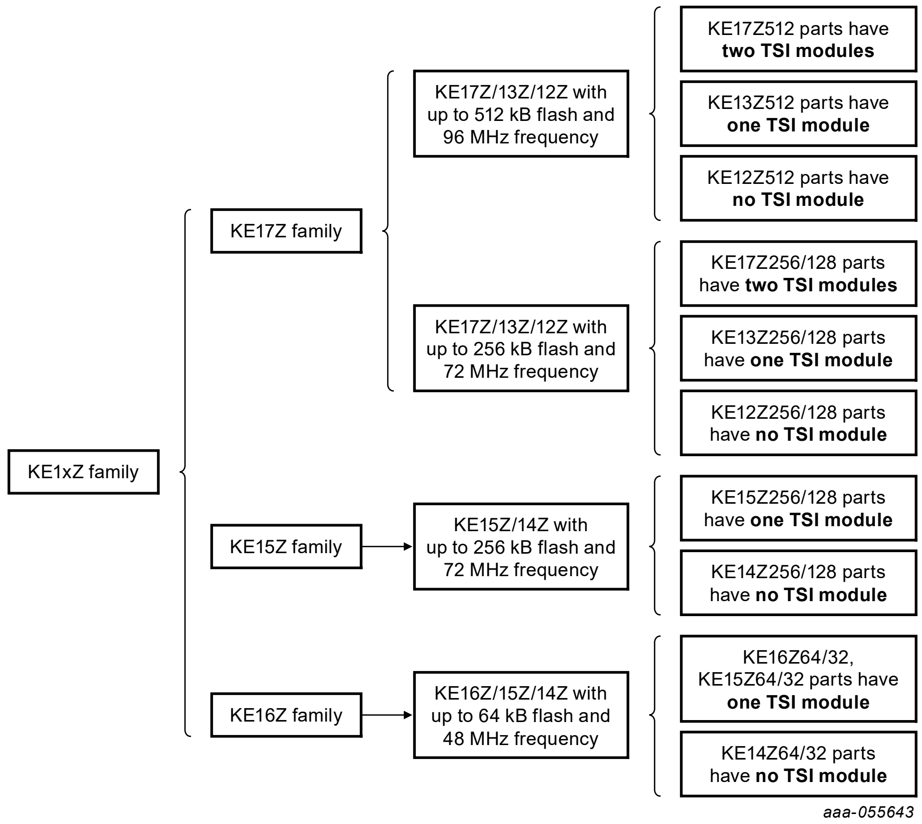

Figure 1. KE1xZ family category according to the TSI module support

1.2 KE17Z dual TSI

1.2.1 KE17Z dual TSI features

KE17Z MCU has two TSI modules. It supports two kinds of touch sensing methods: self-capacitance (also called self-cap) mode and mutual-capacitance (also called mutual-cap) mode.

The dual-TSI technology of the KE17Z MCU supports up to 50 touch channels. The two TSI modules not only increase the number of touch electrodes, but also work in parallel to increase the scanning efficiency of touch electrodes and save the scanning time.

To enhance the liquid tolerance and improve the driving ability, each TSI module has three shield channels, up to 25 touch channels for self-cap mode, and up to 6 × 6 touch channels for mutual-cap mode. Both mentioned methods can be combined on one single PCB, while only the lower 12 TSI channels TSI[0:11] can be used for mutual mode.

Note: *`TSI[0:5]` are TSI TX pins and `TSI[6:11]` are TSI RX pins in mutual mode.*

- In the self-capacitive mode, developers can use these 50 channels to design 50 (25 × 2) touch electrodes.
- In the mutual-capacitive mode, design options expand to up to 72 (6 × 6 × 2) touch electrodes.

In some use cases, such as a multi-burner induction cooker with touch controls or touch keyboards, the MCUs can support touchscreen designs scaling up to 98 touch electrodes (26 electrodes using self-capacitance + 72 electrodes using mutual channels).

1.2.2 TSI model difference of KE17Z512 and KE17Z256/128

KE17Z512 and KE17Z256/128 are all support the dual TSI modules. To improve shield drive strength, the TSI IP in KE17Z512 series has done upgrade to enhance the shield channel drive strength and increase the number of shield channels by the using a shield multiplexing feature.

Table 1 describes the shield feature comparison between KE17Z512 series and KE17Z256 series.

Table 1. Shield feature comparison between KE17Z512 series and KE17Z256/128 series

Shield channel features	KE17Z512	KE17Z256/128
Flexible shield channel	Each TSI channel can be configured as a shield channel.	Each TSI module has up to three normal drive shield channels. These three channels are flexible and configurable.
Support more TSI shield channels	Each TSI can support up to 25 shield channels.	
Enhanced TSI shield channel	The shield drive strength of four TSI shield channels are enhanced four times compared to other shield channels.	

1.2.3 Features of KE17Z dual TSI models

Table 2. Features of KE17Z dual TSI models

Features	KE17Z series TSI
Operating voltage	2.7 V – 5.5 V
Function clock source	TSI internal generated
Function clock range	37 KHz-10 MHz
Sensing mode	• Self-cap mode: – Basic self-cap mode – Sensitivity boost mode – Noise cancellation mode • Mutual-cap mode: – Basic mutual-cap mode – Sensitivity boost enable
TSI channels	Up to 50 channels (TSI0, TSI1)
Touch channel assignment	• Self-cap mode: TSI[0:24]

Table 2. Features of KE17Z dual TSI models...*continued*

Features	KE17Z series TSI
	• Mutual-cap mode: Tx[0:5], Rx[6:12]
Touch Electrodes support	• Self-cap electrodes: up to 50 (25+25) • Mutual-cap electrodes: up to 72 (6 × 6 + 6 × 6) • Total up to: 98
Shield channels	• KE17Z512: – Each touch channel can be configured as the shield channel, up to 25 shield channels for each TSI module. – Four enhanced shield channels for each TSI: CH4, CH12, CH21, CH24 • KE17Z256/128: – Three shield channels for each TSI: CH4, CH12, CH21
Trigger source support	• Software trigger by writing GENCS[SWTS] bit. • Hardware trigger through INPUTMUX
Interrupt support	End of scan interrupt, Out of range interrupt
Low power support	STOP mode, VLPS mode: fully function when setting `GENCS[STPE]` to 1
Low power wakeup	Each TSI channel can wake up MCU from low power mode
DMA support	The out-of-range event or end-of-scan event can trigger the DMA transfer
Hardware noise filter	SSC reduces the frequency noise and promotes the signal-to-noise ratio. (PRBS mode, up-down counter mode)
IEC 61000 -4-6	Passed 3 V/10 V level

1.3 KE1xZ part numbers supporting TSI model

This chapter lists all the KE1xZ ordering parts with TSI supported, which is for users to check.

1.3.1 KE17Z parts supporting dual TSI modules

Table 3 lists the number of TSI channels corresponding to different parts of KE17Z. These parts all support dual TSI modules.

Table 3. KE17Z parts supporting dual TSI modules

Product	Frequency	Memory		Package		IO and ADC channel			HMI
Part number	MHz	Flash (kB)	SRAM (kB)	Pin count	Package	GPIOs	GPIOs (INT/HD)	ADC channels	TSI [Number, channels]
MKE17 Z512VLL9	96	512	96	100	LQFP	89	89/8	24	2, 50 ch
MKE17 Z512VLH9	96	512	96	64	LQFP	58	58/8	24	2, 50 ch
MKE17 Z256VLL7	72	256	48	100	LQFP	89	89/8	16	2, 50 ch
MKE17 Z256VLH7	72	256	48	64	LQFP	58	58/8	16	2, 47 ch
MKE17 Z256VLF7	72	256	48	48	LQFP	42	42/6	11	2, 31 ch

Table 3. KE17Z parts supporting dual TSI modules*...continued*

Product	Frequency	Memory		Package		IO and ADC channel			HMI
Part number	MHz	Flash (kB)	SRAM (kB)	Pin count	Package	GPIOs	GPIOs (INT/HD)	ADC channels	TSI [Number, channels]
MKE17 Z128VLL7	72	128	32	100	LQFP	89	89/8	16	2, 50 ch
MKE17 Z128VLH7	72	128	32	64	LQFP	58	58/8	16	2, 47 ch
MKE17 Z128VLF7	72	128	32	48	LQFP	42	42/6	11	2, 31 ch

1.3.2 KE1xZ parts supporting one TSI module

Table 4 to Table 6 list the number of TSI channels corresponding to different parts of KE13Z, KE15Z256/128, KE16Z64/32, and KE15Z64/32. These parts all support one TSI modules.

Table 4. KE13Z parts supporting one TSI module

Product	Frequency	Memory		Package		IO and ADC channel			HMI
Part number	MHz	Flash (kB)	SRAM (kB)	Pin count	Package	GPIOs	GPIOs (INT/HD)	ADC channels	TSI [Number, channels]
MKE13 Z512VLL9	96	512	96	100	LQFP	89	89/8	24	1, 25 ch
MKE13 Z512VLH9	96	512	96	64	LQFP	58	58/8	24	1, 22 ch
MKE13 Z256VLL7	72	256	48	100	LQFP	89	89/8	16	1, 25 ch
MKE13 Z256VLH7	72	256	48	64	LQFP	58	58/8	16	1, 22 ch
MKE13 Z256VLF7	72	256	48	48	LQFP	42	42/6	11	1, 15 ch
MKE13 Z128VLL7	72	128	32	100	LQFP	89	89/8	16	1, 25 ch
MKE13 Z128VLH7	72	128	32	64	LQFP	58	58/8	16	1, 22 ch
MKE13 Z128VLF7	72	128	32	48	LQFP	42	42/6	11	1, 15 ch

Table 5. KE15Z256/128 parts supporting one TSI module

Product	Frequency	Memory			Package		IO and ADC channel			HMI
Part number	MHz	Flash (kB)	SRAM (kB)	Flex NVM/ FlexRAM (KB)	Pin count	Package	GPIOs	GPIOs (INT/HD)	ADC channels	TSI [Number, channels]
MKE15 Z256 VLL7	72	256	32	32/2	100	LQFP	89	89/8	16+12	1, 25 ch
MKE15 Z256 VLH7	72	256	32	32/2	64	LQFP	58	58/8	16+11	1, 22 ch
MKE15 Z128 VLL7	72	128	16	32/2	100	LQFP	89	89/8	16+12	1, 25 ch
MKE15 Z128 VLH7	72	128	16	32/2	64	LQFP	58	58/8	16+11	1, 22 ch

Table 6. KE16Z64/32, KE15Z64/32 parts supporting one TSI module

Product	Frequency	Memory		Package		IO and ADC channel			HMI
Part number	MHz	Flash (kB)	SRAM (kB)	Pin count	Package	GPIOs	GPIOs (INT/HD)	ADC channels	TSI [Number, channels]
MKE16 Z64VLF4	48	64	8	48	LQFP	42	42/6	12	1, 25 ch
MKE16 Z64VLD4	48	64	8	44	LQFP	38	38/6	12	1, 22 ch
MKE15 Z64VLF4	48	64	8	48	LQFP	42	42/6	12	1, 25 ch
MKE15 Z64VLD4	48	64	8	44	LQFP	38	38/6	12	1, 22 ch
MKE16 Z32VLF4	48	32	4	48	LQFP	42	42/6	12	1, 25 ch
MKE16 Z32VLD4	48	32	4	44	LQFP	38	38/6	12	1, 22 ch
MKE15 Z32VLF4	48	32	4	48	LQFP	42	42/6	12	1, 25 ch
MKE15 Z32VLD4	48	32	4	44	LQFP	38	38/6	12	1, 22 ch
MKE15 Z64VFP4	48	64	8	40	QFN	36	36/4	11	1, 23 ch
MKE15 Z32VFP4	48	32	4	40	QFN	36	36/4	11	1, 23 ch

1.4 TSI model comparison of KE1xZ family

Table 7 shows the detailed TSI channel configuration for each KE1xZ part. It helps users to select the proper part number for touch application design.

Table 7. KE1xZ TSI channels for different package

		KE17Z family with up to 512 kB Flash				KE17Z family with up to 256 kB Flash						KE15Z with up to 256 kB Flash	KE16Z family with up to 64 kB Flash		
TSI module		2		1		2			1			1	1		
Package		KE17 Z512 100LQFP	KE17 Z512 64LQFP	KE13 Z512 100LQFP	KE13 Z512 64LQFP	KE17Z 100LQFP	KE17Z 64LQFP	KE17Z 48LQFP	KE13Z 100LQFP	KE13Z 64LQFP	KE13Z 48LQFP	KE15Z 100/64 LQFP	KE16Z/ KE15Z 48LQFP	KE16Z/ KE15Z 44LQFP	KE15Z 40QFN
Part number		MKE17 Z512 VLL9	MKE17 Z512 VLH9	MKE13 Z512 VLL9	MKE13 Z512 VLH9	MKE17 Z256 VLL7 MKE17 Z128 VLL7	MKE17 Z256 VLH7 MKE17 Z128 VLH7	MKE17 Z256 VLF7 MKE17 Z128 VLF7	MKE13 Z256 VLL7 MKE13 Z128 VLL7	MKE13 Z256 VLH7 MKE13 Z128 VLH7	MKE13 Z256 VLF7 MKE13 Z128 VLF7	MKE15Z256 VLL7 MKE15 Z128VLL7 MKE15Z256 VLH7 MKE15 Z128VLH7	MKE16 Z64VLF4 MKE15 Z64VLF4 MKE16 Z32VLF4 MKE15 Z32VLF4	MKE16 Z64VLD4 MKE15 Z64VLD4 MKE16 Z32VLD4 MKE15 Z32VLD4	MKE15 Z64VFP4 MKE15 Z32VFP4
Frequency		96 MHz	96 MHz	96 MHz	96 MHz	72 MHz	72 MHz	72 MHz	72 MHz	72 MHz	72 MHz	72 MHz	48 MHz	48 MHz	48 MHz
Flash		512 kB	512 kB	512 kB	512 kB	256 KB/128 KB	256 KB/128 KB	256 KB/128 KB	256 KB/128 KB	256 KB/128 KB	256 KB/128 KB	256 KB/128 KB	64 KB/32 KB	64 KB/32 KB	64 KB/32 KB
Max. keys support		98	95	49	46	98	95	39	49	46	19	49	49	33	47
Total TSI channels	Self-cap mode	50-ch (TSI0:25-ch, TSI1:25-ch)	47-ch (TSI0:22-ch, TSI1:25-ch)	25-ch (TSI0:25-ch)	22-ch (TSI0:22-ch)	50-ch (TSI0:25-ch, TSI1:25-ch)	47-ch (TSI0:22-ch, TSI1:25-ch)	31-ch (TSI0:15-ch, TSI1:16-ch)	25-ch (TSI0:25-ch)	22-ch (TSI0:22-ch)	15-ch (TSI0:15-ch)	25-ch (TSI0:25-ch)	25-ch (TSI0:25-ch)	22-ch (TSI0:22-ch)	23-ch (TSI0:23-ch)
	Mutual-cap mode	24-ch (TSI0: TX/6-ch, RX/6-ch; TSI1:TX/6-ch, RX/6-ch)	24-ch (TSI0: TX/6-ch, RX/6-ch; TSI1:TX/6-ch, RX/6-ch)	12-ch (TSI0: TX/6-ch, RX/6-ch)	12-ch (TSI0: TX/6-ch, RX/6-ch)	24-ch (TSI0: TX/6-ch, RX/6-ch; TSI1:TX/6-ch, RX/6-ch)	24-ch (TSI0: TX/6-ch, RX/6-ch; TSI1:TX/6-ch, RX/6-ch)	16-ch (TSI0: TX/2-ch, RX/6-ch; TSI1:TX/6-ch, RX/2-ch)	12-ch (TSI0: TX/6-ch, RX/6-ch)	12-ch (TSI0: TX/6-ch, RX/6-ch)	8-ch (TSI0: TX/2-ch, RX/6-ch)	12-ch (TSI0: TX/6-ch, RX/6-ch)	12-ch (TSI0: TX/6-ch, RX/6-ch)	9-ch (TSI0: TX/4-ch, RX/5-ch)	12-ch (TSI0: TX/6-ch, RX/6-ch)

Table 7. KE1xZ TSI channels for different package*...continued*

		KE17Z family with up to 512 kB Flash				KE17Z family with up to 256 kB Flash						KE15Z with up to 256 kB Flash	KE16Z family with up to 64 kB Flash		
TSI0	Self-cap channel	25-ch TSI0[0:24]	22-ch TSI0[0:12],[16:24]	25-ch TSI0[0:24]	22-ch TSI0[0:12],[16:24]	25-ch TSI0[0:24]	22-ch TSI0[0:12],[16:24]	15-ch TSI0[0-1,6-12,16-18,22-24]	25-ch TSI0[0:24]	22-ch TSI0[0:12],[16:24]	15-ch TSI0[0-1,6-12,16-18,22-24]	25-ch TSI0[0:24]	25-ch TSI0[0:24]	22-ch TSI0[0:1,4:10,12:24]	23-ch TSI0[0:18,20:23]
	Mutual-cap channel	TX[0:5], RX[6:11]	TX[0:5], RX[6:11]	TX[0:5], RX[6:11]	TX[0:5], RX[6:11]	TX[0:5], RX[6:11]	TX[0:5], RX[6:11]	TX[0:1], RX[6:11]	TX[0:5], RX[6:11]	TX[0:5], RX[6:11]	TX[0:1], RX[6:11]	TX[0:5], RX[6:11]	TX[0:5], RX[6:11]	TX[0:1, 4:5], RX[6:10]	TX[0:5], RX[6:11]
	Shield channel	Up to 25 shield channels: CH4, CH12, CH21, CH24 are enhanced TSI channels than others.	Up to 22 shield channels: CH4, CH12, CH21, CH24 are enhanced TSI channels than others.	Up to 25 shield channels: CH4, CH12, CH21, CH24 are enhanced TSI channels than others.	Up to 22 shield channels: CH4, CH12, CH21, CH24 are enhanced TSI channels than others.	Three shield channels: CH4, CH12, CH21	Three shield channels: CH4, CH12, CH21	One shield channel: CH12	Three shield channels: CH4, CH12, CH21	Three shield channels: CH4, CH12, CH21	One shield channel: CH12	One shield channel: CH12	One shield channel: CH12	One shield channel: CH12	One shield channel: CH12
	Comment		No CH13, CH14, CH15		No CH13, CH14, CH15		No CH13, CH14, CH15	No CH2, CH3, CH4, CH5, CH13, CH14, CH15, CH19, CH20, CH21		No CH13, CH14, CH15	No CH2, CH3, CH4, CH5, CH13, CH14, CH15, CH19, CH20, CH21			No CH2, CH3, CH11	No CH19, CH24
TSI1	Self-cap channel	25-ch TSI0[0:24]	25-ch TSI1[0:24]	NA	NA	25-ch TSI1[0:24]	25-ch TSI1[0:24]	16-ch TSI1[0-7,11-12,15-18,23-24]				NA	NA	NA	NA

Table 7. KE1xZ TSI channels for different package*...continued*

		KE17Z family with up to 512 kB Flash				KE17Z family with up to 256 kB Flash						KE15Z with up to 256 kB Flash	KE16Z family with up to 64 kB Flash		
	Mutual-cap channel	TX[0:5], RX[6:11]	TX[0:5], RX[6:11]			TX[0:5], RX[6:11]	TX[0:5], RX[6:11]	TX[0:5], RX[7,11]							
	Shield channel	Up to 25 shield channels: CH4, CH12, CH21, CH24 are enhanced TSI channels than others.	Up to 25 shield channels: CH4, CH12, CH21, CH24 are enhanced TSI channels than others.			Three shield channels: CH4, CH12, CH21	Three shield channels: CH4, CH12, CH21	Two shield channels: CH4, CH12							
	Comment							No CH8, CH9, CH10, CH13, CH14, CH19, CH20, CH21, CH22							
Datasheet		KE1xZP100M96SF0				KE1xZP100M72SF1						KE1xZP100 M72SF0	KE1xZP48M48SF0		

Figure 2 shows the assignment of dual TSI channels on the three packages of KE17Z. Compared with the KE17Z 100LQFP, the TSI channels marked in yellow are not supported in the KE17Z 64 LQFP. The ones marked in yellow and red are TSI channels not supported in K17Z 48 LQFP.

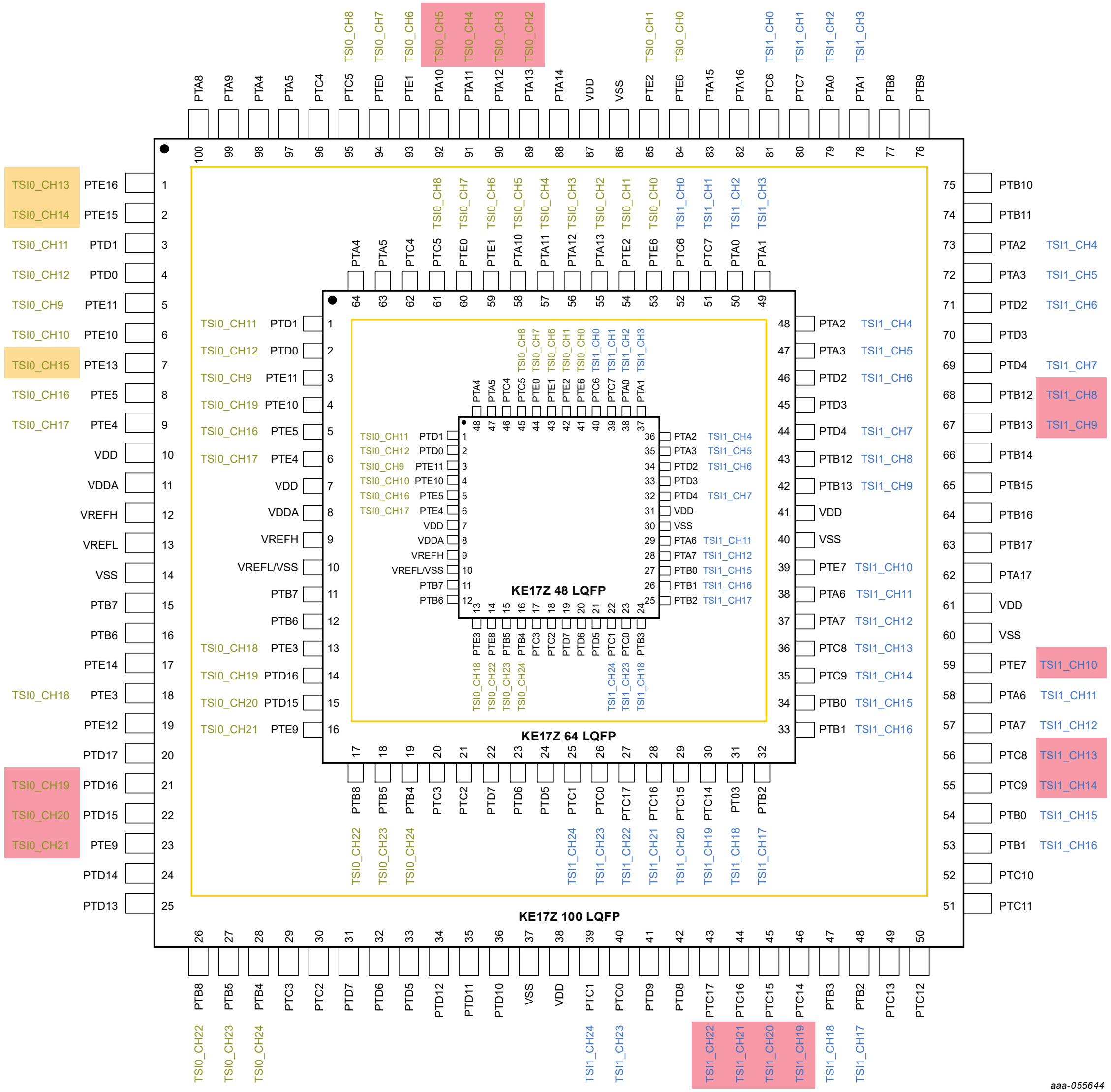

Figure 2. TSI channel assignment of KE17Z 100 LQFP, KE17Z 64 LQFP, and KE17Z 48 LQFP

For the KE17Z in 100LQFP, 64LQFP, and 48LQFP packages, its pin assignment is compatible with the KE15Z. That is, the number and position of GPIO pins are the same. But the TSI channel assignment of KE17Z is different from KE15Z. To migrate the touch code from KE15Z to KE17Z, see Figure 3, Figure 4, and Figure 5 for the TSI channel assignment. For more migration details, see the *Migration Guide from KE15Z256 to KE17Z256* (document AN13429) and the *Migration Guide from MT256P to MT512X* (document AN14202)

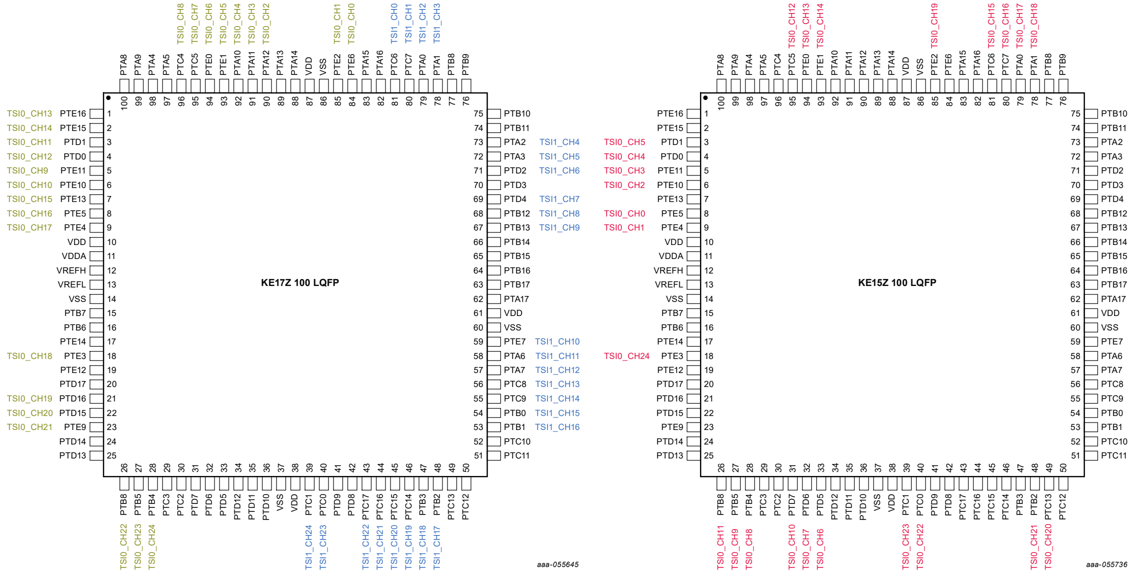

Figure 3. TSI pin assignment comparison of 100 LQFP between KE15Z and KE17Z

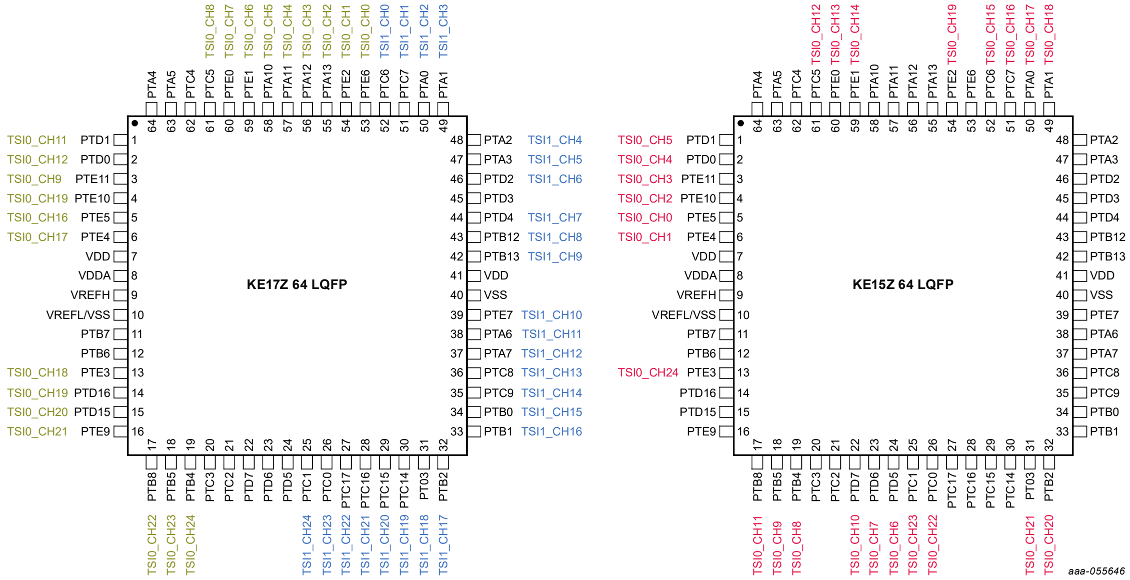

Figure 4. TSI pin assignment comparison of 64 LQFP between KE15Z and KE17Z

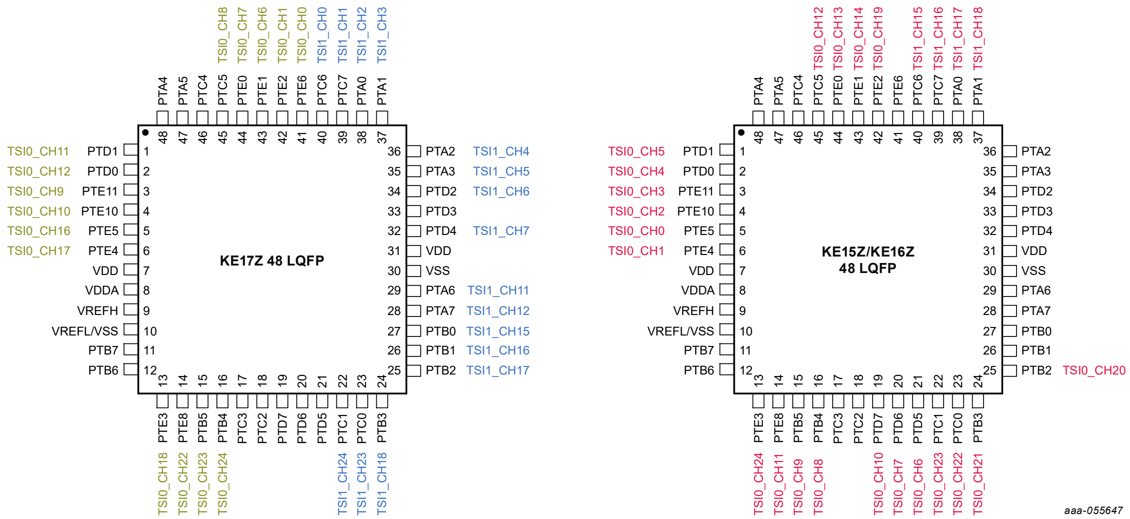

Figure 5. TSI pin assignment comparison of 48 LQFP between KE15Z/KE16Z and KE17Z

1.5 KE17Z dual TSI evaluation board

X-KE17Z-TSI-EVB is a touch sensing reference design including multiple touch patterns based on the 5 V Robust KE17Z MCU of NXP. It has dual-TSI modules and supports up to 50 touch channels, all demonstrated on the board.

Figure 6. X-KE17Z-TSI-EVB, KE17Z dual TSI evaluation board

2 TSI self-cap mode introduction

The sensor structure and electric field distribution between self-cap sensor and mutual-cap sensor are different.

2.1 Self-cap touch sensor

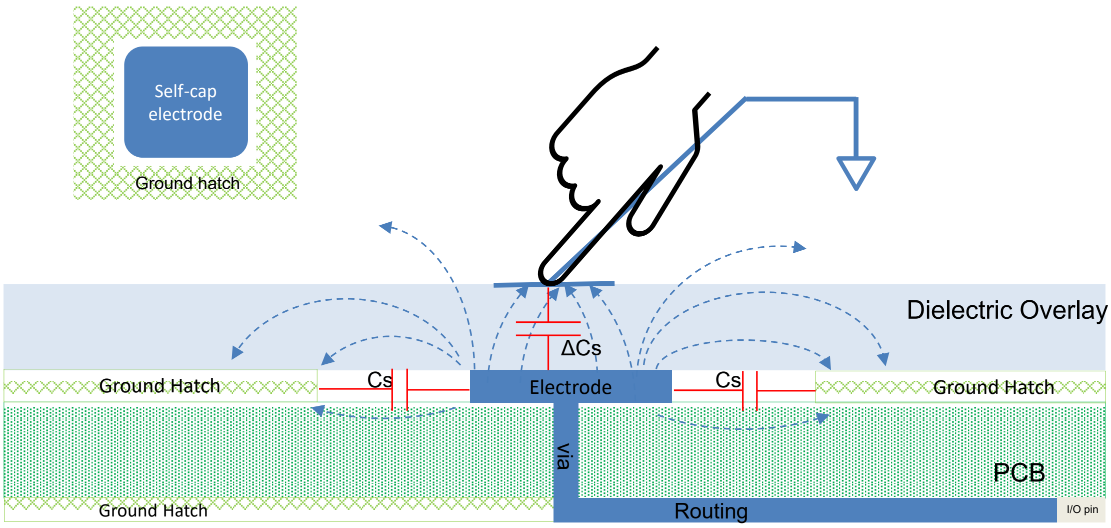

Figure 7. Self-cap touch sensor structure and electric field

In self-cap mode, TSI requires only one pin for each touch sensor. As shown in Figure 7, capacitance exists between electrode to system ground. Touch changes the field through the human body and creates extra capacitance.

Self-cap touch sensor structure:

- Cs: Intrinsic self-capacitance. 10 - 50 pF as usual.
- ΔCs: Touch generated self-capacitance. 0.3 - 2 pF as usual.
- Sensitivity of sensor: ΔCs/Cs. 1 - 10 % as usual.

2.2 Self-cap sensing mode

There are three modes of self-cap mode:

- Basic self-cap mode
- Noise cancellation mode
- Sensitivity boost mode

The noise cancellation mode and sensitivity boost mode cannot be enabled at same time. The following describes the three modes.

2.2.1 Basic self-cap sensing mode

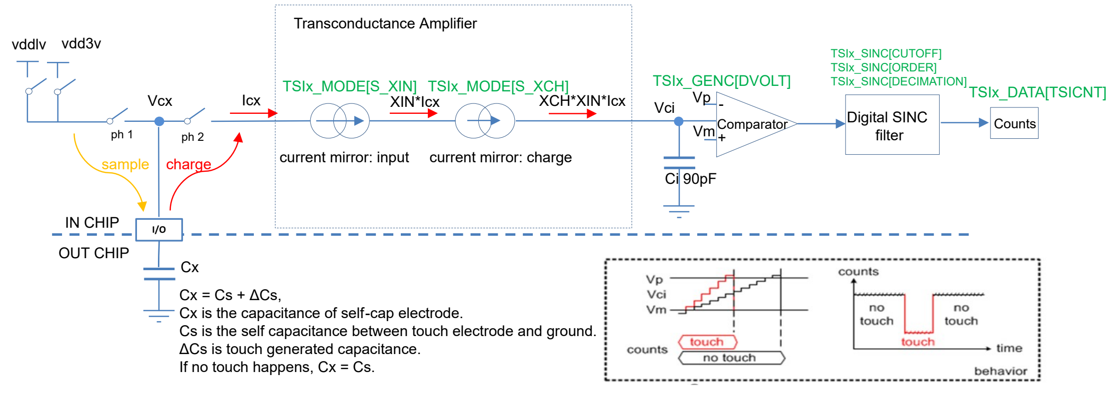

Figure 8. TSI basic self-cap mode HW architecture

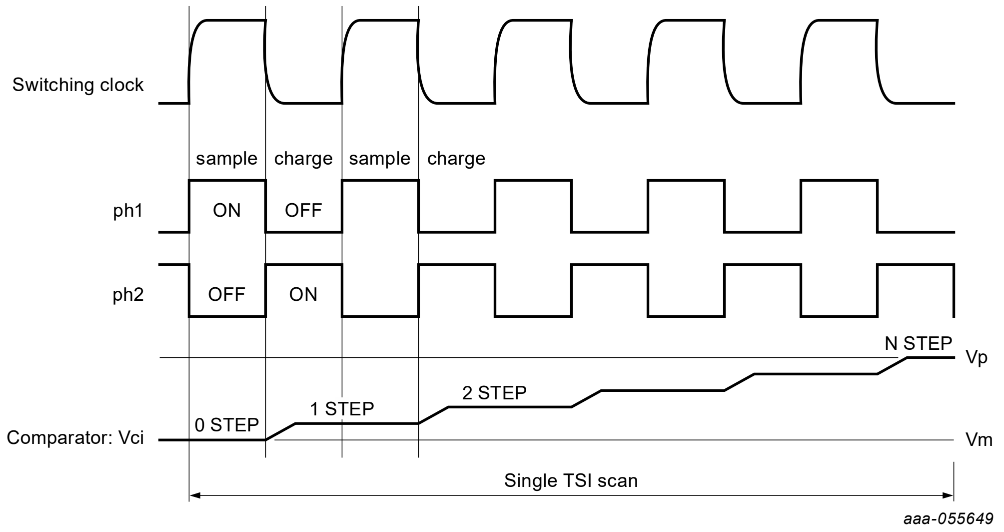

Figure 9. TSI self-cap timing

Inside the TSI IP module, the TSI scan is operated by non-overlapping clock ph1/ph2 and trans-conductance amplifier.

There are two phases controlled by the ph1 and ph2 respectively for the TSI scan module:

- Sample phase: The switch **ph1** controls the sample phase. When ph1 turns on, the external touch electrode C_x is charged by vdd3v.
- Charge phase: The switch **ph2** controls the charge phase. When ph1 turns off and then ph2 turns on, the charge on the capacitor C_x flows to the internal integrated capacitor Ci, which generates the average current I_{cx}.

Via the trans-conductance amplifier, the I_{cx} are amplified to charge Ci and the voltage V_{ci} ramps on Ci. V_{ci} is detected by the comparator, when the V_{ci} becomes larger than the pre-setting V_p, C_i is discharged to negative reference V_m. Then the next scanning cycle continues.

The digital SINC filter controls the scan cycle. The digital SINC filter is a digital decimation filter for filtering out the low frequency noise from EMC. The digital SINC detects and accumulates the filter number of V_{ci} ramp up steps in per cycle. The digital SINC filter outputs the total counter, which can be read from `TSIx_DATA[TSICNT]`. The software uses the counts to detect touch.

When touch happens, input capacitance C_x increases. The charging current of C_i becomes larger and then the number of V_{ci} ramp up steps is reduced. The output count of the digital SINC filter is reduced, so the value of `TSIx_DATA[TSICNT]` is decreased.

2.2.2 Noise cancellation mode of self-cap

If the touch sensor encounters strong low frequency noise, noise cancellation can be activated by setting `TSIx_MODE[S_NOISE]`.

In the noise cancellation mode, vdd3v, and vddlv (1.2 V) are dual sample voltages. Two phases exist in noise cancellation architecture:

- Charging phase of C_i when vdd3v is on and vddlv is off
- Discharging phase of C_i when vdd3v is off and vddlv is on

Two switching clock cycles cost to samples twice, which includes charging phase (sampling vdd3v) and discharging phase (sampling vddlv). The input current of C_i equals to the charging phase current abstract discharging phase current. At the end of each second phase, low frequency noise is subtracted. In a long integration period, the noise induced error can be canceled.

2.2.3 Sensitivity boost mode of self-cap

The larger parasitic capacitance causes the low sensitivity. The low sensitivity results in the difficulty to recognize the touch event. For example, when the touch overlay is thick, it becomes hard to detect a touch event correctly.

To increase the sensitivity, enable a sensitivity-boost feature by removing part parasitic capacitance virtually. So, the touch works well under the thicker overlay with sensitivity boost enabled.

Note: *The capacitance to be removed cannot be configured more than the intrinsic capacitance of the touch key. Otherwise, it causes the sensitivity invalid.*

2.3 Clock generation

The clock generation determines the TSI scan speed. The maximum frequency of TSI is about 10 MHz.

The TSI module is only clocked by the main clock, which is generated by the TSI module itself without any other external clock source. The main clock has four ranges of frequency. It can be divided into the switching clock, which is used to control the ph1/ph2 switching speed and finally determines the whole scan time, as shown in Figure 10.

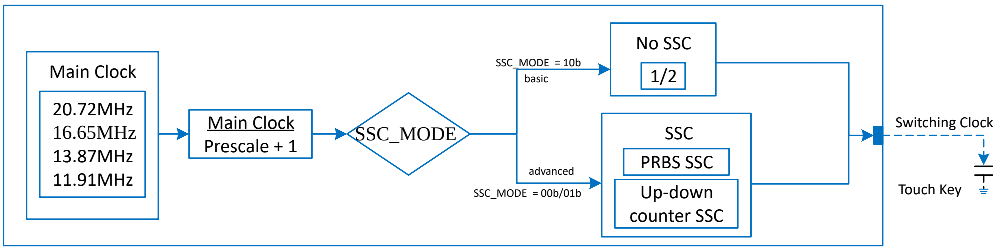

Figure 10. Block diagram of clock generation

- When SSC_MODE = 10b, the switching clock is divided from the main clock directly, as the basic clock generation.
- When SSC_MODE = 00b/01b, the switching clock is generated from the SSC module, as the advanced clock generation.

2.3.1 Basic clock generation

Equation 1 is the basic clock generation, when TSIx_SSC0[SSC_MODE] = 10b.

$$Switching\ Clock = \frac{Main\ Clock}{SSC\_PRESCALE\_NUM + 1} \times \frac{1}{2} \quad (1)$$

Table 8. Main clock setting

Register	Value	Main clock (MHz)
TSI_MODE[SETCLK]	00	20.72
	01	16.65
	10	13.87
	11	11.91

Table 9. Divider setting

Register	Value	SSC_PRESCALE_NUM + 1
TSI_SSC0.SSC_PRESCALE_NUM[7:0]	00000000	divide 1
	00000001	divide 2
	…	…
	11111111	divide 256

There is an example of the basic clock generation, the main clock as 16.65 MHz, the divider as 16, and the result of switching clock is 1.04 MHz.

To use no SSC switching clock with a frequency of 1 MHz,

- Set SETCLK < 1:0 > to **01b** to get the main clock = 16.65 MHz.
- Set SSC_MODE < 1:0 > to **10b** to disable the SSC function.
- Set SSC_PRESCALE_NUM < 7:0 > to **00000111b** to get division 8. When SSC mode is disabled, the frequency is ***main clock/[(SSC_PRESCALE_NUM+1) × 2]***.
- Keep other registers in `TSIx_SSC0`, `TSIx_SSC1`, and `TSIx_SSC2` as the default value.

$$Switching\ Clock = \frac{Main\ Clock}{Divider} \times \frac{1}{2} = \frac{16.65\ MHz}{8} \times \frac{1}{2} = 1.04\ MHz \quad (2)$$

2.3.2 Advanced clock generation, spread spectrum clocking

The Spread Spectrum Clocking (SSC) increases the noise immunity to RF interference and spreads the emissions.

With the SSC enabled (TSIx_SSC0[SSC_MODE] = 00/01b), the switching clock is generated by the SSC module, other than the direct divided main clock.

In the Self-cap mode, changing the SSC charge time does not affect the final scan result. It changes the total scan time as it changes the switching clock frequency.

If SSC mode is enabled, the timing of the switching clock generation is as shown in Figure 11.

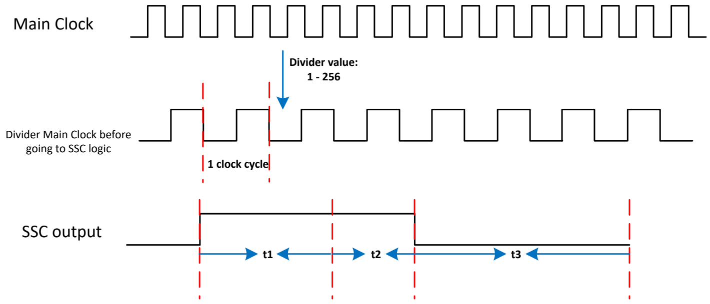

Figure 11. Timing of the advance clock generation with SSC enabled

As shown in Figure 11, t1 and t2 determine the SSC output 1's period and t3 determines the SSC output 0's period.

Equation 3 shows the advanced clock generation, with SSC enabled when TSIx_SSC0[SSC_MODE] = 00/01b.

$$Switching\ Clock = \frac{Main\ Clock}{(SSC\_PRESCALE\_NUM + 1) \times [t1+t2+t3]} \quad (3)$$

- When TSIx_SSC0[SSC_MODE] = 00b, t2 can be random (PRBS).
- When TSIx_SSC0[SSC_MODE] = 01b, t2 can be the range of TSIx_SSC2[MOVE_NOCHARGE_MIN] to TSIx_SSC2[MOVE_NOCHARGE_MAX].

The generation of the switching clock includes:

- The switching clock can be generated as a pseudo random clock using the Pseudo-Random Binary Sequence (PRBS) method by setting TSI_SSC0[SSC_MODE] = 00. t2 is configured as the random width.

Table 10. TSI_SSC0[SSC_MODE] = 00, PRBS mode

Variable	Register	Clock cycle	Description
t1	TSIx_SSC0[BASE_NOCHARGE_NUM]	1 - 16	SSCHighWidth
t2	TSIx_SSC0[PRBS_OUTSEL]	2 - 15	SSCHighRandomWidth
t3	TSIx_SSC0[CHARGE_NUM]	1 - 16	SSCLowWidth

- Switching Clock can be generated in a configurable up-down counter method by setting TSI_SSC0[SSC_MODE] = 01. The range of t2 is limited by `TSI_SSC2[MOVE_NOCHARGE_MIN]` and `TSI_SSC2[MOVE_NOCHARGE_MAX]`.

Table 11. TSI_SSC0[SSC_MODE] = 01, up-down counter mode

Variable	Register	Clock cycle	Description
t1	TSI_SSC0[BASE_NOCHARGE_NUM]	1 - 16	SSCHighWidth
t2	TSI_SSC2[MOVE_NOCHARGE_MIN] TSI_SSC2[MOVE_NOCHARGE_MAX]	MAX-MIN	SSCHighCounterWidth
t3	TSI_SSC0[CHARGE_NUM]	1 ~ 16	SSCLowWidth

There is an example of the advance clock generation attached below.

To use PRBS mode SSC switching clock with a central frequency of 1 MHz.

- Set `SETCLK<1:0>` to **01b** to get the main clock = 16.65 MHz.
- Set `SSC_PRESCALE_NUM<7:0>` to **0b** to get division 1. The divided main clock is 16.65 MHz.
- Set `SSC_MODE<1:0>` to **00b** to enable PRBS SSC mode. SSC t2 is random.
- Set `BASE_NOCHARGE_NUM<3:0>` to **0100b** to set t1 = 5. The basic length of SSC output bit 1's period is five clock cycle of the divided main clock.

- Set `PRBS_OUTSEL<3:0>` to **0110b** to set the t2 range from 1 to 6. The average of t2 is 3.5. t2 is the random length of SSC output bit 1's period. It is a 3.5 clock cycle of the divided main clock.
- Set `CHARGE_NUM<3:0>` to **0110b** to set t3 = 7. The basic length of SSC output bit 1's period is seven clock cycle of the divided main clock.
- Keep other registers in `TSIx_SSC0`, `TSIx_SSC1`, and `TSIx_SSC2` as default value.
- Then, the switching clock = 16.65 MHz/[(5+3.5+7) * (0 + 1)] = 1.074 MHz. The switching clock is spectrum spread pulse.

$$Switching\ Clock = \frac{Main\ Clock}{(SSC\_PRESCALE\_NUM + 1) \times [SSCHighWidth(t1) + SSCHighRandomWidth(t2) + SSCLowWidth(t3)]} = \frac{16.65MHz}{(0+1) \times (5+3.5+7)} = 1.074MHz \quad (4)$$

2.4 TSI scan time and scan result accumulation

TSI supports multiple scans per channel. That is, to get better Signal-to-Noise Ratio (SNR) and resolution, TSI performs multiple scans. The final scan result is accumulated in `TSI_DATA[TSICNT]` counter as the NSTEP multiplied by the number of scans, and the scan time is multiple of single TSI scan time.

Note:

*With higher **Decimation**, the number of scans is increased. The result is the physically longer TSI counter accumulation and increased resolution.*

*If the **Order** is higher than 1, then the scan number physically executed by TSI is smaller than the scan number calculated by HW. It is beneficial to get the higher resolution.*

2.4.1 TSI single scan process

Figure 12 shows one process that the step voltage (V_{ci}) reaches threshold V_p of comparator from V_m. If V_{ci} reaches the threshold V_p, the voltage VCI is discharged to V_m for next scanning. The step voltage (V_{ci}) depends on touch sensor and IP configuration.

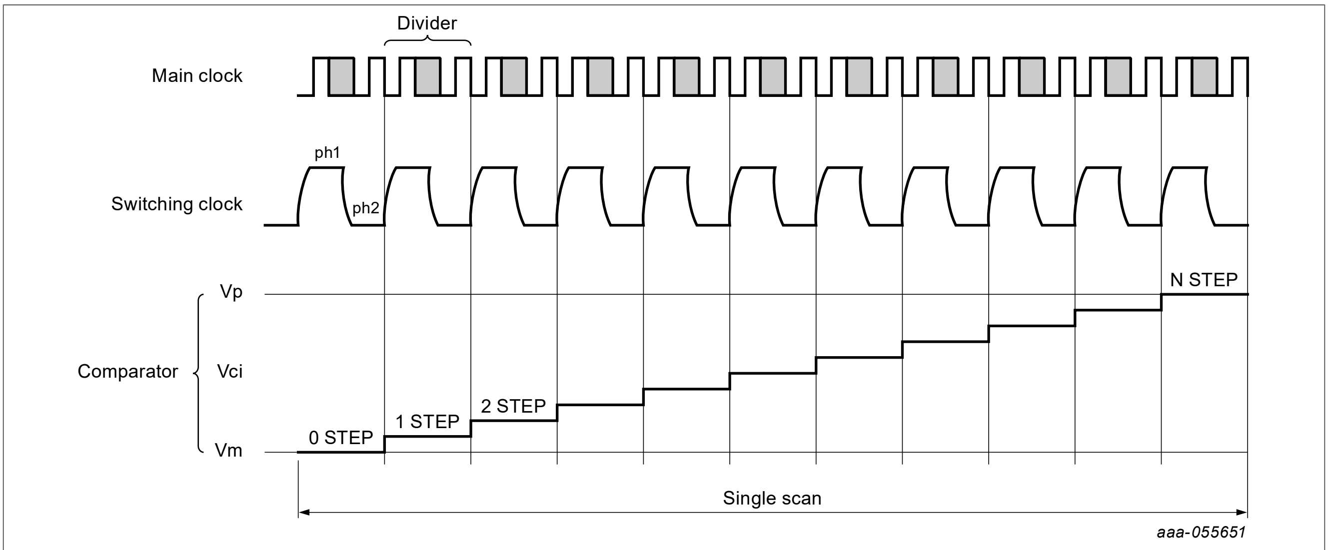

Figure 12. One process of the step voltage (Vci) reach threshold Vp of comparator

1. Calculate NSTEP in basic self-cap mode.
   Equation 5 is the basic equation of the self-cap mode. NSTEP is the V_{ci} steps of TSI single scan in self-cap mode.

$$NSTEP = \frac{Ci \times (Vp - Vm)}{vdd3v \times Cs \times S\_XIN \times S\_XCH} \quad (5)$$

Equation 6 is the basic equation of the scan time. T_{nstep} is the time cost of TSI single scan in **self-cap mode**.

$$Tnstep = NSTEP \times \frac{1}{Fsw} \tag{6}$$

- C_i: Typical 90 pF. The integrated capacitance inside the TSI module.
- Vdd3v: Typical 3.3 V. PMC internal voltage regulator generates the analog power supply voltage.
- V_p, V_m: Configurable, dual reference voltage, which can be configured by TSIx_GENCS[DVOLT].
- S_XIN, S_XCH: Configurable, the parameters of analog front end, configured TSIx_MODE[S_XIN], TSIx_MODE[S_XCH].
- F_{sw}: Configurable, the switching clock frequency.
- C_s: The self-capacitance of touch sensor.

2. Equation 7 is a new equation to calculate NSTEP when noise cancellation mode is enabled.

$$NSTEP = \frac{2 \times Ci \times (Vp - Vm)}{(vdd3v - vddlv) \times Cs \times S\_XIN \times S\_XCH} \tag{7}$$

Vddlv: The internal power supply voltage. Typical 1.2 V.

3. Calculate NSTEP in basic self-cap mode.
The TSI self-cap mode implements the sensitivity boost by canceling the external intrinsic capacitance. The value of the capacitance to be canceled ranges from 2.5 pF to 20 pF, which is configurable in register `TSI_MODE[S_CTRIM]`.
For example, given the intrinsic capacitance of the touch electrode is 20 pF (it can be calculated by NSTEP equation), setting the `S_CTRIM` value as 5.0 pF can make the effective intrinsic capacitance become 15 pF. As the intrinsic sensitivity of the touch key is given by ΔCs/Cs, the less intrinsic capacitance would result in more sensitive touch response. With this sensitivity boost enabled, sensitivity can be improved to ΔCs/ (Cs-S_CTRIM*(S_XDN/S_XCH)).
The sensitivity boost feature in self-cap mode can be activated by setting `TSI_MODE[S_SEN]`. Equation 8 is a new equation to calculate NSTEP when sensitivity boost function is enabled.

$$NESTP = \frac{Ci \times (Vp - Vm)}{vdd3v \times (Cs - S\_CTRIM \times (S\_XDN / S\_XCH)) \times S\_XIN \times S\_XCH} \tag{8}$$

- `S_CTRIM`: Configurable, the capacitance to be removed.
- `S_XDN/S_XCH`: Configurable, the capacitance multiplier.
- The actual capacitance to be removed is S_CTRIM × (S_XDN/S_XCH).

2.4.2 TSI scan multiple rounds in self-cap mode

To minimize the noise deviation on the single scan, TSI supports multiple scans per channel. That is, TSI performs a single scan operation for many times from getting the trigger to the end of the scan.

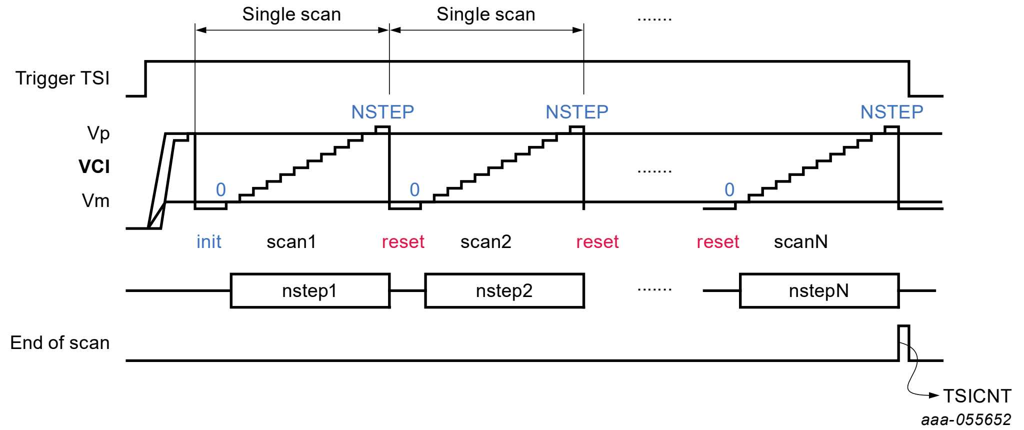

Figure 13. Multiple scans per channel

Each time the TSI is triggered, multiple scans can be performed inside the TSI. The scan round is set by the registers (`TSI_SINC[DECIMATION]`, `[ORDER]`, and `[CUTOFF]`), ranged from 1 to 32^2. When the `TSI_SINC[DECIMATION]` is set to **0** (only once), the single scan is engaged.

The 16-bit counter accumulates all scan results until the scan number reaches a predefined number. To get the final scan result, read `TSI_DATA[TSICNT]`.

There are two kinds of scan number:

- For digital calculation to accumulate the final TSI scan result, as shown in Equation 7.
- For TSI IP to execute the scan action practically, as shown in Equation 8.

$$Scan\ \ Result: \qquad TSICNT = NSTEP \times \frac{Decimation^{Order}}{Cutoff} \tag{9}$$

$$Scan\ \ Time: \qquad Time = \ Tnstep \times Decimation \ \times \ Order \tag{10}$$

According to Equation 5, Equation 6, Equation 9, and Equation 10, the parameters of Decimation, Order and Cutoff, `S_XIN`, `S_XCH`, and (Vp -Vm) affect the final accumulated scan result and the total scan time.

Users must adjust the touch electrode according to different applications. The parameters of TSI can be adjusted comprehensively to achieve the best performance of TSI.

For example,

- Increase the voltage of (Vp-Vm) can reduce the effect of low frequency noise, but the scan time of TSI increases. The increase of `S_XCH` and `S_XIN` can increase the charging current of C_i and shorten the scan time of TSI, but the noise increases. Therefore, when (Vp-Vm) increases, `S_XCH` and `S_XIN` can be reduced, which cannot only reduce the scanning time but also reduce the noise and enhance the sensitivity.
- Decimation, Order, and Cutoff increase the number of scans for the touch electrodes and enhance the anti-interference of the electrodes. At the same time, the scan time of the touch electrodes is also longer. Setting the Order as 2 is recommended as it can save scan time to achieve the same digital scan result.

2.5 Scan time and sensitivity boost tests in self-cap mode

2.5.1 Scan time test in self-cap mode

This chapter shows the one self-cap touch electrode scan time test results on X-KE17Z-TSI-EVB.

As shown in Table 12, given the NSTEP is 110 and Tnstep is 239 us by the measurement result of a single scan, shown as Example 1. The theoretical value can be calculated by Equation 9 and Equation 10.

Table 12. Scan time test by changing the configuration of Decimation, Order, Cutoff

	Switching Clock (MHz)	NSTEP	Tnstep (µs)	Configurations			Result			
				Decimation	Order	Cutoff	NSTEP Multiple	Counter (TSICNT)[1]	Real Scan Round	Scan Time[2] (µs)
1	0.52			**1**	1	1	1	**110**	**1**	**239**
2	0.52	110	239	**2**	1	1	2	**220**	**2**	**448**
3	0.52	110	239	**4**	1	1	4	**440**	**4**	**869**
4	0.52	110	239	**8**	1	1	8	**880**	**8**	**1709**
5	0.52	110	239	**16**	1	1	16	**1760**	**16**	**3390**
6	0.52	110	239	**32**	1	1	32	**3520**	**32**	**6750**
7	0.52	110	239	1	**2**	1	1	**110**	2	**449**

Table 12. Scan time test by changing the configuration of Decimation, Order, Cutoff...*continued*

	Switching Clock (MHz)	NSTEP	Tnstep (µs)	Configurations			Result			
				Decimation	Order	Cutoff	NSTEP Multiple	Counter (TSICNT)[1]	Real Scan Round	Scan Time[2] (µs)
8	0.52	110	239	2	**2**	1	4	**440**	4	**869**
9	0.52	110	239	4	**2**	1	16	**1760**	8	**1709**
10	0.52	110	239	8	**2**	1	64	**7040**	16	**3390**
11	0.52	110	239	8	2	**2**	32	**3520**	16	**3390**

[1] The **Counter (TSICNT)** is read from the register when debugging the code.
[2] The actual **Scan time** is calculated by LPTMR module.

- Other conditions: Ci, 90 pF; vdd3v, 3.3 V; S_XIN, 1/4; S_XCH, 1/2.
- Example 1: Configure the Decimation, Order, and Cutoff as 1, and the final scan result is 110. TSI performs a scan operation for one time, and the scan time is 239 µs.
- Example 2: Change the Decimation to 2, and the final scan result becomes 220. TSI performs the scan twice, and the scan time is 448, about twice of the previous 239 µs.
- Example 10: Change the order to 2, and the final scan result becomes 110 * 64 = 7040. TSI only performs a scan for 8 * 2 = 16 times, and the scan time is 3390 µs, saving time by setting order = 2.

By comparing the test results when setting order to 1 and order to 2, the conclusion is:

Increasing TSI conversion result (TSICNT) means to cost longer scan time. When TSI performs multiple scans, it is recommended to set order to 2 to reduce interference and save touch electrode scan time. Then change the Decimation and Cutoff to adjust the TSI conversion result. Increasing TSI conversion result means longer scan time.

The scan time in this table is measured by the LPTMR module. That is, start LPTMR on the TSI scan start, stop LPTMR on the TSI scan end, and then read the LPTMR counter to estimate the time cost. There are some inevitable small errors and differences between LPTMR measurement and real TSI scan time.

2.5.2 Sensitivity test result when sensitivity boost feature is enable

When the sensitivity boost function is enabled, NSTEP is calculated by Equation 8, and the calculation of TSICNT and scan time still uses Equation 9 and Equation 10.

The sensitivity boost configurations include: `S_SEN` Enable, `S_CTRIM`, and Multiplier (`S_XDN/S_XCH`).

Table 13. Sensitivity boost configurations registers

Variable	Register	Descriptions
S_SEN Enable	TSI_MODE[S_SEN]	Enable a sensitivity boost by setting `S_SEN` to 1.
S_CTRIM	TSI_MODE[S_CTRIM]	Remove the parasitic capacitance virtually, from 2.5 pF to 20 pF.
Multiplier: S_XDN/ S_XCH	TSI_MODE[S_XDN]	Multiplier factor when sensitivity boost is enabled.
	TSI_MODE[S_XCH]	Charge/discharge multiple

The removed capacitance is:

$$Cremoved = S_{CTRIM} \times \frac{S_{XDN}}{S_{XCH}} \tag{11}$$

Table 14. Sensitivity test for sensitivity boost configurations

Current Amplifier			Sensitivity Boost				Intrinsic capacitance calculated Cx	Sensitivity calculated (%)
S_XIN	S_XCH	Current Amplifier (S_XIN*S_XCH)	S_SEN Enable	S_XDN	S_Ctrim (pF)	$C_{removed}$ (pF)		
1/4	1/2	1/8	**OFF**	1/2	2.5	**0.0**	16	**11.6**
1/4	1/2	1/8	ON	1/2	2.5	**2.5**	16	**12.5**
1/4	1/2	1/8	ON	1/2	5.0	**5.0**	16	**15.0**
1/4	1/2	1/8	ON	1/2	7.5	**7.5**	16	**22.2**
1/4	1/2	1/8	ON	1/2	10.0	**10.0**	16	**28.2**
1/4	1/2	1/8	ON	1/2	12.5	**12.5**	15	**43.8**

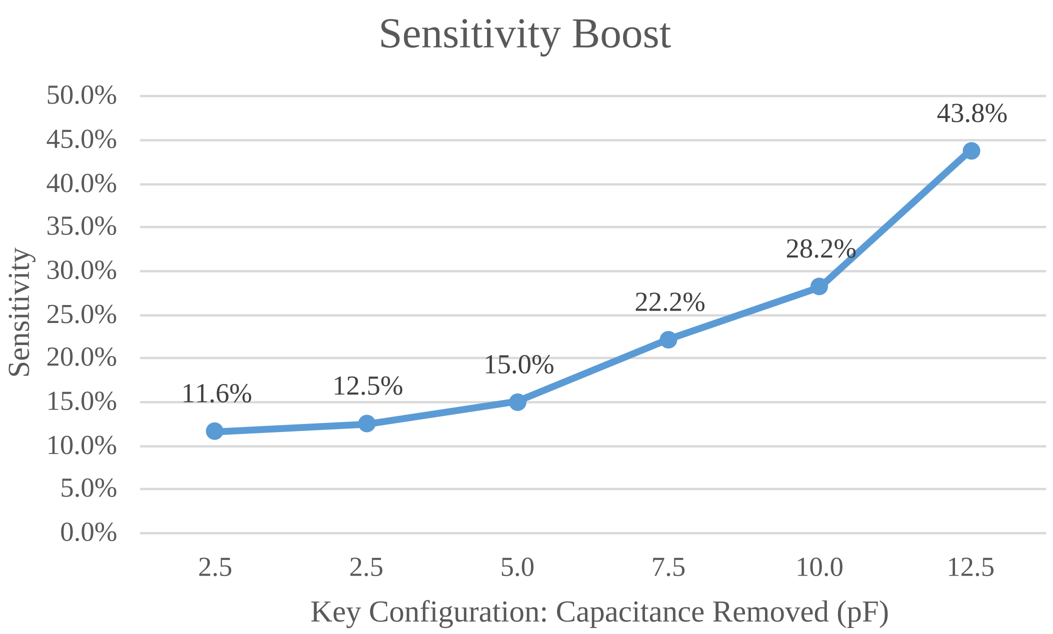

Figure 14. Sensitivity curve

From sensitivity calculate results, we can find out that the $C_{removed}$ is the key configuration to the sensitivity boost feature. As $C_{removed}$ increases, the sensitivity becomes better. That is, it is to recognize touch event. Therefore, users can adjust the `S_CTRIM` and `S_XDN` to quickly adjust the sensitivity of touch electrode recognition.

Figure 15 shows the definition of the sensitivity.

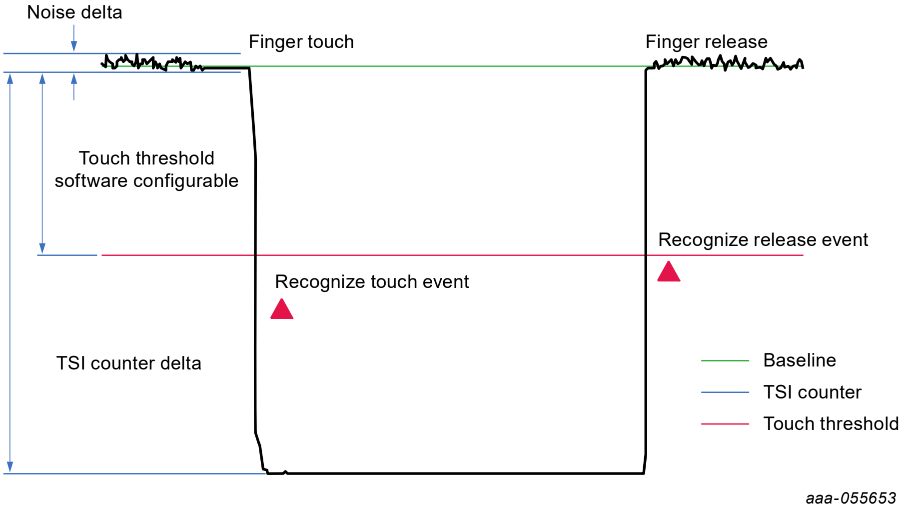

Figure 15. TSI sensitivity definition

$$Sensitivity = \frac{TSI\_Counter\_Delter}{TSI\_Baseline} \times 100\% \quad (12)$$

The large sensitivity value means the stronger signal caused by finger touch.

Sensitivity around 10 % is recommended in self-cap mode.

3 TSI mutual-cap mode

3.1 Mutual-cap sensor

Mutual-cap mode measures the capacitance between two electrodes connected to two TSI channels. One of the TSI channels is used as transmit (TX) channel and the other one is used as receive (RX) channel.

For the two TSI instances of KE17Z, `TSIx[5:0]` can be used as TX channel by configuring `TSIx_MUL0[M_SEL_TX]`. `TSIx[11:6]` can be used as RX channel by configuring `TSIx_MUL0[M_SEL_RX]`. The mutual-cap touch electrode design of TSI0 and TSI1 is independent. Each TSI instance supports the design of 6 × 6 touch electrodes.

Touch changes the field through the human body and reduces the mutual capacitance. TSI IP is to convert the capacitance changing from the sensor to digital code for application.

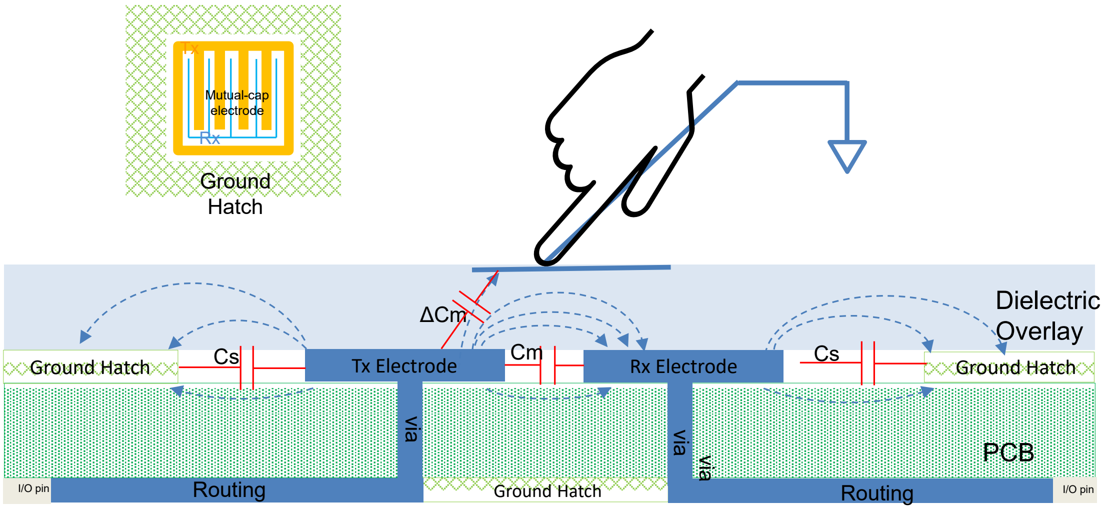

Figure 16. Mutual-cap touch sensor structure and electric field

Sensor structure:

- Cm: Intrinsic mutual cap. 2 - 10 pF as usual.
- ΔCm: Touch reduced mutual cap. 0.3 - 2 pF as usual.
- Cs: Parasitic self-cap. 10 - 50 pF as usual.
- Sensitivity of sensor: ΔCm/Cm. 1 - 20 % as usual.

3.2 Clock generation in mutual-cap mode

One difference to the self-mode clock, the **SSC** must be enabled for mutual mode to generate a switching clock, because the TSI RX signal in the mutual mode depends on the `TSI_SSC0[CHARGE_NUM]`. In the mutual mode, changing the SSC charge time changes the RX signal coupled from the TX channel and affects the final scan result.

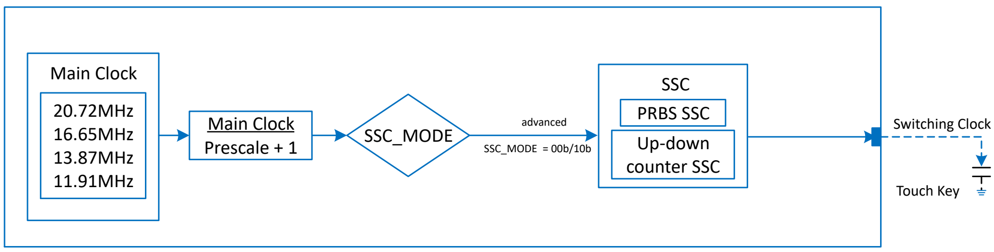

Figure 17. Clock generation in mutual-cap mode, spread spectrum clocking

SSC is enabled, the mutual mode shares the clock generation of the self-cap mode. For detailed configurations, see Section 2.3.2.

Equation 3 is used to calculate the Switching Clock when SSC is enabled.

3.3 Mutual-cap sensing mode

Mutual-cap sensing includes transmitter and receiver. Under clocking, the transmitter outputs pulses, which decouple through a mutual cap then reach the receiver site. The receiver amplifies the signal with a noise cancellation method. The method is similar as a charge transfer circuit in self-cap sensing. That is, convert to averaging charge current on integration cap C_i, which creates step voltage V_{ci}.

The step number of each scanning is accumulated to give a final count TSICNT for each trigger.

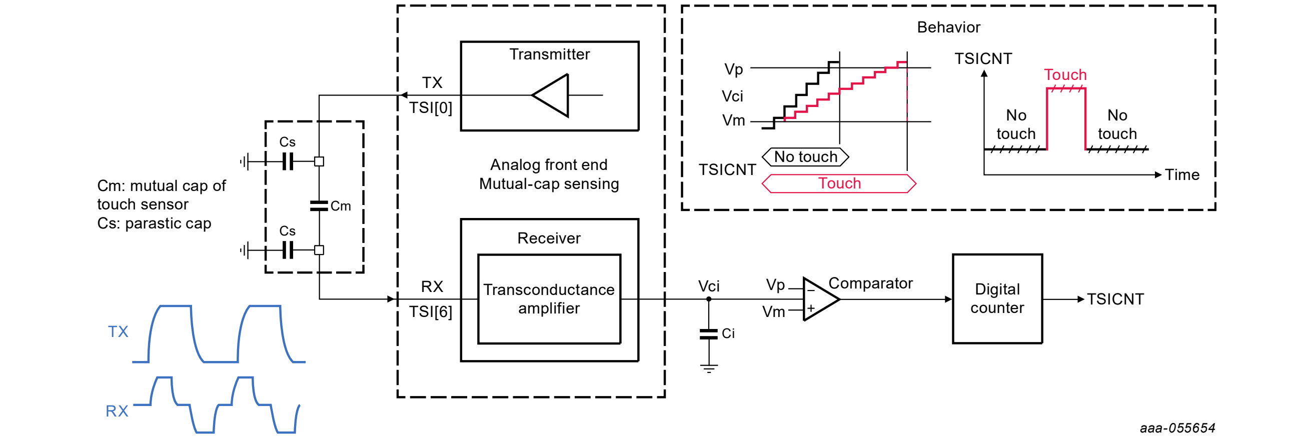

Figure 18. Block diagram of TSI mutual-cap mode

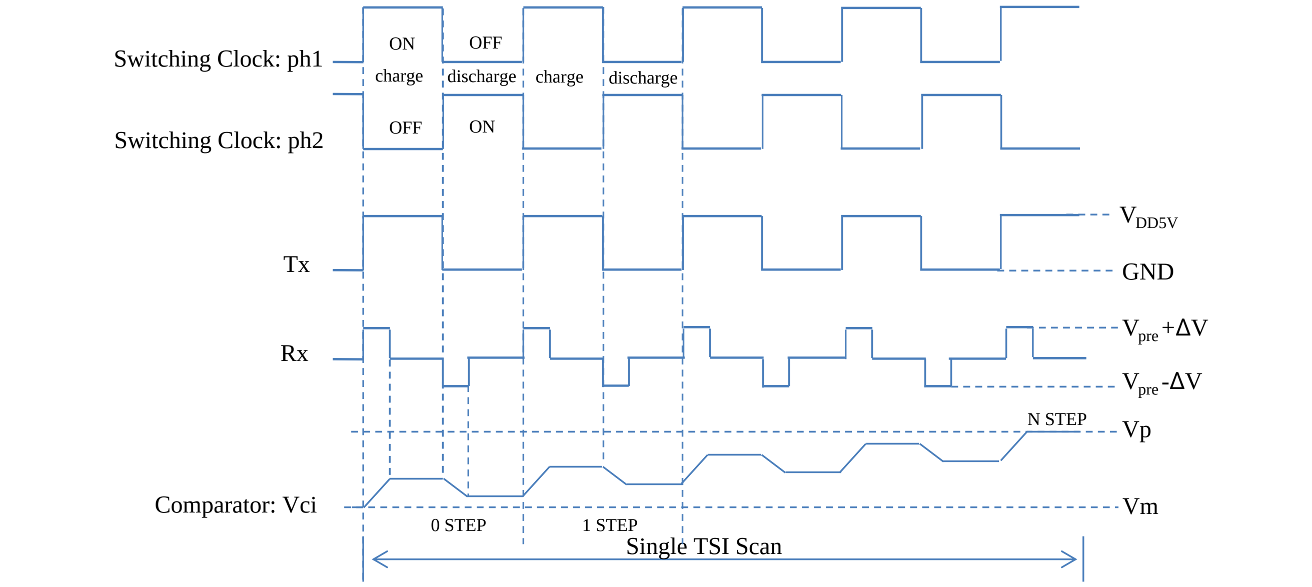

Figure 19. Mutual capacitive mode timing

- V_{pre} is selected by `TSIx_MUL1[M_VPRE_CHOOSE]`.
- ΔV: signal voltage RX received, decided by VDD5V × $C_m/(C_m + C_s)$.
- TX drive mode is controlled by TSIx_MUL1[M_MOD], -5 - +5 V is selected in Figure 19.

As shown in Figure 18 and Figure 19, there are two phases controlled by the switching clock for the TSI mutual capacitive mode:

- Charge phase: The switch ph1 controls the charge phase, when ph1 turns on, the transmit channel outputs pulses, which are coupled through the mutual capacitance C_m. Receiver converts the received voltage pulse (V_{pre} + ΔV) to the current I_{charge} through the resistor R_s.
- Discharge phase: The switch ph2 controls the discharge phase, when ph1 turns off then ph2 turns on, the transmit channel changes the voltage from V_{DD5V} to -V_{DD5V}, as TX drive mode is selected to output -5 - +5 V by configuring `M_MOD` to 1. Receiver converts the received voltage change (Vpre-ΔV) to the current $I_{discharge}$ through Rs.

As the integrated C_i is charged/discharged by the mirrored/amplified current from the receiver, the voltage V_{ci} ramps on C_i. When V_{ci} becomes larger than the pre-setting V_p, the comparator stops this TSI scan round. TSI can scan multiple rounds by configuring the digital SINC filter (`TSIx_SINC`) to filter out the low frequency noise. Accumulated sample results are recorded the as `TSIx_DATA[TSICNT]`.

There are two drive modes of Transmitter. Figure 20 shows the difference. In one switching clock cycle, when M_MODE = 1, the voltage change value of RX terminal is ΔV. When M_MODE = 0, the voltage change value of RX terminal is 2 * ΔV, and the charging efficiency of Ci is also twice M_MODE = 1. Setting `M_MODE` to **0** is recommended as it is more energy efficient.

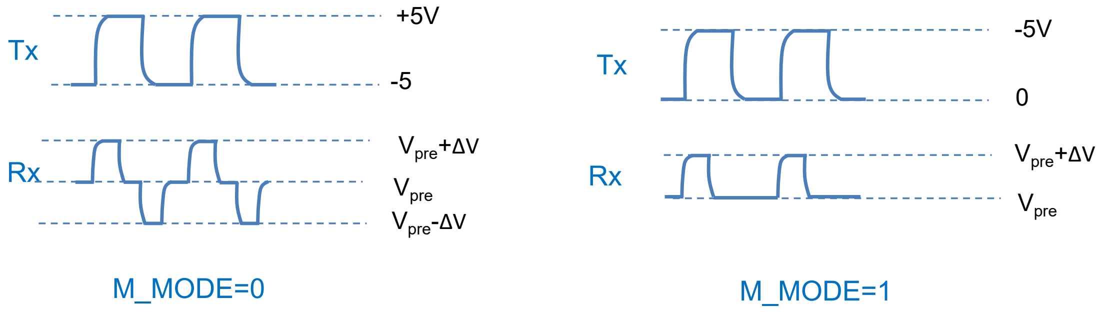

Figure 20. TX drive mode

3.3.1 Single scan in mutual-cap mode

The digital process in mutual mode is same as self-cap mode, as shown in Figure 12 and Figure 13. C_i ramp up steps in per cycle is detected and accumulated by digital SINC filter. Digital SINC filter outputs totally counter which can be read from TSIx_DATA[TSICNT].

NSTEP is the result of TSI single scan in mutual-cap mode, as shown in Equation 13.

$$NSTEP = \frac{Ci \times (Vp - Vm) \times Rs}{\Delta V} \times \frac{M\_PMIRRORL}{M\_PMIRRORR} \times \frac{1}{t3} \quad (13)$$

- Ci: Fixed 90 pF, the integrated capacitance inside TSI module.
- V_p, V_m: Configurable, dual reference voltage which can be configured by DVOLT<1:0>.
- R_s: Configurable, parameter of analog front end which can be configured by M_SEN_RES<3:0>.
- M_PMIRRORL, M_PMIRRORR: Configurable, the current multiplier.
- t3: Configurable, SSC output low period.
- ΔV: Signal voltage RX received, decided by VDD5V × $C_m/(C_m+C_s)$
  C_m is the mutual capacitance between the TX and RX touch electrode. C_s is the parasitic capacitance of the touch electrodes. When the mutual-cap electrode is touched, C_m is decreased, C_s is increased, and ΔV is reduced. The value of NSTEP is increased and the accumulated sample results TSICNT also increase. Equation 14 is the basic equation of the scan time. T_{nstep} is the time cost of TSI single scan.

$$Tnestp = \frac{Ci \times (Vp - Vm) \times Rs}{\Delta V} \times \frac{M\_PMIRRORL}{M\_PMIRRORR} \times \frac{1}{t3} \times \frac{1}{Fsw} \quad (14)$$

- F_{sw}: Configurable, the switching clock frequency in mutual-cap mode.

3.3.2 TSI scan multiple rounds in mutual-cap mode

Same with the self-cap mode, the scan round in mutual-cap mode is set by the registers (TSI_SINC[DECIMATION], [ORDER], and [CUTOFF]), ranged from 1 to 32^2. The scan result and the scan time can be calculated with Equation 9 and Equation 10.

There is an example to calculate the scan result and scan time in mutual-cap mode.

Test cases:

1. ΔV =100 mV, Rs=10k, Vp-Vm=1 V, Ci=90 pF, M_PMIRRORL = 8, M_PMIRRORR = M_NMIRROR= 2, Tsw = 1 µs, t3=0.25 µs.
   Use Equation 13 and Equation 14 to calculate:
   NSTEP = 144, TNSTEP = 144 µs.
2. Dec = 8, Order = 2, Cutoff = 1:
   Use Equation 9 and Equation 10 to calculate:
   TSICNT = 144 × 64 = 9216, SCANTIME = 144 us × 8 × 2 = 2304 µs.

Note: *When using the mutual-cap mode, keep M_PMIRRORR and M_NMIRROR same.*

3.3.3 Scan time test in mutual-cap mode

The scan time determines how long the TSI finishes the scan and get conversion result.

Similar to the Self-cap mode configurations, the mutual mode also supports multiple scan rounds per channel, and the scan number is configured by TSI_SINC [DECIMATION], [ORDER], and [CUTOFF].

Table 15 shows the one mutual-cap touch electrode scan time test results on X-KE17Z-TSI-EVB. The actual **Scan Time** is calculated by LPTMR module. The **Counter (TSICNT)** is read from the register when debugging the code.

In Table 15, give the NSTEP as 388, and Tnstep is 315 µs by the measurement result of single scan, as shown in Example 1. The theoretical value can be calculated by Equation 13 and Equation 14.

There are examples for scan time configurations, as shown in Table 15. Give the NSTEP as 388, and Tnstep is 315 µs by the measurement of single scan.

By comparing Example 5 and Example 9, you can find that when the TSI scan rounds are 16, the scan time of Example 5 costs 4473 µs and the scan time of Example 9 costs 2256 µs.

Setting order = 2 saves time so that the TSI can scan more touch electrodes in the same amount of time.

Table 15. Scan time test by changing the configuration of Decimation, Order, Cutoff

	Switching clock (MHz)	NSTEP	Tnstep (µs)	Configurations			Result			
				Decimation	Order	Cutoff	NSTEP multiple	Counter (TSICNT)	Actual scan round	Real LPTMR measured
1	1.28	388	315	**1**	1	1	1	**388**	1	**315**
2	1.28	388	315	**2**	1	1	2	**780**	2	**596**
3	1.28	388	315	**4**	1	1	4	**1552**	4	**1147**
4	1.28	388	315	**8**	1	1	8	**3110**	8	**2257**
5	1.28	388	315	**16**	1	1	16	**6218**	16	**4473**
6	1.28	388	315	**32**	1	1	32	**12448**	32	**8918**
7	1.28	388	239	1	**2**	1	1	**387**	2	**593**
8	1.28	388	239	2	**2**	1	4	**1550**	4	**1145**
9	1.28	388	239	4	**2**	1	16	**6220**	8	**2256**
10	1.28	388	239	8	**2**	1	64	**24828**	16	**4475**
11	1.28	388	239	8	2	**2**	32	**12414**	16	**4463**

3.4 Sensitivity boost in mutual-cap mode

3.4.1 Sensitivity boost in mutual-cap mode

Mutual capacitive mode supports sensitivity boost.

If the mutual touch sensor intrinsic sensitivity is limited due to parasitic, the sensitivity boost feature can be activated by setting `M_SEN_BOOST`<4:0>. The basis average charge current is subtracted by boost current which enlarges the signal current.

Different to the self-cap mode, mutual-cap mode implements sensitivity boost by changing the current. It is configurable in register `TSI_MUL0[M_SEN_BOOST]`. The current value ranges from 0 µA to 62 µA.

Table 16. Sensitivity boost enable in mutual-cap mode

Variable	Register	Value	Descriptions
Sensitivity boost current	TSIx_MUL0[M_SEN_BOOST]	0 - 62 µA	Choose the sensitivity boost current to change sensitivity.

3.4.2 Sensitivity test result when sensitivity boost feature enabled

From the configuration above, we can find that the boost current is the key configuration to the sensitivity boost feature. As the boost current increases, the sensitivity becomes better. That is, it is easier to recognize touch event, as shown in Figure 21.

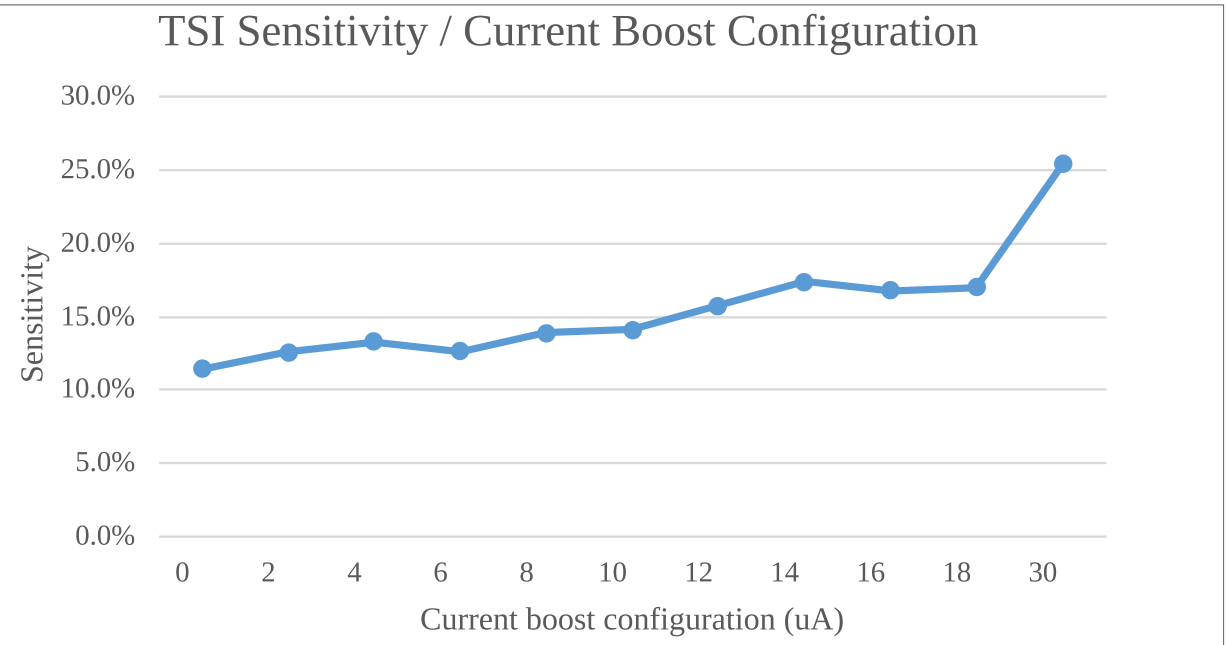

Figure 21. TSI sensitivity change curve when current boost increase

4 Shield channels

Shielding methods are used to eliminate or the environmental influences, such as temperature drifts, humidity on PCB, or water droplets on the touch control panel.

Shield electrodes can reduce mis-trigger risk induced by water drop, oil, steam, and other environmental influence. Table 1 describes the shield feature comparison between the KE17Z512 series and KE17Z256 series.

For the KE17Z512 series, each TSI module adds the shield multiplexing feature to realize any one or ones of touch channels can be configured as shield channel through the `TSIx_SHIELD` register, provides four enhanced shield channel: CH4, CH12, CH21, CH24. The shield drive strength is improved to 960 pF at 1 MHz enhance the liquid tolerance performance when 24 shield channels are enabled.

For the KE17Z256 series, each TSI module has three shield channels on CH4, CH12, and CH21. These shield channels can be enabled and selected by configuring `TSIx_MOD[S_W_SHIELD]`. Shield channels can work as touch channels when turned off.

Shield electrode is only used in self-cap mode. Due to the different internal structures of self-cap and mutualcap, mutual-cap mode can be implemented without using a shield channel.

Shield electrode is only used in self-cap mode. Due to the different internal structures of self-cap and mutual-cap, mutual-cap mode can be implemented without using a shield channel.

4.1 Principle of self-cap mode to improve liquid tolerance by enabling shield channels

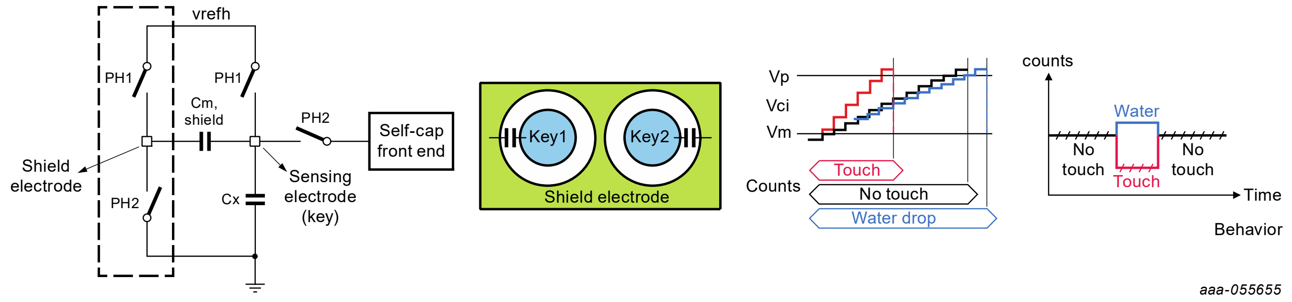

Figure 22. Self-cap touch key with water shield function

If the shelf channel is enabled, a parasitic mutual capacitance (C_m) is created between shield electrode and self-cap sensing electrode. When PH1 is turned on, C_x is charged and C_m is cleared. When PH2 is turned on, C_x charges C_m and C_i.

- When the hand touches self-cap electrode, C_x becomes larger and C_m decreases. When PH2 is on, the current charging C_i becomes larger and the number of charging times decreases, so the count number decreases.
- When there is interference such as water drop on the self-cap, C_m becomes larger. When PH2 is turned on, C_m shares some charge in C_x during transfer, the current charging C_i becomes smaller, and the number of charging times increases, so counter number increases.

Water drop induces TSI count increasing. It is an opposite trend, compared with normal touch – count decreasing.

4.2 Advantages of three shield channels of KE17Z of each TSI

3-shield channels can enhance the liquid tolerance and improve the driving ability of shield channel.

Based on X-KE17Z-TSI board, add Load capacitor 47 pF to shield channel. Perform a set of tests: Blue line is the Spring key in self-cap mode, yellow line is shield channel, and clock frequency is 1.04 MHz.

According to the test results, when the load increases and the three shield channels are opened, the waveform of the shield channel can still follow the waveform of the self-cap channel.

Figure 23. Driving capability comparison of shield channels

4.3 Principle of mutual-cap mode to improve liquid tolerance

Mutual-cap mode does not need the shield electrode.

When there is a water drop between RX and TX, a parasitic cap is made between drive electrode and receiving electrode. C_m is increased. It enlarges the collected charge and reduces the count number.

While the panel is touched, there is less coupling between drive electrode and receive electrode. C_m is decreased, $C_x = C_p + C_f$ is increased. The count number increases. Therefore, water drops do not send out a mis-trigger in mutual-cap mode.

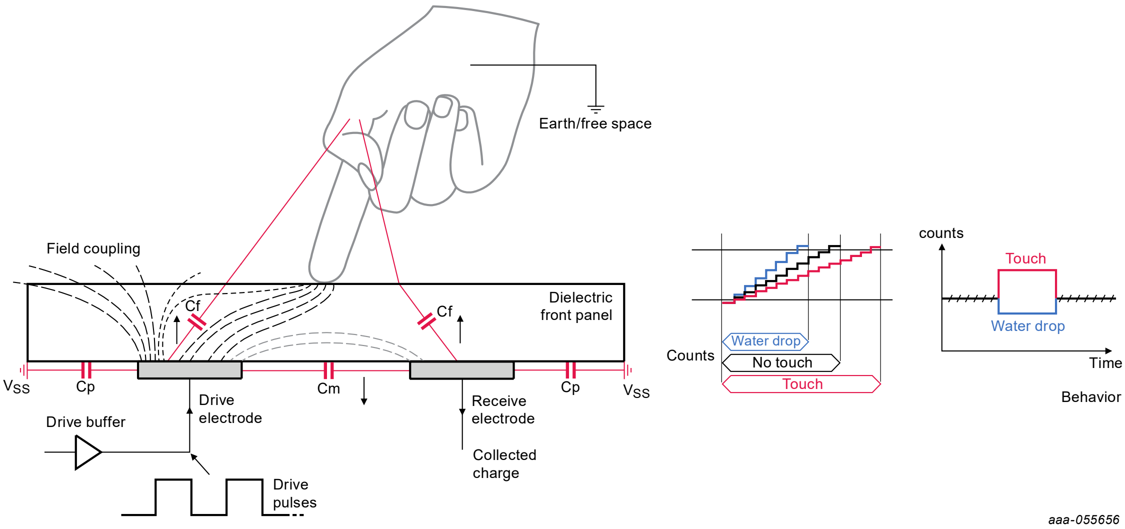

Figure 24. Mutual-cap mode count values of touch, no touch, and water drop

5 Hardware design guide

5.1 Electrode design

5.1.1 Electrode design for self-cap mode

Usually the electrode size is around 5 - 15 mm. A larger size of the electrode is appropriate for thicker overlays. To maximize the area of the electrodes from the capacitor plates, it is recommended that the size of the electrode be similar to a human finger (10 × 10 mm is considered a good size). To prevent charges from accumulating at the tips, try to avoid sharp corners when designing touch electrodes.

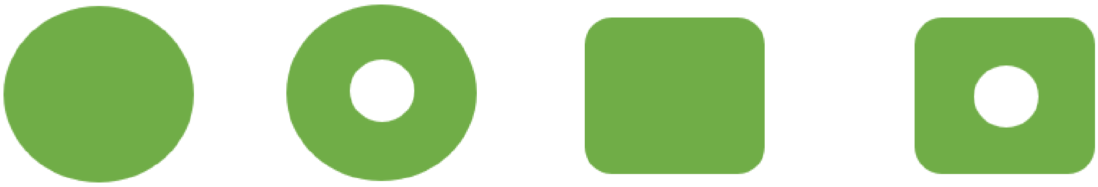

Figure 25. Electrode shapes for self-mode

5.1.2 Electrode design for mutual-cap mode

Mutual key is used to connect the TX and RX channels of TSI. It detects whether the key is pressed by sensing the change of mutual inductance capacitance between RX and TX. When designing the pattern of the mutual key, note that when the finger touches the key, the electric field between RX and TX can be affected to the greatest extent.

Figure 26 is the recommended mutual key shape. The electrode of TX wraps the electrode of RX, which can prevent RX from being affected by noise. The number of finger has much impact on the touch sensitivity. In general, more fingers result in stronger noise immunity but less touch sensitivity. Customer must select the right finger numbers for the thickness of touch overlay. For example, if the touch overlay is 3 mm in thickness, four fingers are the best choice. If the touch overlay is 2 mm in thickness, five fingers are OK.

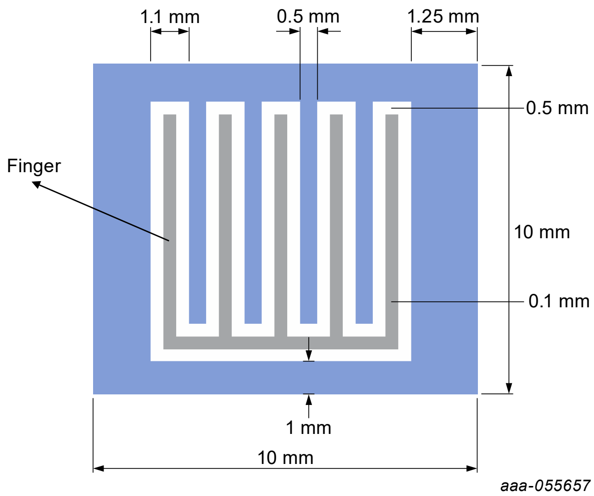

Figure 26. Electrode shapes for mutual mode

5.2 PCB trace routing

The following are recommendations for correctly routing the traces of capacitive electrodes.

- Width — Keep traces width as thin as possible. 5 - 7 mil trace is recommended. A 5-mil trace has half the capacitive coupling with the planes compared to a 10 mil trace.
- Length — As short as possible. Trace length must be less than 300 mm. To optimize signal strength, minimize trace length from TSI pins to touch pads.
- Clearance — To ensure signal integrity, leave a minimum clearance of 10 mils for the lines that run parallel to each other in the same layer, and route perpendicularly the ones running in adjacent layers. Good design practice is to keep traces separated by as much as the design allows. At the end of the sensor, where typically

the pitch is lower than 10 mils, a bottleneck mode connection is recommended as shown in Figure 27. Figure 27 is an example for maintaining adequate clearance in touch sensing traces.

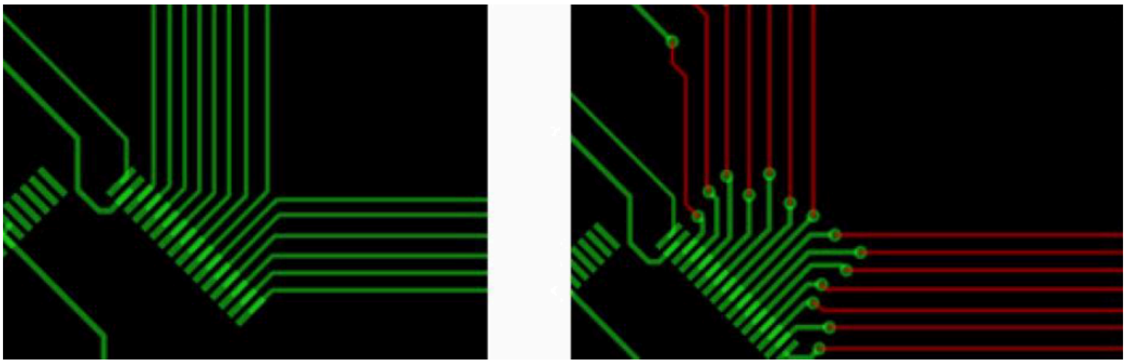

Figure 27. PCB trace routing

- Avoid routing under touch electrode: Do not route traces directly under any touch pad. Avoid electrical noise to be capacitive coupled to the electrodes.
- There must be no components near the touch electrodes.
- Better to routing under the bottom layer of PCB, to avoid impact of fingers.
- Avoid crossover with other signals.
- For the mutual mode key, keep the TX trace as far as possible from the RX trace.

5.3 Ground plane

A proper ground plane prevents the coupling of external electromagnetic interference to the touch sensing electrodes. It also acts as a shield for undesired electric fields. X-hatch pattern ground is recommended instead of solid filled ground to use around and under touch electrodes. This pattern can decrease the parasitic capacitance and increase the sensitivity of the touch sensor. When there is enough space between electrodes, it is recommended to use X-hatch pattern between the electrodes. This provides additional noise shielding and reference.

Following are a few recommendations and best practices for ground planes usage.

- Use X-hatch pattern on the top layer, 25 % ground fill, 7 mil line, 45 mil spacing.
- Use X-hatch pattern on the bottom layer (for example, underneath the electrodes area), 17 % ground fill, 7 mil line, 70 mil spacing.

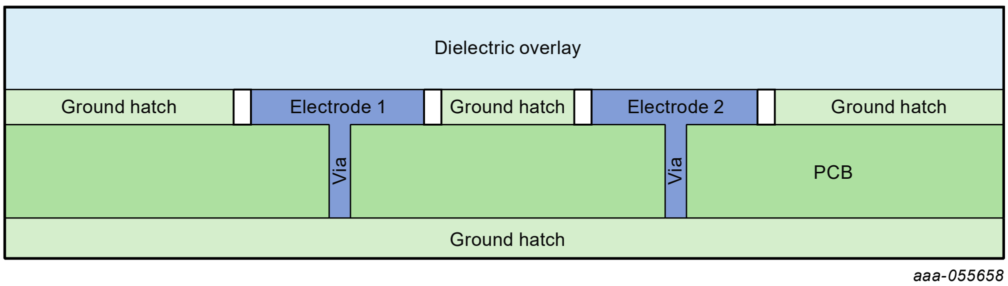

Figure 28. Ground plane on top and bottom plane

Annular gap size must be equal to the overlay thickness, but not smaller than 0.5 mm or larger than 2 mm. For example, a PCB layout for a system with a 1-mm overlay contains a 1 mm annular gap, while a 3-mm overlay design contains a 2-mm annular gap.

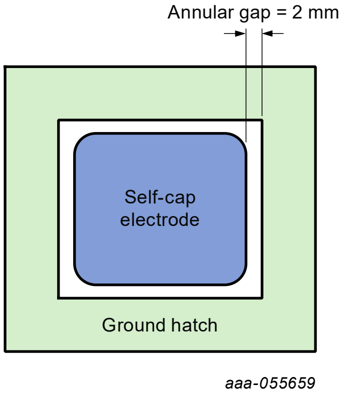

Figure 29. Annual gap size of the touch electrode

5.4 Overlay of the touch electrode

To protect the touch electrode from the interference of the external environment, overlay material must be closely attached to the surface of the touch electrode. There must not be air gap between the touch electrode and the overlay. Using an overlay with a high dielectric constant or an overlay with a small thickness can improve the sensitivity of the touch electrode.

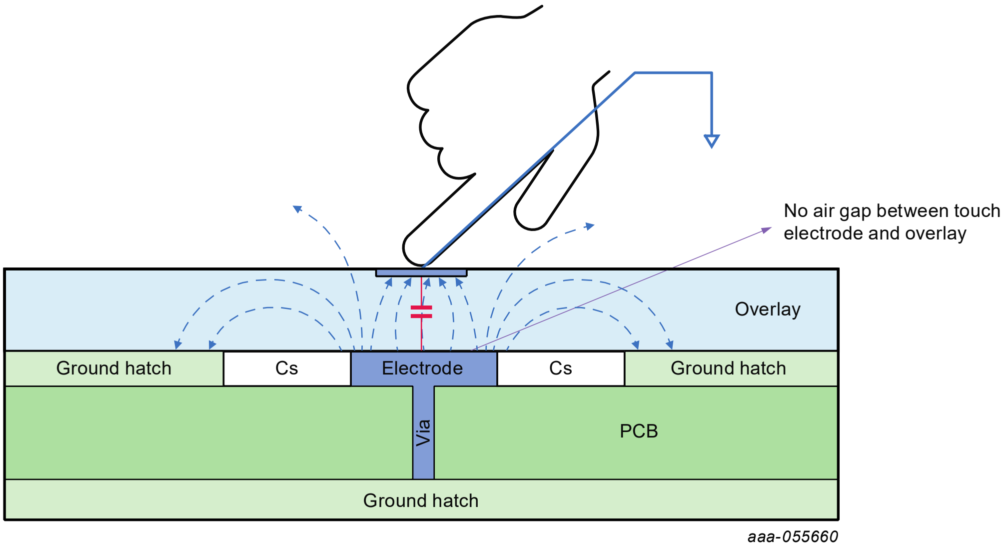

Figure 30. Parallel plate capacitor

Touch sensing capacitance can be calculated by Equation 15:

$$\Delta\, Cs = k * \varepsilon 0 * \frac{A}{d} \tag{15}$$

- $\Delta\, Cs$ is the touch sensing capacitance in farads (F).
- A is the touch area between finger and overlay
- d is the distance between finger and electrode in meter (m)
- k is the dielectric constant of the overlay material
- $\varepsilon 0$ is the permittivity of the free space (8.85 × 1012 F/m)

Overlay can use different material, the dielectric constants of common material are as follows:

Table 17. Dielectric constants of common material

Material	Dielectric constant (k)
Acrylic (PMMA)	2.7 - 4.5
Air	1.0
Tempered Glass	7.2 - 8.0
Polyester (PET)	2.8 - 4.5

Air has the lowest dielectric constant, and other commonly used overlay materials have relatively high dielectric constants. According to Equation 15, selecting an overlay with a high dielectric constant enhances the sensitivity of the touch electrode. Thicker overlay decreases the touch electrode resolution.

Note: *When using overlays with higher dielectric constants, remove any gap between touch electrode and overlay material.*

5.5 Electrodes placement

The following are recommendations for placing the touch sensing electrodes on a PCB or FlexPCB.

- All touch electrodes must be placed as close to the MCU as possible. As the long trace loops in layout cause extra intrinsic capacitance and easily coupled noise, placing touch electrodes closer to the chip is always better.
- Components underneath electrodes — It is not recommended to place any component underneath the area of touch sensing electrode, especially in two-layer boards.
- Keep electrodes far away power module, RF antenna, and so on.

5.6 Hardware checklist

The following is a checklist based on the recommendations in this application note. Before having a board, film, ITO, and the touch sensing board made, make sure that the design follows all or most of these rules:

- GND return path is provided per specifications (GND hatch below or at least around the electrode keypad).
- No pull-ups present in TSI-enabled (touch sensing input module) pins.
- Series resistors in cases where series current protection is desired must lower than 100 Ω.
- Make sure that no signals are not touch sensing run parallel to the touch sensing signals. If signals must go through the touch sensing traces, let them go in a different layer and perpendicular.
- Make sure to fill in ground between groups of traces (analog, digital, and touch). If possible, fill in ground between touch sensing traces.
- Traces as thin as the PCB or film technology allows.
- Short traces (< 300 mm. from electrode to MCU, ideally < 50 mm.)
- Electrode shape corners as rounded as the layout allows.

5.7 X-KE17Z-TSI-EVB touch electrode patterns design

The X-KE17Z-TSI-EVB is a two-layer reference board that enables dual TSI evaluation. It offers comprehensive touch patterns, including mutual-cap touchpads, self-cap touchpads, self-cap spring touch keys, shield electrode, touch slide, two-dimensional (2D) touchpad, and proximity loop (outside 2D touchpad and 3 × 5 self-cap touchpad). The following is the introduction of several electrode patterns.

5.7.1 2D touchpad

2D touchpad input interface that must be able to detect touch and release conditions and vertical and horizontal sliding in a specific area. As shown in Figure 31, 2D touchpad is implemented in an X–Y or row–column fashion.

To accomplish the interleaving of the rows and the columns for a fingertip, two layers of conductive materials are needed.

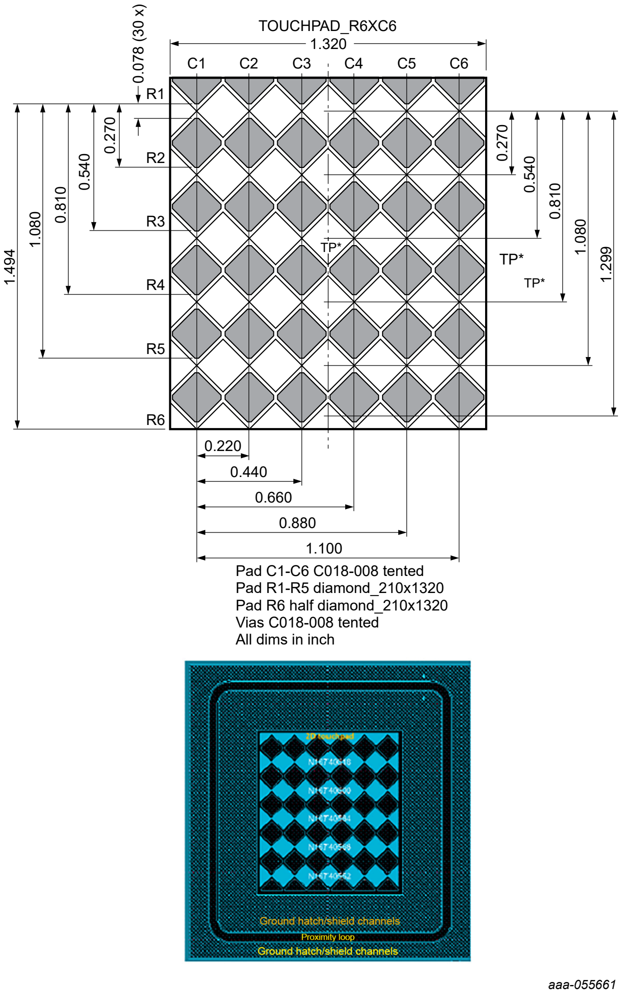

Figure 31. 2D touchpad

The decoding for this type of interfaces is the combination of two sliders. The horizontal one created by sliding a finger through the different columns, and the vertical slider created when a finger slides through the rows. In the same manner, a touch and release condition in a certain region of the touchpad is detected by the combination of one row and one column touched at a time.

Resolution can be increased by reducing the size of the diamonds. However, depending on thickness and dielectric constant of the overlay on top of the touchpad, the electrodes sensitivity is too minimal to detect acceptable touches above the signal-to-noise ratio.

5.7.2 Keyboard touchpads

3 × 5 self-cap touchpad and 6 × 6 mutual-cap touchpad are already on the X-KE17Z-TSI-EVB. The keyboard touchpads are designed to evaluate the keys in self-cap mode/mutual-cap mode, the application of slider, and other applications, such as, e-lock and touch keyboard.

For 3 × 5 self-cap touchpad, each electrode is connected to a TSI touch channel. Each electrode is independent of each other, reducing interference between electrodes.

The hatched area around the 3 × 5 self-cap touchpad is the common area of shield electrodes and GND. The function of hatched area is switched through a 0 Ω resistors.

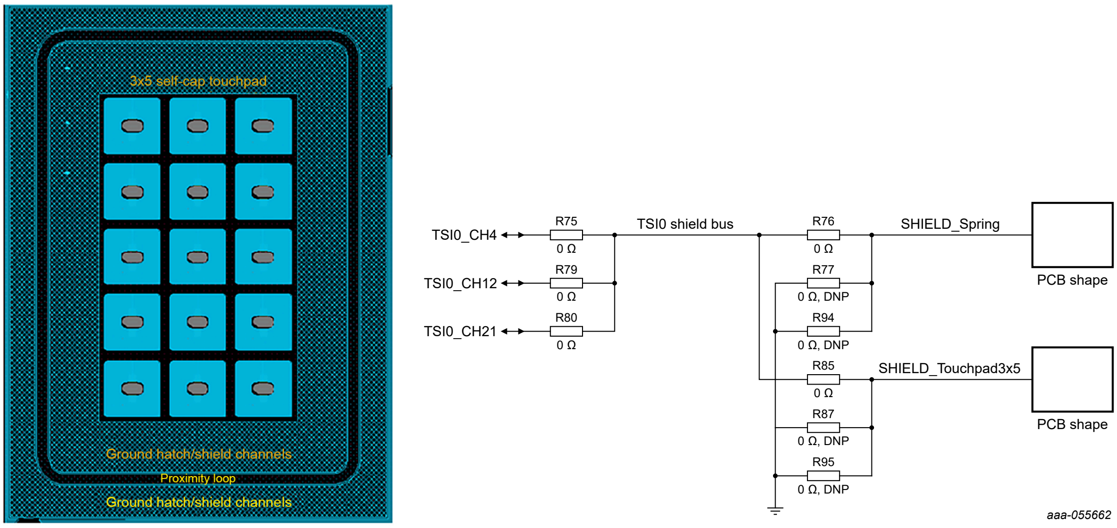

Figure 32. 3 × 5 self-cap touchpad

For the 6 × 6 mutual-cap touchpad, it only cost 12 touch channels to get the 36 electrodes. Using the mutual-cap key to design the touchpad can save touch channels and get more touch electrodes. But there is a little more interference between the electrodes. When any button is touched, the electrodes in both vertical and horizontal directions produce capacitance changes.

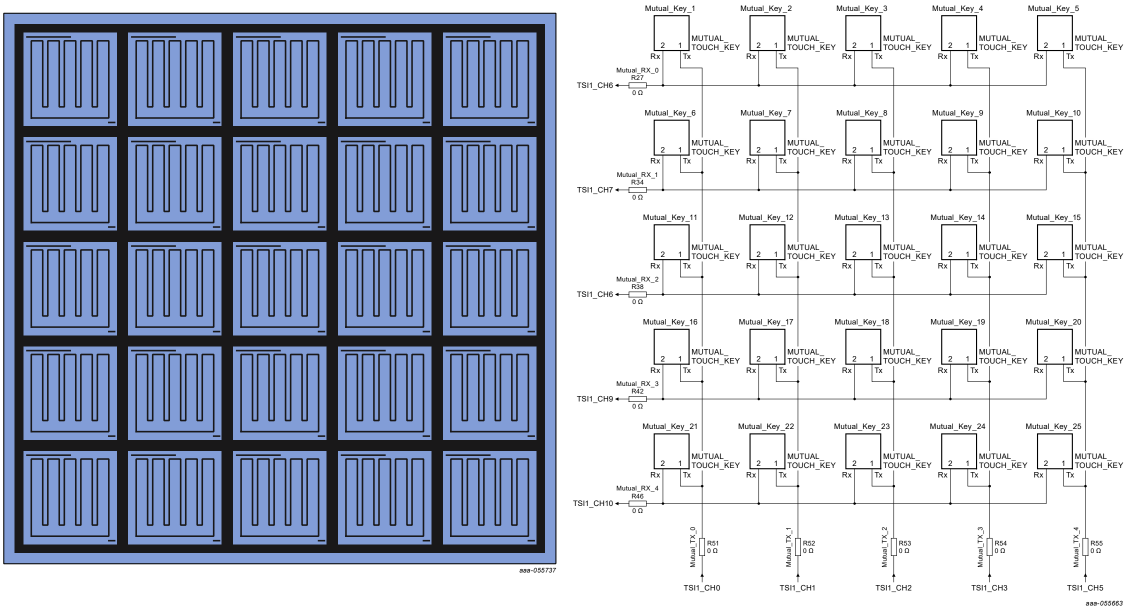

Figure 33. 6 × 6 mutual-cap touchpad, realized by 12 TSI touch channel

5.7.3 Spring keys

Spring key connects touch channel and overlay through spring. The spring key keeps the PCB far away from overlay to get the enhanced liquid tolerance. When there is water drop on the spring key, the parasitic capacitance, C_S, between the liquid and the ground is relatively small. No mis-trigger happens.

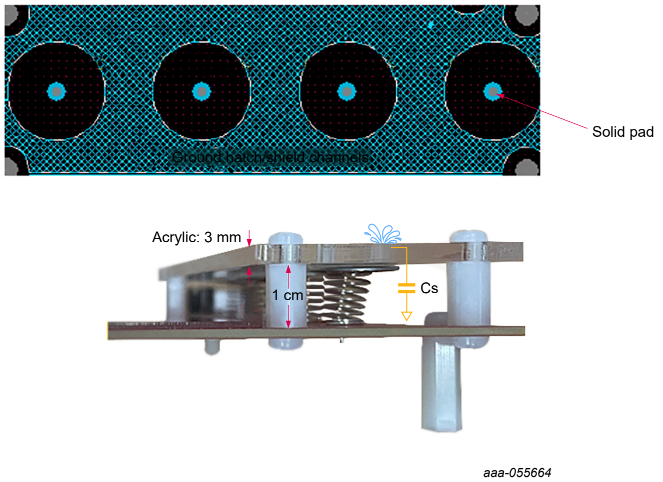

Figure 34. Spring keys

6 References

Following references are available on NXP website.

- *Designing Touch Sensing Electrodes* (document AN3863)
- *Kinetis KE17Z/13Z/12Z with up to 256 kB Flash Reference Manual* (document KE1xZP100M72SF1RM)
- *NXP Touch Development Guide* (document AN12709)

7 Revision history

Table 18 summarizes the revisions to this document.

Table 18. Revision history

Document ID	Release date	Description
KE17ZDTSIUG v.2	07 May 2024	• Updated some images to svg format • Added Section 1.1 "TSI model support of KE1xZ family" • Updated Section 1.2 "KE17Z dual TSI" • Added Section 1.3 "KE1xZ part numbers supporting TSI model"
KE17ZDTSIUG v.1	10 January 2023	• Updated Figure 2 • Updated Figure 2
KE17ZDTSIUG v.0	05 May 2022	Initial public release

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