

SPF5020CVNAQES – NXP Standard

Configuration report for PF5020-QM OTP program ID: AQ rev A

Rev. 1.2 - 10/17/2022

Report

1 General description

The PF5020 is a power management integrated circuit (PMIC) featuring multiple high efficiency buck regulators designed to operate as a stand alone regulator or as a companion chip to a larger PMIC.

Built-in one time programmable memory stores key startup configurations, drastically reducing external components typically used to set output voltage and sequence of external regulators. Regulator parameters are adjustable through high-speed I2C after start up offering flexibility for different system states.

Note: Electrical characteristics are maintained in the PF5020 data sheet.

2 Features and benefits

- Up to three high efficiency buck converters
- One linear regulators with load switch options
- RTC supply and coin cell charger
- Watchdog timer/monitor
- Independent Voltage Monitoring circuit
- One time programmable device configuration
- 3.4 MHz I2C communication interface
- 40-pin QFN package with wettable flank and exposed pad

3 Applications

- Automotive Infotainment
- High - End Industrial

4 Ordering information

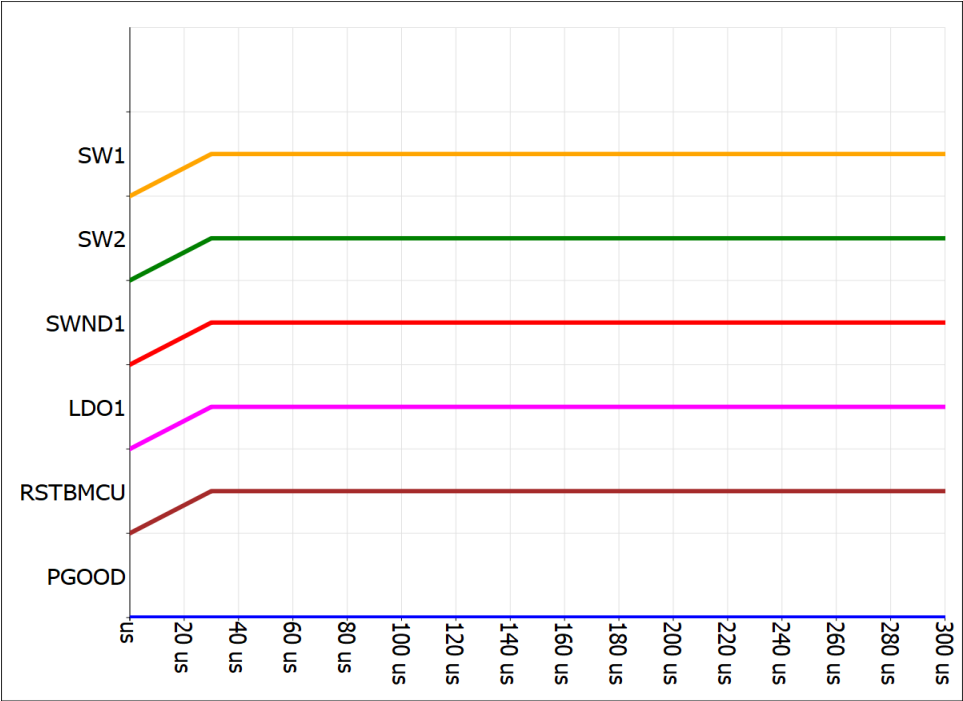
Table 1. Ordering information

Type number ^[1]	Package		
	Name	Description	Version
SPF5020CVNAQES	HVQFN40	HVQFN40, plastic, thermally enhanced very thin quad flat pack; non-leaded wettable flank, 40 terminals; 0.5 mm pitch; 6 mm x 6 mm x 0.9 mm body	SOT618-17(D)

[1] To order parts in tape and reel, add the R2 suffix to the part number.

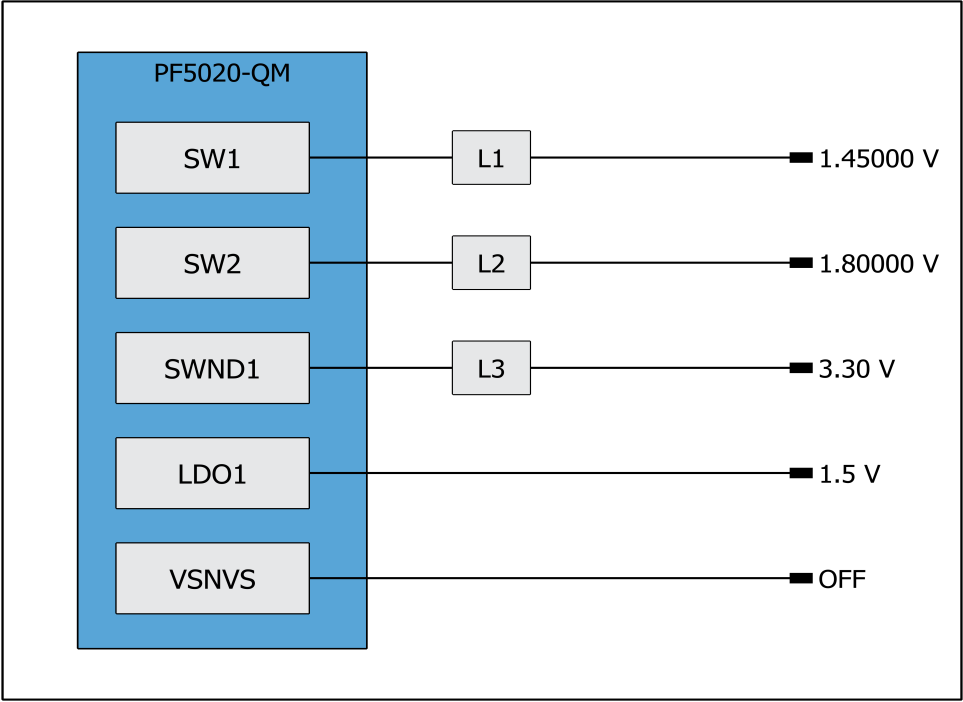


5 Power-up sequence summary



The signals depicted above are enable signals for each regulator. They don't represent the actual ramp voltage.

6 Hardware configuration diagram



7 OTP configuration

See PF5020 datasheet for parametric details. The OTP configuration summary for AQ sequence ID is provided in Tables below.

Table 2. Device OTP configuration

Functional block	Feature	OTP selection
I2C Settings	I2C Address	0x08
	I2C CRC	Disabled
VIN OV lockout	VIN_OVLO Mode	Disabled
	VIN_OVLO Shutdown	Interrupt Only
	VIN_OVLO Debounce	10 us
Power good	PG Check On Power Up	PG not checked at power up
	PG Active Mode	PGOOD Mode
PWRON control	Power On Event Detection	Level sensitive mode
	PWRON Debounce	32 ms
	TRESET Time	2 s
	TRESET Behavior	PMIC shuts down after push button pressed
STANDBY control	STANDBY Polarity	Active High
EWARN timer	EWARN Delay	100 us
XFAIL pin	XFAIL Operation	Disabled
WDI control	WDI Reset Type	Soft WD Reset
	WDI Polarity	Falling edge of WDI
	WDI Detection In Standby	Disabled in STBY
WD Timer control	WD Timer	WD Timer Disabled
	WD Clear Window	Cleared within 100 %
	WD Window Duration	1 ms

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	WD Expire Number	Event on step 1
	Maximum WD Event Counter	1 Event
	WD Detection In Standby	Disabled in STBY
Frequency control	Nominal Switching Frequency	2.500 MHz
	Switching Mode	PWM
	FSYNC Mode	SYNCOUT
	SYNCIN Range	2000 KHz to 3000 KHz
	SYNCOUT Operation	Disabled
	Frequency Spread Spectrum	Disabled
	FSS Range	+/-5 %

Table 3. OTP fault management configuration

Functional block	Feature	OTP selection
Fault management	Fault Timer	1 ms
	Maximum Fault Counter	Disabled

Table 4. Sequencer OTP configuration

Functional block	Feature	OTP selection
Power up sequencing	Sequence TBASE	30 us
	RESETBMCU Sequence Slot	Slot 0
	PGOOD Sequence Slot	OFF
	SW1 Sequence Slot	Slot 0
	SW2 Sequence Slot	Slot 0
	SWND1 Sequence Slot	Slot 0
	LDO1 Sequence Slot	Slot 0
Power down sequencing	Power Down Mode	Mirror power down
	RESETBMCU Power Down	Group 4

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	PGOOD Power Down Group	Group 4
	SW1 Power Down Group	Group 4
	SW2 Power Down Group	Group 4
	SWND1 Power Down Group	Group 4
	LDO1 Power Down Group	Group 4
	RESETBMCU Group Delay	No delay
	Group 1 Power Down Delay	120 us
	Group 2 Power Down Delay	120 us
	Group 3 Power Down Delay	120 us
	Group 4 Power Down Delay	120 us
	Power Down Delay	No delay
	VTT Power Down	High impedance

Table 5. Regulator OTP configuration

Functional block	Feature	OTP selection
SW1	Output Voltage	1.45000 V
	Current Limit	2.6 A
	OV Detection Threshold	105 %
	UV Detection Threshold	95 %
	DVS Ramp	7.81 mV/us
	Switching Phase	45°
	Output Inductor	1 uH (Default)
	PGOOD Mode	Enabled
	SW1 WD Bypass	Reset on WDI
	SW1 OV Bypass	OV protection enabled

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	SW1 UV Bypass	UV protection enabled
	SW1 ILIM Bypass	ILIM protection enabled
	SW1 Transconductance	65 umho
	SW1 Multi-phase Selector	SW1 and SW2 single phase
SW2	Output Voltage	1.80000 V
	Current Limit	2.6 A
	OV Detection Threshold	105 %
	UV Detection Threshold	95 %
	DVS Ramp	7.81 mV/us
	Switching Phase	45°
	Output Inductor	1 uH (Default)
	VTT Mode	Disabled
	PGOOD Mode	Enabled
	SW2 WD Bypass	Reset on WDI
	SW2 OV Bypass	OV protection enabled
	SW2 UV Bypass	UV protection enabled
	SW2 ILIM Bypass	ILIM protection enabled
	SW2 Transconductance	65 umho
SWND1	Output Voltage	3.30 V
	Current Limit	2.6 A
	OV Detection Threshold	105 %
	UV Detection Threshold	95 %
	Switching Phase	45°
	Output Inductor	1 uH (Default)

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	PGOOD Mode	Enabled
	SWND1 WD Bypass	Reset on WDI
	SWND1 OV Bypass	OV protection enabled
	SWND1 UV Bypass	UV protection enabled
	SWND1 ILIM Bypass	ILIM protection enabled
	SWND1 Transconductance	65 umho
	SWND1 Resistance	56 KOhm
LDO1	Output Voltage	1.5 V
	OV Detection Threshold	105 %
	UV Detection Threshold	95 %
	Operating Mode	Normal Mode
	PGOOD Mode	Enabled
	LDO1 WD Bypass	Bypass WDI
	LDO1 OV Bypass	OV protection enabled
	LDO1 UV Bypass	UV protection enabled
	LDO1 ILIM Bypass	ILIM protection enabled
VSNVS	Output Voltage	OFF
PROGRAM ID	Program ID High	A
	Program ID Low	Q

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