

SPF5020CMBAKES – NXP Standard

Configuration report for PF5020-B OTP program ID: AK rev A

Rev. 1.0 - 7/19/2022

Report

1 General description

The PF5020 is a power management integrated circuit (PMIC) featuring multiple high efficiency buck regulators designed to operate as a stand alone regulator or as a companion chip to a larger PMIC.

Built-in one time programmable memory stores key startup configurations, drastically reducing external components typically used to set output voltage and sequence of external regulators. Regulator parameters are adjustable through high-speed I2C after start up offering flexibility for different system states.

Note: Electrical characteristics are maintained in the PF5020 data sheet.

2 Features and benefits

- Up to three high efficiency buck converters
- One linear regulators with load switch options
- RTC supply and coin cell charger
- Watchdog timer/monitor
- Independent Voltage Monitoring circuit
- One time programmable device configuration
- 3.4 MHz I2C communication interface
- Integrated Functional Safety to fit ASIL B systems

3 Applications

- Automotive Infotainment
- High - End Industrial

4 Ordering information

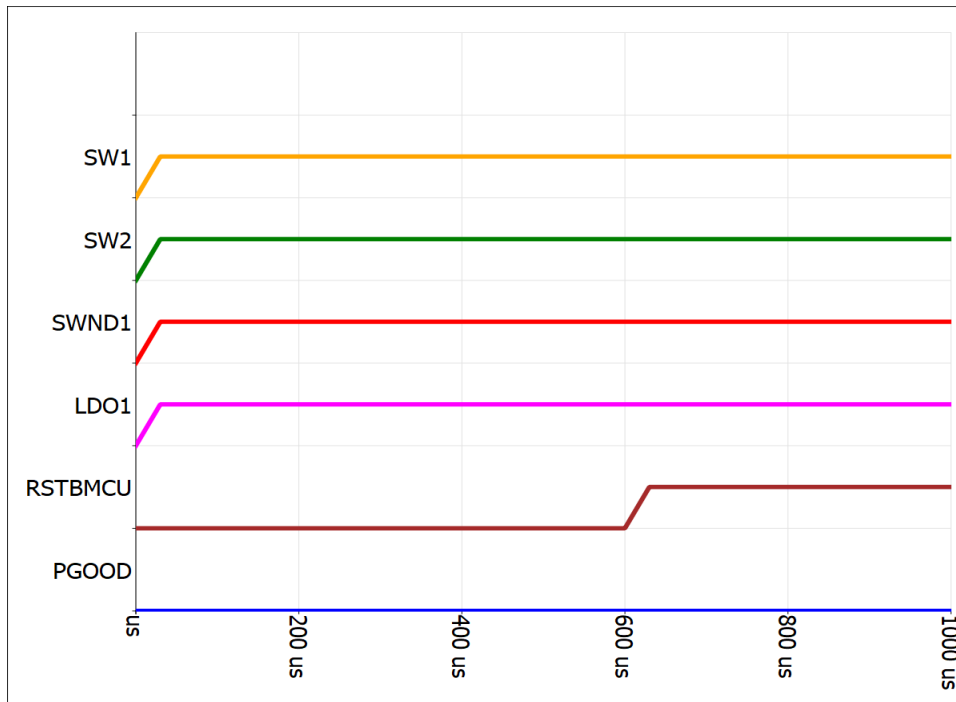
Table 1. Ordering information

| Type number ^[1] | Package | | |
|----------------------------|---------|---|--------------|
| | Name | Description | Version |
| SPF5020CMBAKES | HVQFN40 | HVQFN40, plastic, thermally enhanced very thin quad flat pack; non-leaded wettable flank, 40 terminals; 0.5 mm pitch; 6 mm x 6 mm x 0.9 mm body | SOT618-17(D) |

[1] To order parts in tape and reel, add the R2 suffix to the part number.

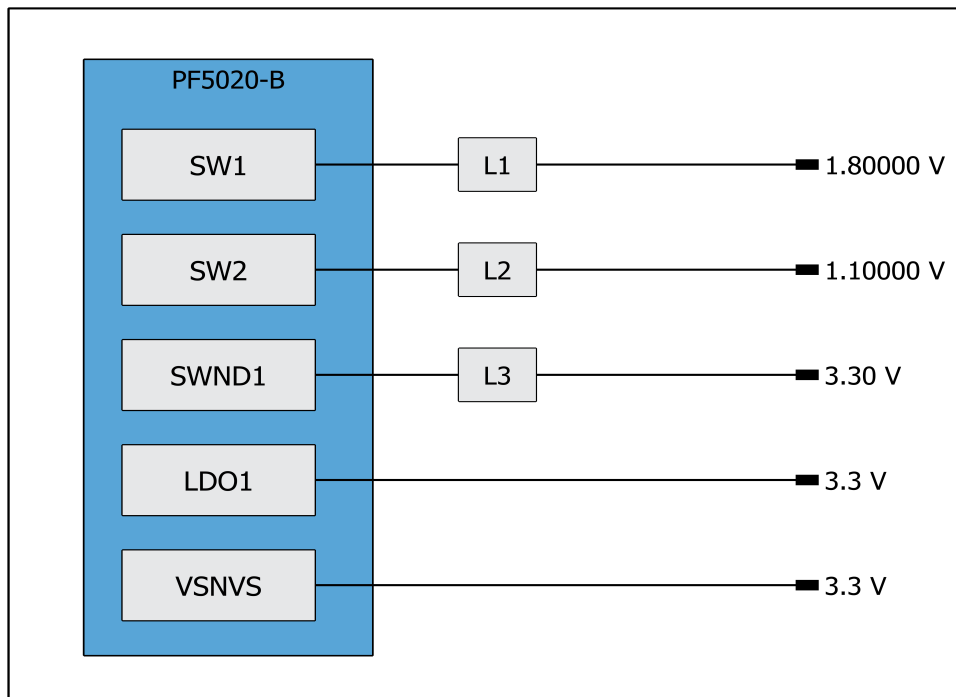


5 Power-up sequence summary



The signals depicted above are enable signals for each regulator. They don't represent the actual ramp voltage.

6 Hardware configuration diagram



7 OTP configuration

See PF5020 datasheet for parametric details. The OTP configuration summary for AK sequence ID is provided in Tables below.

Table 2. Device OTP configuration

| Functional block | Feature | OTP selection |
|------------------|--------------------------|---|
| I2C Settings | I2C Address | 0x09 |
| | I2C CRC | Enabled |
| VIN OV lockout | VIN_OVLO Mode | Enabled |
| | VIN_OVLO Shutdown | Interrupt Only |
| | VIN_OVLO Debounce | 10 us |
| Power good | PG Check On Power Up | PG not checked at power up |
| | PG Active Mode | PGOOD Mode |
| PWRON control | Power On Event Detection | Level sensitive mode |
| | PWRON Debounce | 32 ms |
| | TRESET Time | 2 s |
| | TRESET Behavior | PMIC shuts down after push button pressed |
| STANDBY control | STANDBY Polarity | Active High |
| EWARN timer | EWARN Delay | 100 us |
| XFAIL pin | XFAIL Operation | Enabled |
| WDI control | WDI Reset Type | Soft WD Reset |
| | WDI Polarity | Falling edge of WDI |
| | WDI Detection In Standby | Disabled in STBY |
| WD Timer control | WD Timer | WD Timer Disabled |
| | WD Clear Window | Cleared within 100 % |
| | WD Window Duration | 1 ms |

Configuration report for PF5020-B OTP program ID: AK rev A

| | | |
|-------------------|-----------------------------|----------------------|
| | WD Expire Number | Event on step 1 |
| | Maximum WD Event Counter | 1 Event |
| | WD Detection In Standby | Disabled in STBY |
| Frequency control | Nominal Switching Frequency | 2.500 MHz |
| | Switching Mode | PWM |
| | FSYNC Mode | SYNCOUT |
| | SYNCIN Range | 2000 KHz to 3000 KHz |
| | SYNCOUT Operation | Disabled |
| | Frequency Spread Spectrum | Disabled |
| | FSS Range | +/-5 % |

Table 3. OTP fault management configuration

| Functional block | Feature | OTP selection |
|------------------|-----------------------|---------------|
| Fault management | Fault Timer | 1 ms |
| | Maximum Fault Counter | Disabled |

Table 4. Sequencer OTP configuration

| Functional block | Feature | OTP selection |
|-----------------------|-------------------------|-------------------|
| Power up sequencing | Sequence TBASE | 30 us |
| | RESETBMCU Sequence Slot | Slot 20 |
| | PGOOD Sequence Slot | OFF |
| | SW1 Sequence Slot | Slot 0 |
| | SW2 Sequence Slot | Slot 0 |
| | SWND1 Sequence Slot | Slot 0 |
| | LDO1 Sequence Slot | Slot 0 |
| Power down sequencing | Power Down Mode | Mirror power down |
| | RESETBMCU Power Down | Group 4 |

Configuration report for PF5020-B OTP program ID: AK rev A

| | | |
|--|--------------------------|----------------|
| | PGOOD Power Down Group | Group 4 |
| | SW1 Power Down Group | Group 4 |
| | SW2 Power Down Group | Group 4 |
| | SWND1 Power Down Group | Group 4 |
| | LDO1 Power Down Group | Group 4 |
| | RESETBMCU Group Delay | No delay |
| | Group 1 Power Down Delay | 120 us |
| | Group 2 Power Down Delay | 120 us |
| | Group 3 Power Down Delay | 120 us |
| | Group 4 Power Down Delay | 120 us |
| | Power Down Delay | No delay |
| | VTT Power Down | High impedance |

Table 5. Regulator OTP configuration

| Functional block | Feature | OTP selection |
|------------------|------------------------|-----------------------|
| SW1 | Output Voltage | 1.80000 V |
| | Current Limit | 2.6 A |
| | OV Detection Threshold | 105 % |
| | UV Detection Threshold | 95 % |
| | DVS Ramp | 7.81 mV/us |
| | Switching Phase | 45° |
| | Output Inductor | 1 uH (Default) |
| | PGOOD Mode | Enabled |
| | SW1 WD Bypass | Reset on WDI |
| | SW1 OV Bypass | OV protection enabled |

Configuration report for PF5020-B OTP program ID: AK rev A

| | | |
|-------|--------------------------|--------------------------|
| | SW1 UV Bypass | UV protection enabled |
| | SW1 ILIM Bypass | ILIM protection enabled |
| | SW1 Transconductance | 65 umho |
| | SW1 Multi-phase Selector | SW1 and SW2 single phase |
| SW2 | Output Voltage | 1.10000 V |
| | Current Limit | 2.6 A |
| | OV Detection Threshold | 105 % |
| | UV Detection Threshold | 95 % |
| | DVS Ramp | 7.81 mV/us |
| | Switching Phase | 45° |
| | Output Inductor | 1 uH (Default) |
| | VTT Mode | Disabled |
| | PGOOD Mode | Enabled |
| | SW2 WD Bypass | Reset on WDI |
| | SW2 OV Bypass | OV protection enabled |
| | SW2 UV Bypass | UV protection enabled |
| | SW2 ILIM Bypass | ILIM protection enabled |
| | SW2 Transconductance | 65 umho |
| SWND1 | Output Voltage | 3.30 V |
| | Current Limit | 2.1 A |
| | OV Detection Threshold | 105 % |
| | UV Detection Threshold | 95 % |
| | Switching Phase | 45° |
| | Output Inductor | 1 uH (Default) |

Configuration report for PF5020-B OTP program ID: AK rev A

| | | |
|--------------------------|------------------------|-------------------------|
| | PGOOD Mode | Enabled |
| | SWND1 WD Bypass | Reset on WDI |
| | SWND1 OV Bypass | OV protection enabled |
| | SWND1 UV Bypass | UV protection enabled |
| | SWND1 ILIM Bypass | ILIM protection enabled |
| | SWND1 Transconductance | 65 umho |
| | SWND1 Resistance | 56 KOhm |
| LDO1 | Output Voltage | 3.3 V |
| | OV Detection Threshold | 105 % |
| | UV Detection Threshold | 95 % |
| | Operating Mode | Normal Mode |
| | PGOOD Mode | Enabled |
| | LDO1 WD Bypass | Reset on WDI |
| | LDO1 OV Bypass | OV protection enabled |
| | LDO1 UV Bypass | UV protection enabled |
| | LDO1 ILIM Bypass | ILIM protection enabled |
| VSNVS | Output Voltage | 3.3 V |
| ASIL B functional safety | Fail Safe State | FS state Disabled |
| | Max FS Counter | 15 Events |
| | FS Self-clear Timer | 1 Minute |
| | Bandgap Comparator | Interrupt on BG fault |
| | I2C Secure Write | Enabled |
| PROGRAM ID | Program ID High | A |
| | Program ID Low | K |

8 Legal information

8.1 Definitions

Draft - The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Limited warranty and liability - Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes - NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use - NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications - Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem

which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values - Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale - NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license - Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Suitability for use in automotive applications - This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Export control - This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations - A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

8.2 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

NXP - is a trademark of NXP B.V.

Contents

| | |
|--|---|
| 1 General description | 1 |
| 2 Features and benefits | 1 |
| 3 Applications | 1 |
| 4 Ordering information | 1 |
| 5 Power up sequence summary | 2 |
| 6 Hardware configuration diagram | 2 |
| 7 OTP configuration | 3 |
| 8 Legal information | 8 |

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2022 .

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 7/19/2022

Document identifier: R_SPF5020CMBAKES