

1 General description

The PF8100 is a power management integrated circuit (PMIC) designed for high performance i.MX 8 and S32V based applications. It features seven high efficiency buck converters and four linear regulators for powering the processor, memory and miscellaneous peripherals. It meets the stringent requirements of automotive applications and is fully AEC-Q100 grade 2 qualified.

Built-in one time programmable memory stores key startup configurations, drastically reducing external components typically used to set output voltage and sequence of external regulators. Regulator parameters are adjustable through high-speed I2C after start up offering flexibility for different system states.

Note: Electrical characteristics are maintained in the PF8100_PF8200 data sheet

2 Features and benefits

- Up to seven high efficiency buck converters
- Four linear regulators with load switch options
- RTC supply and coin cell charger
- Watchdog monitoring
- Independent OV/UV monitoring circuits
- One time programmable device configuration
- 3.4 MHz I2C communication interface
- 56-pin 8 x 8 QFN package
- AEC-Q100 grade 2 qualified

3 Applications

- Automotive Infotainment
- High-end consumer and industrial



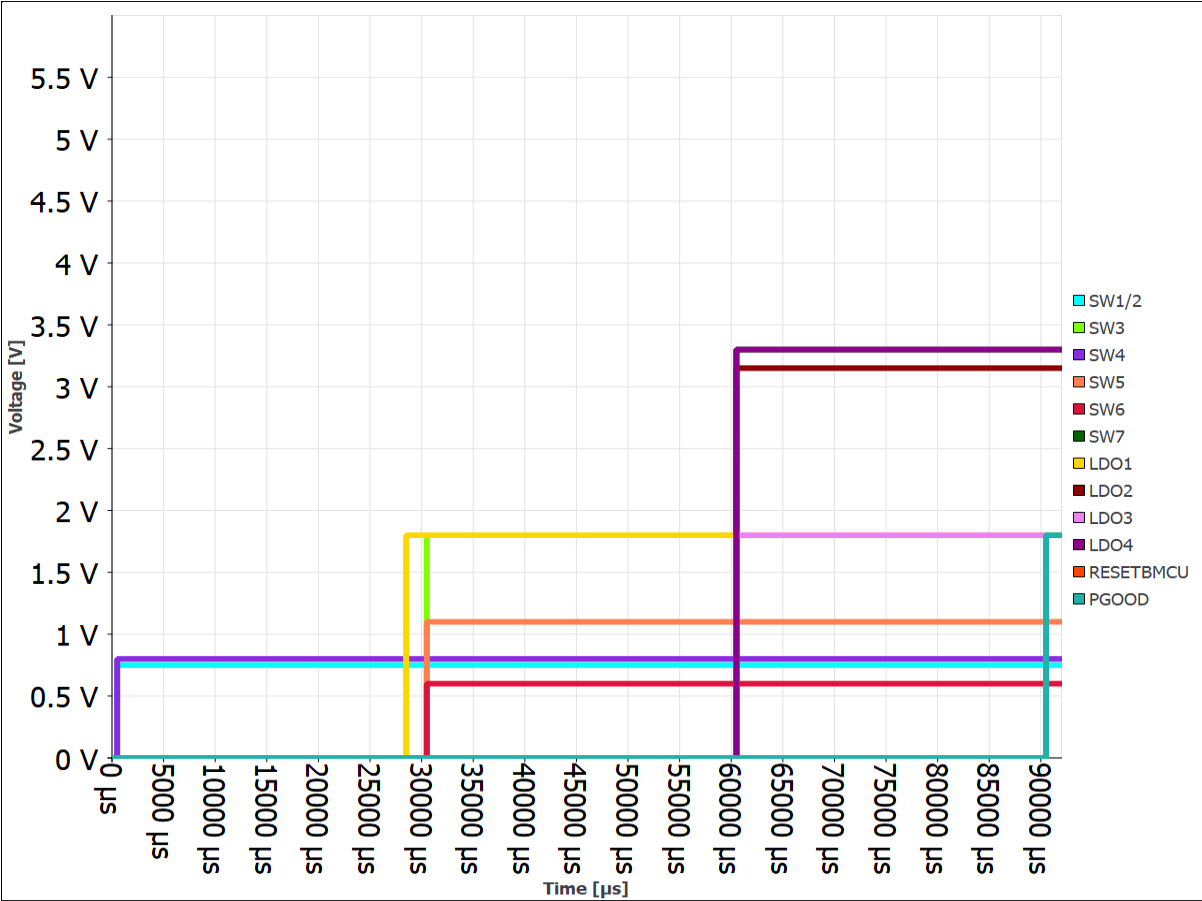
4 Ordering information

Table 1. Ordering information

Type number ^[1]	Package		
	Name	Description	Version
SC33PF8100G9EP	WF-Type HVQFN56	HVQFN56, plastic, thermally enhanced very thin quad; flat non-leaded package, wettable flanks; 56 terminals; 0.5 mm pitch; 8 mm x 8 mm x 0.85 mm body	SOT684-21 (DD/SC)

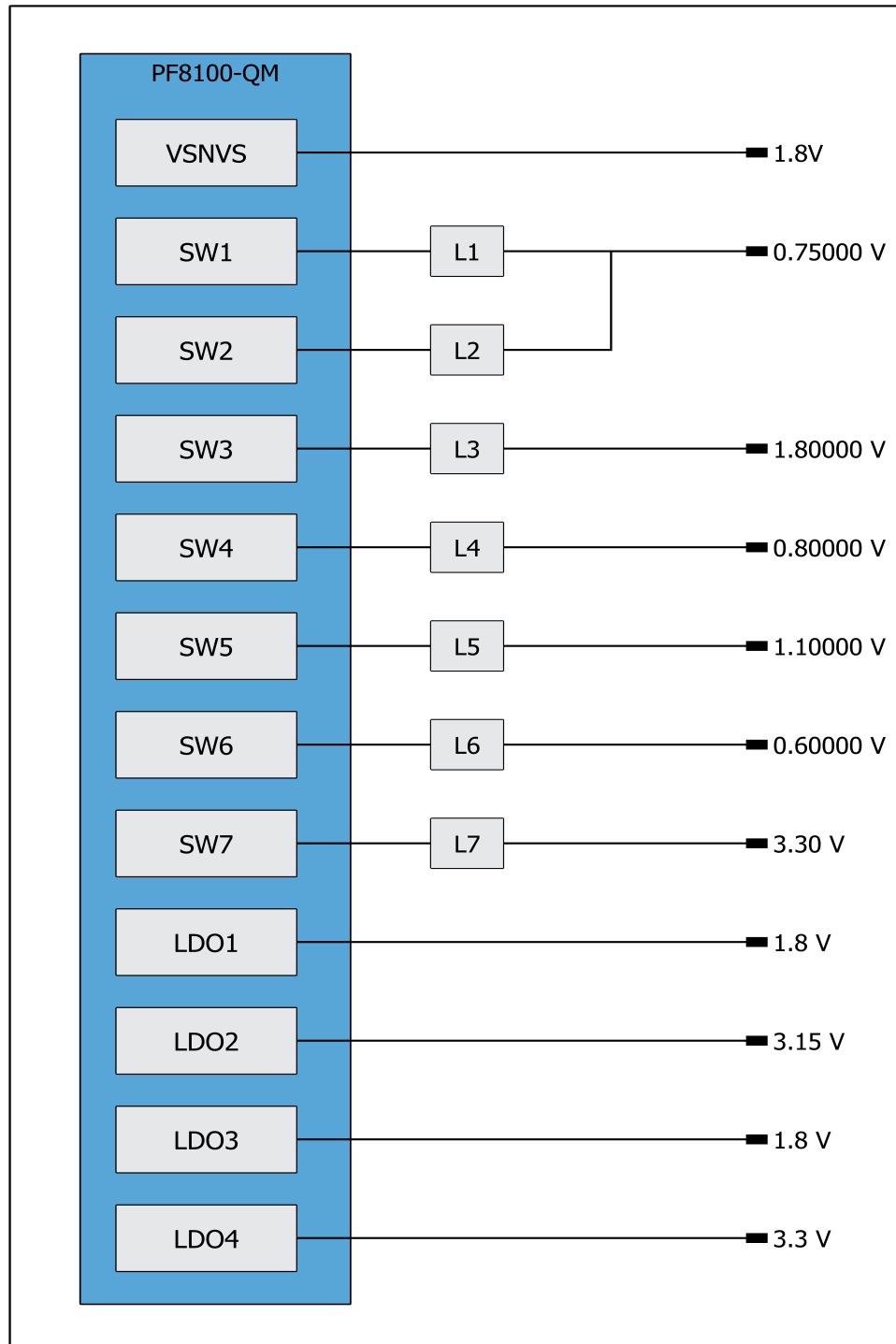
[1] To order parts in tape and reel, add the R2 suffix to the part number.

5 Power-up sequence summary



The signals depicted above are enable signals for each regulator. They don't represent the actual ramp voltage.

6 Hardware configuration diagram



7 OTP configuration

See PF8100_PF8200 data sheet for parametric details. The OTP configuration summary for G9 (sequence ID) is provided in Tables below.

Table 2. Device OTP configuration

Functional block	Feature	OTP selection
System configuration	I2C Address	0x08
	I2C CRC	Disabled
	VIN OVLO Monitor	VIN_OVLO Enabled
	VIN OVLO Debounce	100µs
	VIN OVLO Shutdown	VIN_OVLO Shutdown Disabled
	Maximum Fault Count	Disabled
	Fault Timer	DISABLED
Watchdog monitoring	WDI Mode	Hard WD Reset
	WDI Polarity	WD event detected on falling edge
	WDI In Standby	WDI event Disabled in Standby
	WD Counter	WD Timer Disabled
	WD Counter In Standby	WD Timer Disabled in Standby
	WD Clear Window	Clear within 100% of window
	Maximum Time Out Steps	7
	WD Duration	1024 ms
	Maximum WD Event	15
Clock management	Switching Frequency	2.5 MHz
	SYNCIN Range	2000KHz to 3000KHz
	SYNCIN Operation	Disabled
	SYNCOUT Operation	Disabled

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	Frequency Spread Spectrum	Frequency Spread Spectrum Disabled
	FSS Range	FSS Range set to 10%
COINCELL Control	Coin Cell Charging Voltage	3.0 V

Table 3. I/Os configuration

Functional block	Feature	OTP selection
I/O Configuration	PWRON Mode	Level Sensitive
	PWRON Debounce	32 msec
	PWRON Reset Mode	Shut down >TRESET
	TRESET Delay	2 sec
	STANDBY Polarity	STANDBY Active High
	PGOOD Pin Mode	PGOOD Indicator
	OV/UV Check On Power Up	PGOOD monitoring on PWRUP enabled
	EWARN Time	0.1ms
	XFAILB Operation	XFAILB Operation Disabled
	FSOB Soft Fault Event	Event does not assert FSOB
	FSOB Hard Fault Event	Event does not assert FSOB
	FSOB WDI Event	Event does not assert FSOB
	FSOB WDC Event	Event does not assert FSOB

Table 4. Sequencer configuration

Functional block	Feature	OTP selection
SW configurations	SW1 Multiphase Selector	SW1/2 Dual Phase
	SW4 Multiphase Selector	SW3/4 Single Phase
	SW5 Multiphase Selector	SW5/6 Single Phase
	Default SW Operation	SW Regulators Default in PWM mode

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	SW6 VTT Mode	VTT Mode Disabled
	Bandgap Monitor Reaction	BGMON shutdown Bypassed
	VTT Discharge Mode	VTT Output Disable in HI-Z
Power-up sequence	Sequencer Time Base	500 μ s
	SW1 Sequence	Slot 1
	SW2 Sequence	Slot 1
	SW3 Sequence	Slot 61
	SW4 Sequence	Slot 1
	SW5 Sequence	Slot 61
	SW6 Sequence	Slot 61
	SW7 Sequence	Slot 121
	LDO1 Sequence	Slot 57
	LDO2 Sequence	Slot 121
	LDO3 Sequence	Slot 121
	LDO4 Sequence	Slot 121
	RESETBMCU Sequence	Slot 181
	PGOOD Sequence	Slot 181
Power down sequence	Power Down Mode	Mirror power up sequence
	SW1 Power Down Group	Group 4 (1st)
	SW2 Power Down Group	Group 4 (1st)
	SW3 Power Down Group	Group 3
	SW4 Power Down Group	Group 4 (1st)
	SW5 Power Down Group	Group 3
	SW6 Power Down Group	Group 3

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	SW7 Power Down Group	Group 2
	LDO1 Power Down Group	Group 3
	LDO2 Power Down Group	Group 1 (Last)
	LDO3 Power Down Group	Group 1 (Last)
	LDO4 Power Down Group	Group 1 (Last)
	RESETBMCU Power Down Group	Group 4 (1st)
	PGOOD Power Down Group	Group 4 (1st)
Power Down Delays	Group 1 Power Down Delay	120 μ s
	Group 2 Power Down Delay	120 μ s
	Group 3 Power Down Delay	120 μ s
	Group 4 Power Down Delay	120 μ s
	RESETBMCU Group Delay	10 μ s
	Power Down Delay	5 ms

Table 5. Switching regulators

Functional block	Feature	OTP selection
SW1	SW1 Output Voltage	0.75000 V
	SW1 DVS Ramp	7.813/5.208 mV/ μ s
	SW1 UV Threshold	93%
	SW1 OV Threshold	107%
	SW1 Current Limit	4.5 A
	SW1 Inductor	1 μ H
	SW1 Phase	0°
	SW1 PGOOD Control	Reg. is part of AND function to control PGOOD
	SW1 WD Bypass	Regulator reacts upon a Watchdog

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	SW1 OV Bypass	OV Fault Bypassed
	SW1 UV Bypass	UV Fault Bypassed
	SW1 ILIM Bypass	ILIM Fault Bypassed
SW2	SW2 Output Voltage	0.75000 V
	SW2 DVS Ramp	7.813/5.208 mV/μs
	SW2 UV Threshold	93%
	SW2 OV Threshold	107%
	SW2 Current Limit	4.5 A
	SW2 Inductor	1 μH
	SW2 Phase	180°
	SW2 PGOOD Control	Reg. is part of AND function to control PGOOD
	SW2 WD Bypass	Regulator reacts upon a Watchdog
	SW2 OV Bypass	OV Fault Bypassed
	SW2 UV Bypass	UV Fault Bypassed
	SW2 ILIM Bypass	ILIM Fault Bypassed
SW3	SW3 Output Voltage	1.80000 V
	SW3 DVS Ramp	7.813/5.208 mV/μs
	SW3 UV Threshold	93%
	SW3 OV Threshold	107%
	SW3 Current Limit	4.5 A
	SW3 Inductor	1 μH
	SW3 Phase	135°
	SW3 PGOOD Control	Reg. is part of AND function to control PGOOD
	SW3 WD Bypass	Regulator reacts upon a Watchdog

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	SW3 OV Bypass	OV Fault Bypassed
	SW3 UV Bypass	UV Fault Bypassed
	SW3 ILIM Bypass	ILIM Fault Bypassed
SW4	SW4 Output Voltage	0.80000 V
	SW4 DVS Ramp	7.813/5.208 mV/μs
	SW4 UV Threshold	93%
	SW4 OV Threshold	107%
	SW4 Current Limit	4.5 A
	SW4 Inductor	1 μH
	SW4 Phase	180°
	SW4 PGOOD Control	Reg. is part of AND function to control PGOOD
	SW4 WD Bypass	Regulator reacts upon a Watchdog
	SW4 OV Bypass	OV Fault Bypassed
	SW4 UV Bypass	UV Fault Bypassed
	SW4 ILIM Bypass	ILIM Fault Bypassed
SW5	SW5 Output Voltage	1.10000 V
	SW5 DVS Ramp	7.813/5.208 mV/μs
	SW5 UV Threshold	93%
	SW5 OV Threshold	107%
	SW5 Current Limit	4.5 A
	SW5 Inductor	1 μH
	SW5 Phase	0°
	SW5 PGOOD Control	Reg. is part of AND function to control PGOOD
	SW5 WD Bypass	Regulator reacts upon a Watchdog

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	SW5 OV Bypass	OV Fault Bypassed
	SW5 UV Bypass	UV Fault Bypassed
	SW5 ILIM Bypass	ILIM Fault Bypassed
SW6	SW6 Output Voltage	0.60000 V
	SW6 DVS Ramp	7.813/5.208 mV/μs
	SW6 UV Threshold	93%
	SW6 OV Threshold	107%
	SW6 Current Limit	4.5 A
	SW6 Inductor	1 μH
	SW6 Phase	180°
	SW6 PGOOD Control	Reg. is part of AND function to control PGOOD
	SW6 WD Bypass	Regulator reacts upon a Watchdog
	SW6 OV Bypass	OV Fault Bypassed
	SW6 UV Bypass	UV Fault Bypassed
	SW6 ILIM Bypass	ILIM Fault Bypassed
SW7	SW7 Output Voltage	3.30 V
	SW7 UV Threshold	93%
	SW7 OV Threshold	107%
	SW7 Current Limit	4.5 A
	SW7 Inductor	1 μH
	SW7 Phase	135°
	SW7 PGOOD Control	Reg. is part of AND function to control PGOOD
	SW7 WD Bypass	Regulator reacts upon a Watchdog
	SW7 OV Bypass	OV Fault Bypassed

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	SW7 UV Bypass	UV Fault Bypassed
	SW7 ILIM Bypass	ILIM Fault Bypassed

Table 6. LDO regulators

Functional block	Feature	OTP selection
LDO1	LDO1 Output Voltage	1.8 V
	LDO1 UV Threshold	93%
	LDO1 OV Threshold	107%
	LDO1 PGOOD Control	Reg. is part of AND function to control PGOOD
	LDO1 WD Bypass	Regulator reacts upon a Watchdog
	LDO1 Mode	Normal Mode
	LDO1 OV Bypass	OV Fault Bypassed
	LDO1 UV Bypass	UV Fault Bypassed
	LDO1 ILIM Bypass	ILIM Fault Bypassed
LDO2	LDO2 Output Voltage	3.15 V
	LDO2 UV Threshold	93%
	LDO2 OV Threshold	107%
	LDO2 PGOOD Control	Reg. is part of AND function to control PGOOD
	LDO2 WD Bypass	Regulator reacts upon a Watchdog
	LDO2 Mode	Normal Mode
	LDO2EN Hardware Control	I2C Control Only
	VSELECT Hardware Control	LDO2 set by VLDO2_RUN bits
	LDO2 OV Bypass	OV Fault Bypassed
	LDO2 UV Bypass	UV Fault Bypassed
	LDO2 ILIM Bypass	ILIM Fault Bypassed

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LDO3	LDO3 Output Voltage	1.8 V
	LDO3 UV Threshold	93%
	LDO3 OV Threshold	107%
	LDO3 PGOOD Control	Reg. is part of AND function to control PGOOD
	LDO3 WD Bypass	Regulator reacts upon a Watchdog
	LDO3 Mode	Normal Mode
	LDO3 OV Bypass	OV Fault Bypassed
	LDO3 UV Bypass	UV Fault Bypassed
	LDO3 ILIM Bypass	ILIM Fault Bypassed
LDO4	LDO4 Output Voltage	3.3 V
	LDO4 UV Threshold	93%
	LDO4 OV Threshold	107%
	LDO4 PGOOD Control	Reg. is part of AND function to control PGOOD
	LDO4 WD Bypass	Regulator reacts upon a Watchdog
	LDO4 Mode	Normal Mode
	LDO4 OV Bypass	OV Fault Bypassed
	LDO4 UV Bypass	UV Fault Bypassed
	LDO4 ILIM Bypass	ILIM Fault Bypassed
VSNVS	VSNVS Output Voltage	1.8V

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