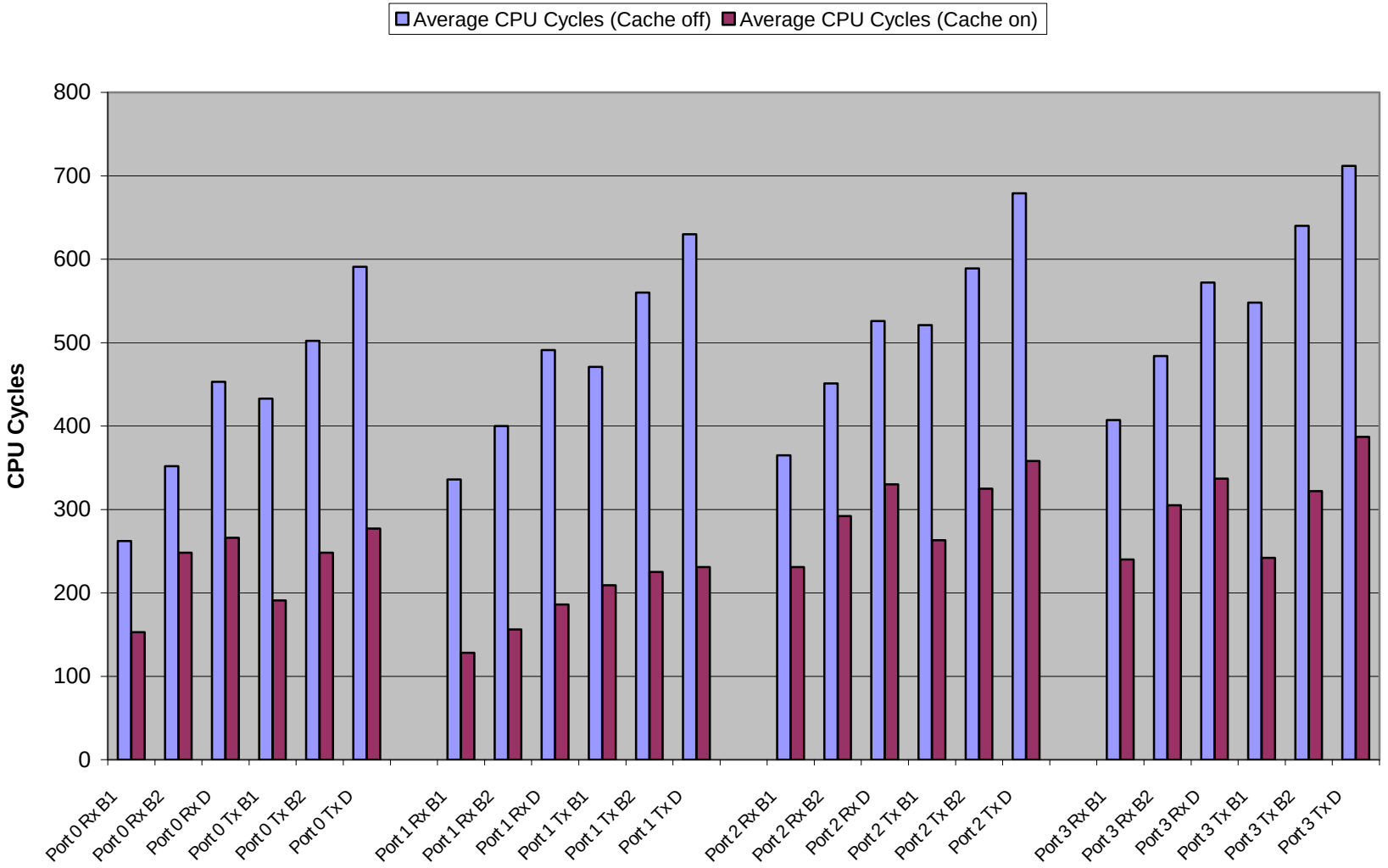
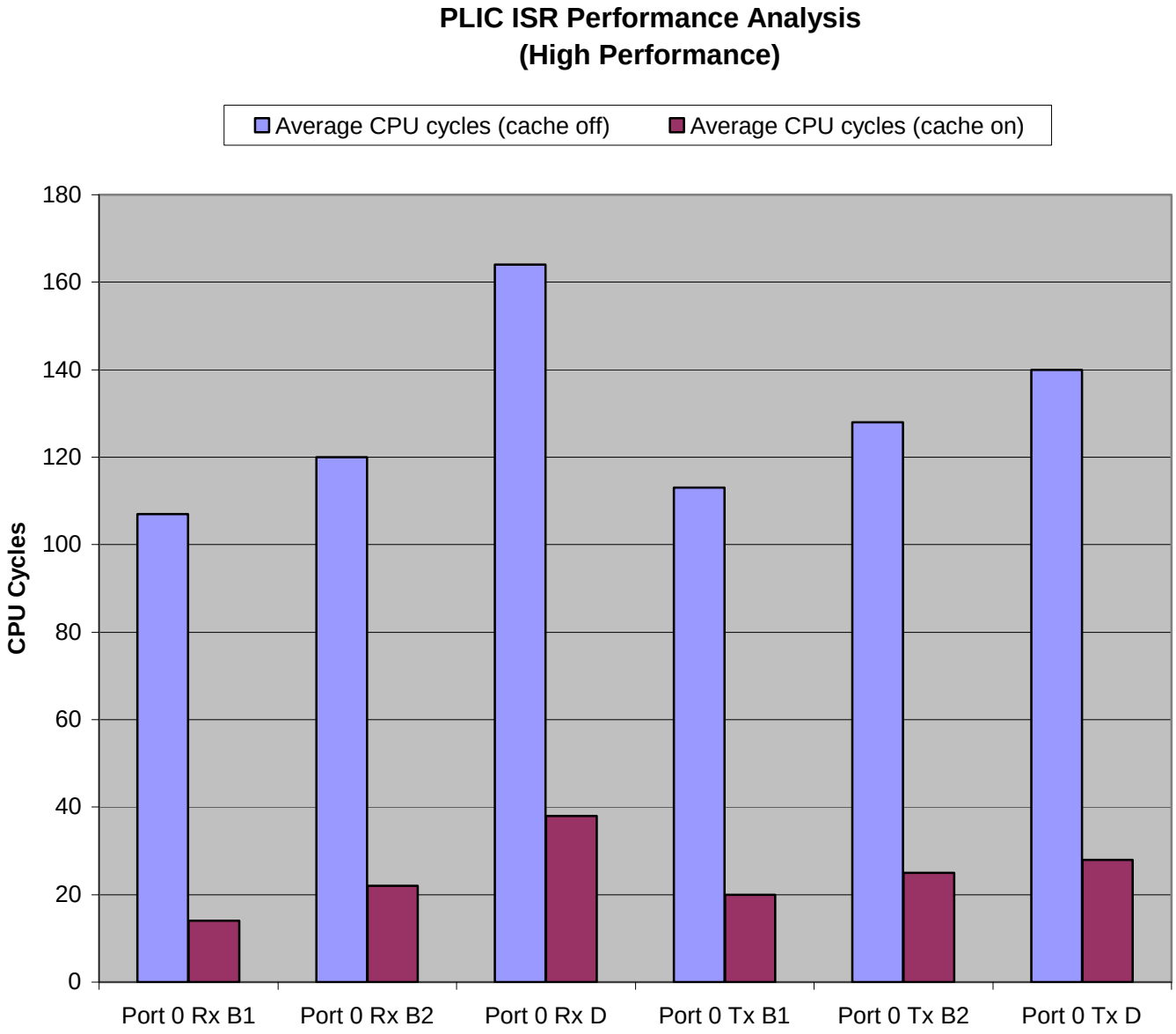
PLIC ISR Performance Analysis
(General Purpose)



Note: This performance analysis is based on the Interrupt Service Routine found in Application Note AN2184.

Operation	Average CPU Cycles (Cache off)	Average CPU Cycles (Cache on)		Comments
Port 0 Rx B1	262	153		These measurments were taken on the M5272C3 running the General Purpose PLIC ISR code packaged in the MCF5272 Initialization Template.
Port 0 Rx B2	352	248		
Port 0 Rx D	453	266		
Port 0 Tx B1	433	191		
Port 0 Tx B2	502	248		
Port 0 Tx D	591	277		
				The 'CPU Cycles' fields measure the execution of the Interrupt Service Routine I_PLI_Periodic() running in SDRAM found in Application Note, AN2184. These routines can be found in the file PerIntVectors.s.
Port 1 Rx B1	336	128		
Port 1 Rx B2	400	156		
Port 1 Rx D	491	186		
Port 1 Tx B1	471	209		
Port 1 Tx B2	560	225		
Port 1 Tx D	630	231		
Port 2 Rx B1	365	231		
Port 2 Rx B2	451	292		
Port 2 Rx D	526	330		
Port 2 Tx B1	521	263		
Port 2 Tx B2	589	325		
Port 2 Tx D	679	358		
Port 3 Rx B1	407	240		
Port 3 Rx B2	484	305		
Port 3 Rx D	572	337		
Port 3 Tx B1	548	242		
Port 3 Tx B2	640	322		
Port 3 Tx D	712	387		


PLIC ISR Performance Analysis
(High Performance)
Average CPU cycles (cache off)
Average CPU cycles (cache on)
CPU Cycles
180
160
140
120
100
80
60
40
20
0
Port 0 Rx B1
Port 0 Rx B2
Port 0 Rx D
Port 0 Tx B1
Port 0 Tx B2
Port 0 Tx D

Operation	Average CPU Cycles (Cache off)	Average CPU Cycles (Cache on)		Comments
Port 0 Rx B1	107	14		These measurments were taken on the M5272C3 running the High Performance PLIC ISR code packaged in the MCF5272 Initialization Template.
Port 0 Rx B2	120	22		
Port 0 Rx D	164	38		
Port 0 Tx B1	113	20		
Port 0 Tx B2	128	25		
Port 0 Tx D	140	28		
				The 'CPU Cycles' fields measure the execution of the PLIC Interrupt Service Routine, an optimized version of I_PLI_Periodic(), running in SDRAM. The performance for the remaining ports will be very similar.