



PF8200ES - NXP General

Configuration report for PF8200 OTP program ID: ES

Rev. A — 9 September 2019

Report

1 General description

The PF8200 is a power management integrated circuit (PMIC) designed for high performance i.MX 8 and S32V based applications. It features seven high efficiency buck converters and four linear regulators for powering the processor, memory and miscellaneous peripherals. It meets the stringent requirements of automotive applications and is fully AEC-Q100 grade 2 qualified.

Built-in one time programmable memory stores key startup configurations, drastically reducing external components typically used to set output voltage and sequence of external regulators. Regulator parameters are adjustable through high-speed I²C after start up offering flexibility for different system states.

Note: Electrical characteristics are maintained in the PF8100_PF8200 data sheet

2 Features and benefits

- Up to seven high efficiency buck converters
- Four linear regulators with load switch options
- RTC supply and coin cell charger
- Watchdog monitoring
- Independent OV/UV monitoring circuits
- One-time programmable device configuration
- 3.4 MHz I²C communication interface
- 56-pin 8 x 8 QFN package
- AEC-Q100 grade 2 qualified
- Safety mechanisms to fit ASIL B applications

3 Applications

- Automotive infotainment
- High-end consumer and industrial

4 Ordering information

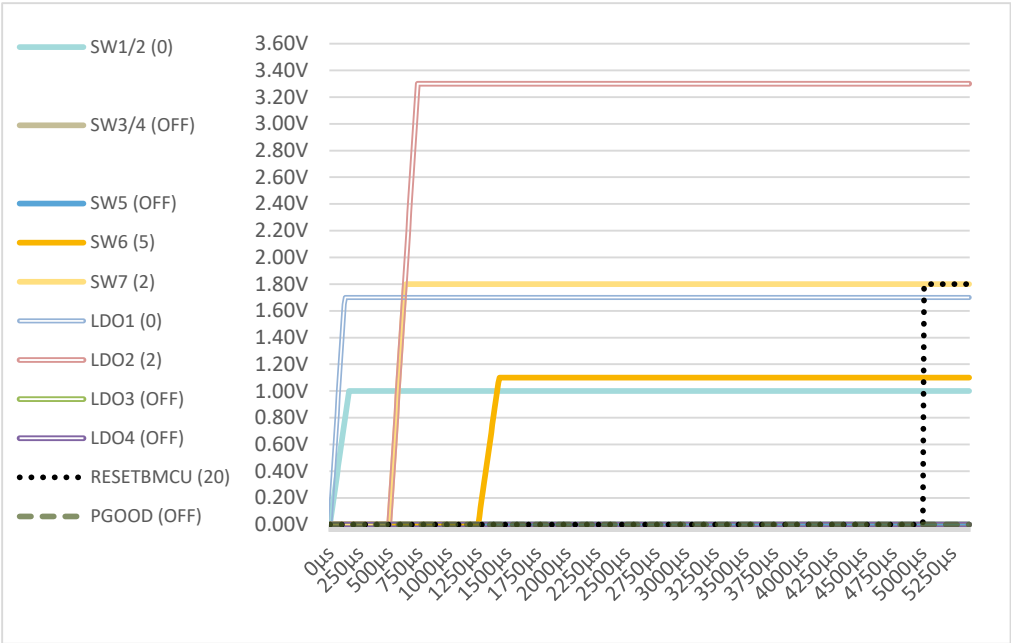
Table 1. Ordering information

Type number ^[1]	Package		
	Name	Description	Version
MC33PF8200ESES	WF-Type HVQFN56	HVQFN56, plastic, thermally enhanced very thin quad; flat non-leaded package, wettable flanks; 56 terminals; 0.5 mm pitch; 8 mm x 8 mm x 0.85 mm body	SOT684-21 (DD/SC)

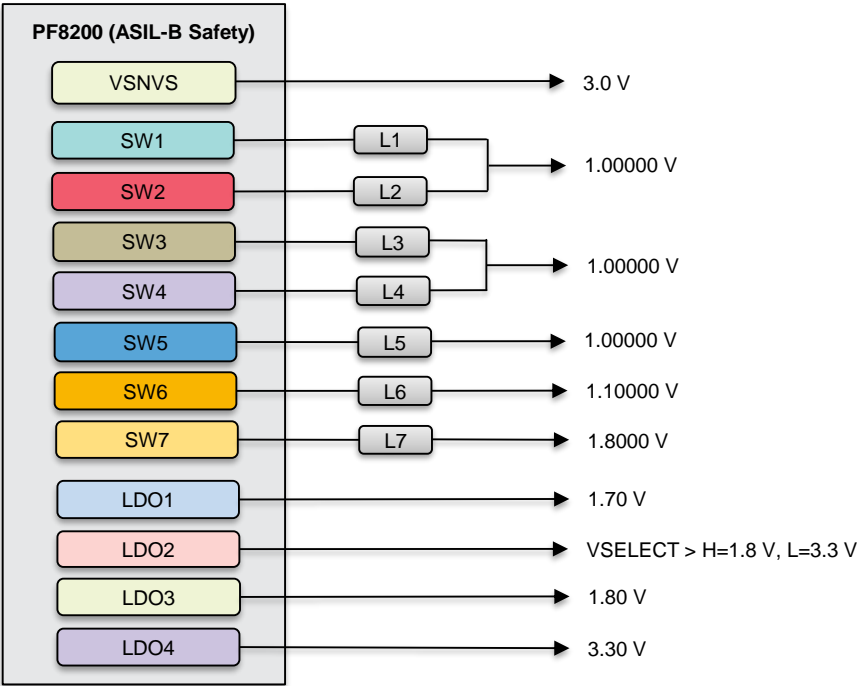
[1] To order parts in tape and reel, add the R2 suffix to the part number.



5 Power up sequence summary



6 Hardware configuration diagram



7 OTP configuration

See PF8100_PF8200 data sheet for parametric details. The OTP configuration summary for ES (sequence ID) is provided in Table 2, Table 3 and Table 4.

Table 2. Device OTP configuration

Functional block	Feature	OTP selection
I ² C settings	Device address	0x08
	I ² C CRC	Enabled
VIN OV lockout	VIN_OVLO	Enabled
	VIN_OVLO shutdown	Disabled
	VIN_OVLO debounce	100 µs
Power good	PG check on power up	RESETBMCU is released regardless of the OV/UV status
	PGOOD pin operation	Power good indicator
	PGOOD pin controlled by	SW1, SW2, SW3, SW4, SW5, SW6, SW7, LDO1, LDO2, LDO3, LDO4
PWRON control	Power on event detection	Level sensitive
	PWRON debounce	32 ms
	TRESET time	2 sec
	TRESET behavior	PMIC shutdown
STANDBY control	STANDBY polarity	STANDBY active high
EWARN timer	EWARN delay	0.1 ms before power down sequence
XFAILB pin	XFAIL operation	XFAILB operation enabled
FSOB control	FSOB operating mode	Fault status mode
	Assertion on hard-fault event	Disabled
	Assertion on WD timer event	Disabled
	Assertion on WDI event	Disabled
	Assertion on soft-fault event	Disabled
WDI control	WDI reset type	Hard WD reset
	WDI polarity	WDI event detected on rising edge
	WDI detection in standby	Disabled
	Regulators affected by WDI event	n/a
Watchdog timer control	WD timer	Disabled at power-up
	WD clear window	100 % window
	WD window duration	1024 ms
	Expire fails before WD event	8
	Maximum WD event counter	16
	WD timer in standby	Disabled
Frequency control	Nominal switching frequency	2.5 MHz
	SYNCOUT operation	Disabled
	SYNCIN operation	Disabled
	Frequency spread spectrum	Disabled
ASILB functional safety	Fail safe state	Disabled
	Max FS counter	16
	FS self-clear timer	60 min
	Bandgap comparator	Shutdown enabled
	Secure write	Disabled

Table 2. Device OTP configuration

Functional block	Feature	OTP selection
Fault management	Fault timer	Disabled
	Maximum fault counter	Disabled
	OV bypass selection	No OV bypass selected
	UV bypass selection	No UV bypass selected
	ILIM bypass selection	SW1, SW2, SW3, SW4, SW5, SW6, SW7, LDO1, LDO2, LDO3, LDO4
Switching mode	Default SW operating mode	PWM

Table 3. Sequencer OTP configuration

Functional block	Feature	OTP selection
Power up sequencing	Sequencer TBASE	250 μ s
	SW1 sequence slot	0
	SW2 sequence slot	0
	SW3 sequence slot	Regulator disabled
	SW4 sequence slot	Regulator disabled
	SW5 sequence slot	Regulator disabled
	SW6 sequence slot	5
	SW7 sequence slot	2
	LDO1 sequence slot	0
	LDO2 sequence slot	2
	LDO3 sequence slot	Regulator disabled
	LDO4 sequence slot	Regulator disabled
	RESETBMCU sequence slot	20
	PGOOD sequence slot	PGOOD not set in sequence
Power down sequencing	Power down mode	Mirror power up sequence
	SW1 power down group	Group 4 (1st)
	SW2 power down group	Group 4 (1st)
	SW3 power down group	Group 4 (1st)
	SW4 power down group	Group 4 (1st)
	SW5 power down group	Group 4 (1st)
	SW6 power down group	Group 4 (1st)
	SW7 power down group	Group 4 (1st)
	LDO1 power down group	Group 4 (1st)
	LDO2 power down group	Group 4 (1st)
	LDO3 power down group	Group 4 (1st)
	LDO4 power down group	Group 4 (1st)
	PGOOD power down group	Group 4 (1st)
	RESETBMCU power down group	Group 4 (1st)
	RESETBMCU group delay	10 μ s
	Group 1 power down delay	120 μ s
	Group 2 power down delay	120 μ s
	Group 3 power down delay	120 μ s
	Group 4 power down delay	120 μ s
	Power down delay	5.0 ms

Table 4. Regulators OTP configuration

Functional block	Feature	OTP selection
SW1 (Dual phase master)	Output voltage	1.0 V
	Current limit	4.5 A
	OV detection threshold	107 %
	UV detection threshold	93 %
	DVS ramp	6.25 mV/μs
	Switching phase	0°
	Output inductor	1.0 μH
SW2 (Dual phase slave)	Output voltage	1.0 V
	Current limit	4.5 A
	OV detection threshold	107 %
	UV detection threshold	93 %
	DVS ramp	6.25 mV/μs
	Switching phase	225°
	Output inductor	1.0 μH
SW3 (Dual phase slave)	Output voltage	1.0 V
	Current limit	4.5 A
	OV detection threshold	107 %
	UV detection threshold	93 %
	DVS ramp	6.25 mV/μs
	Switching phase	0°
	Output inductor	1.0 μH
SW4 (Dual phase master)	Output voltage	1.0 V
	Current limit	4.5 A
	OV detection threshold	107 %
	UV detection threshold	93 %
	DVS ramp	6.25 mV/μs
	Switching phase	225°
	Output inductor	1.0 μH
SW5 (Single phase)	Output voltage	1.0 V
	Current limit	4.5 A
	OV detection threshold	107 %
	UV detection threshold	93 %
	DVS ramp	6.25 mV/μs
	Switching phase	270°
	Output inductor	1.0 μH
SW6 (Single phase)	Output voltage	1.1 V
	Current limit	4.5 A
	OV detection threshold	107 %
	UV detection threshold	93 %
	DVS ramp	6.25 mV/μs
	Switching phase	45°
	Output inductor	1.0 μH
SW7	VTT mode	Disabled
	Output voltage	1.8 V
	Current limit	2.6 A
	OV detection threshold	107 %
	UV detection threshold	93 %
	Switching phase	315°
	Output inductor	1.0 μH

Table 4. Regulators OTP configuration

Functional block	Feature	OTP selection
LDO1 regulator	Output voltage	1.7 V
	OV detection threshold	107 %
	UV detection threshold	93 %
	Operating mode	LDO mode
LDO2 regulator	Output voltage	3.3 V
	OV detection threshold	107 %
	UV detection threshold	93 %
	Operating mode	LDO mode
	LDO2EN hardware control	Disabled
	VSELECT hardware control	Enabled
LDO3 regulator	Output voltage	1.8 V
	OV detection threshold	107 %
	UV detection threshold	93 %
	Operating mode	LDO mode
LDO4 regulator	Output voltage	3.3 V
	OV detection threshold	107 %
	UV detection threshold	93 %
	Operating mode	LDO mode
VSNVS	Output voltage	3.0 V
Coincell	Coin cell voltage	3.0 V

8 Legal information

8.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

8.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with

their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Suitability for use in automotive applications — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

8.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

NXP — is a trademark of NXP B.V.

Contents

1. General description	1
2. Features and benefits	1
3. Applications	1
4. Ordering information	1
5. Power up sequence summary	2
6. Hardware configuration diagram	2
7. OTP configuration	3
8. Legal information	7

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2019.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 9 September 2019

Document identifier: R_PF8200ES