



# FS8430G2

## Configuration report for FS8430 OTP program ID: G2

Rev 1.0 — 13 February 2020

Report

## 1 General description

The FS85/FS84 device family is developed in compliance with ASIL D process, FS84 is ASIL B capable and FS85 is ASIL D capable. All device options are pin to pin and software compatible.

The FS85/FS84 is an automotive functionally safe multi-output power supply integrated circuit, with focus on Radar, Vision, ADAS domain controller, Radio and Infotainment applications. It includes multiple switch mode and linear voltage regulators. It offers external frequency synchronization input and output, for optimized system EMC performance.

The FS85/FS84 includes enhanced safety features, with fail-safe output, becoming a full part of a safety-oriented system partitioning, covering both ASIL B and ASIL D safety integrity level. It is developed in compliance with ISO 26262 standard.

Several device versions are available, offering choice in number of output rails, output voltage setting, operating frequency and power up sequencing, to address multiple applications.

*Note: All parametric information is maintained in FS84\_FS85 datasheet*

## 2 Features and benefits

- 60 V DC maximum input voltage for 12 V and 24 V applications
- VPRE synchronous buck controller with external MOSFETs. Configurable output voltage, switching frequency, and current capability up to 10 A peak.
- Low voltage integrated synchronous BUCK1 converter, dedicated to MCU core supply with SVS capability. Configurable output voltage and current capability up to 3.6 A peak.
- **Based on device options:** low voltage integrated synchronous BUCK2 converter. Configurable output voltage and current capability up to 3.6 A peak. Multi-phase capability with BUCK1 to extend the current capability up to 7.2 A peak on a single rail. Static voltage scaling capability.
- **Based on device options:** low voltage integrated synchronous BUCK3 converter. Configurable output voltage and current capability up to 3.6 A peak.
- BOOST converter with integrated low-side switch. Configurable output voltage and max input current up to 1.5 A peak.
- EMC optimization techniques including SMPS frequency synchronization, spread spectrum, slew rate control, manual frequency tuning
- 2x linear voltage regulators for MCU I/Os and ADC supply, external physical layer. Configurable output voltage and current capability up to 400 mA DC.
- Standby OFF mode with very low sleep current (10  $\mu$ A typ)
- 2x input pins for wake-up detection and battery voltage sensing
- Device control via 32 bits SPI or I2C interface with CRC
- Power synchronization pin to operate 2x FS85 devices or FS85 plus an external PMIC
- Scalable portfolio from ASIL B to ASIL D with independent monitoring circuitry, dedicated interface for MCU monitoring, simple and challenger watchdog function, power good, reset and interrupt, built-in self-test, fail-safe output
- Configuration by OTP programming. Prototype enablement to support custom setting during project development in engineering mode.



3 Applications

- Radar
- Vision
- ADAS domain controller
- Radio
- V2x

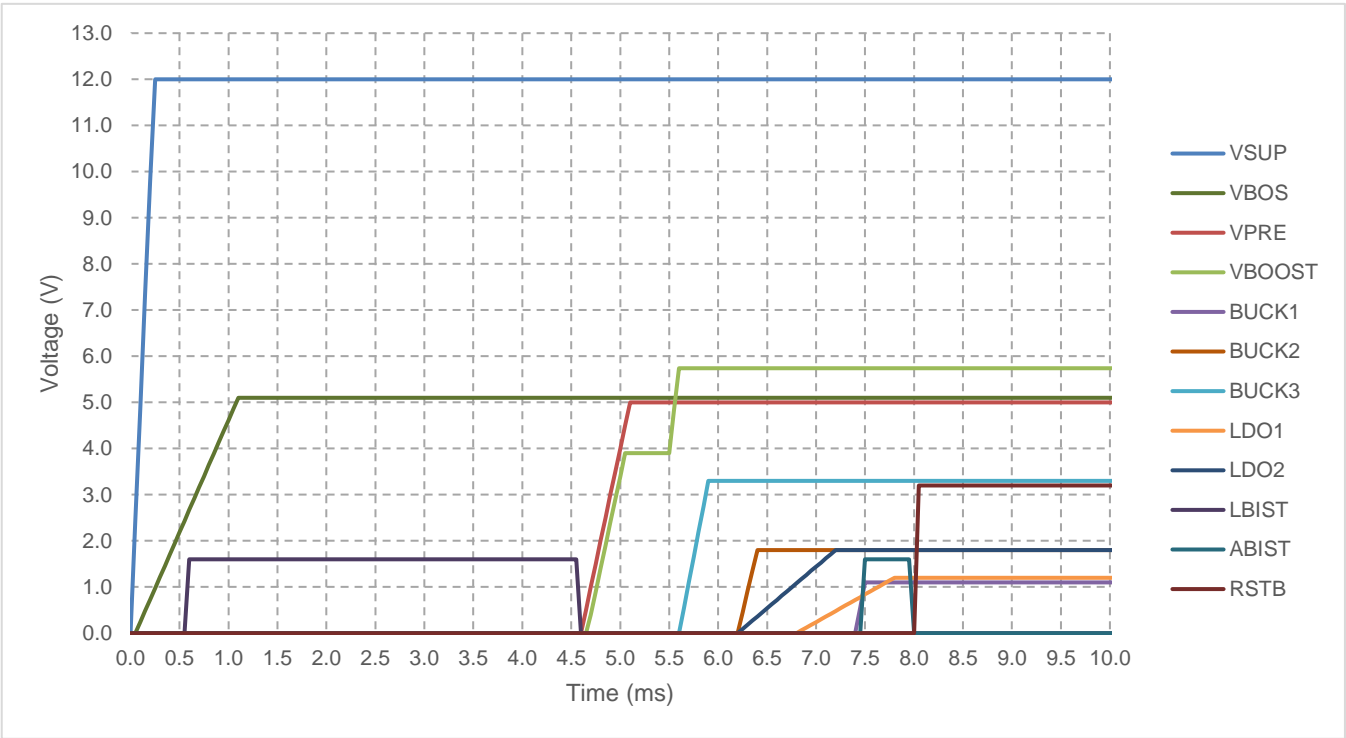
4 Ordering information

Table 1. Ordering Information

| Type number <sup>[1]</sup> | Package |   |           |
|----------------------------|---------|---|-----------|
|                            | Name    | Description   | Version   |
| FS8430G2                   | HVQFN56 | HVQFN56, plastic, thermally enhanced very thin quad; flat non-leaded package, wettable flanks; 56 terminals; 0.5 mm pitch; 8 mm x 8 mm x 0.85 mm body | SOT684-23 |

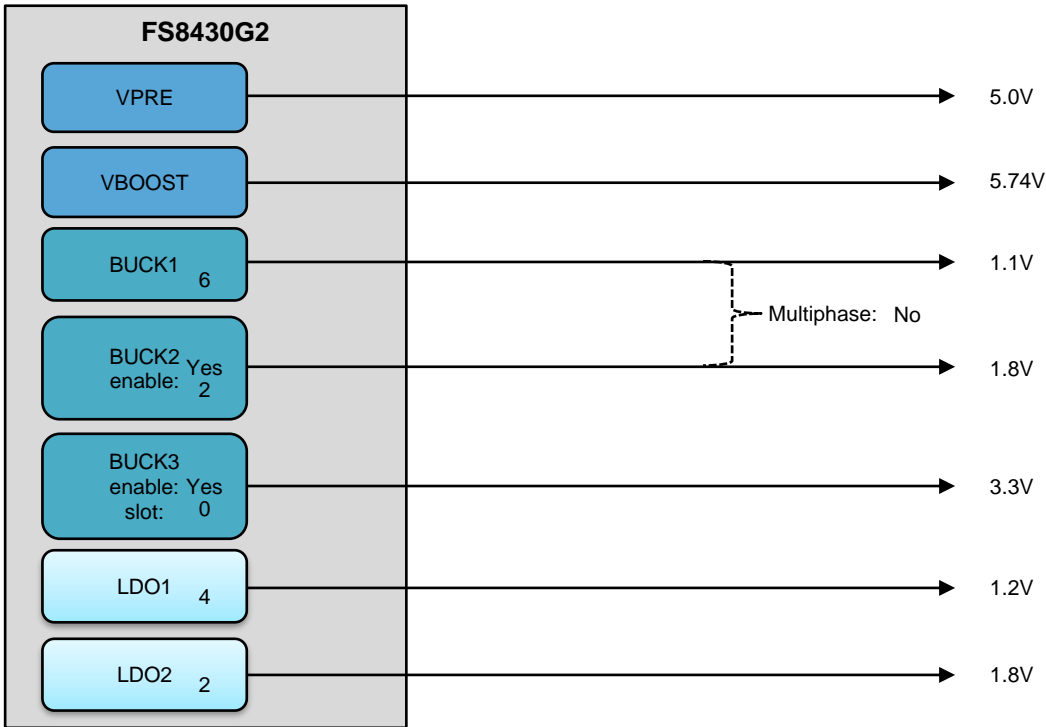
[1] To order parts in tape and reel, add the R2 suffix to the part number.

5 Power up sequence summary



Note: VBOS is set at 5.1 V and RSTB at 3.2 V or 4.9 V to differentiate from regulators on the graph

## 6 Hardware configuration diagram



## 7 OTP configuration

Table 2. Main OTP configuration

| Functional block | Feature             | OTP selection |
|------------------|---------------------|---------------|
| VPRE             | Output voltage      | 5.0V          |
|                  | Slope compensation  | 70mV/μs       |
|                  | Current limitation  | 150mV         |
|                  | High Side slew rate | PU/PD/130mA   |
|                  | Low Side slew rate  | PU/PD/900mA   |
|                  | Switching frequency | 455KHz        |
|                  | Phase shifting      | delay 0       |
|                  | Turn OFF delay      | 250μs         |
|                  | VPRE mode           | Force PWM     |

Table 2. Main OTP configuration (continued)

| Functional block | Feature | OTP selection |
|------------------|---------|---------------|
| VBOOST           | Enabled | Yes           |

|              |                         |                                    |
|--------------|-------------------------|------------------------------------|
|              | Output voltage          | 5.74V                              |
|              | Slope compensation      | 160mV/μs                           |
|              | Slew rate               | 500V/μs                            |
|              | Compensation resistor   | 750kohms                           |
|              | Compensation capacitor  | 125pF                              |
|              | Switching frequency     | 2.22MHz                            |
|              | Phase shifting          | delay 0                            |
|              | Behavior in case of TSD | BOOST Shutdown                     |
| <b>BUCK1</b> | Output voltage          | 1.1V                               |
|              | Inductor                | 1μH                                |
|              | Current limitation      | 4.5A                               |
|              | Compensation network    | 65 GM                              |
|              | Switching frequency     | 2.22MHz                            |
|              | Phase shifting          | delay 0                            |
|              | Behavior in case of TSD | BUCK1 Shutdown                     |
|              | Power sequencing slot   | Regulator Start and Stop in Slot 6 |
|              | Soft start ramp         | 7.81mV/μs                          |
| <b>BUCK2</b> | Enabled                 | Yes                                |
|              | Output voltage          | 1.8V                               |
|              | Inductor                | 1μH                                |
|              | Current limitation      | 4.5A                               |
|              | Compensation network    | 65 GM                              |
|              | Switching frequency     | 2.22MHz                            |
|              | Multiphase with Buck1   | No                                 |
|              | Phase shifting          | delay 0                            |
|              | Behavior in case of TSD | BUCK2 Shutdown                     |
|              | Power sequencing slot   | Regulator Start and Stop in Slot 2 |
|              | Soft start ramp         | 7.81mV/μs                          |

Table 2. Main OTP configuration (continued)

| Functional block | Feature               | OTP selection |
|------------------|-----------------------|---------------|
| <b>BUCK3</b>     | Enabled               | Yes           |
|                  | Output voltage        | 3.3V          |
|                  | Inductor              | 1μH           |
|                  | Current limitation    | 4.5A          |
|                  | Compensation resistor | Default       |

|               |                             |                                    |
|---------------|-----------------------------|------------------------------------|
|               | Gain control                | Default                            |
|               | Switching frequency         | 2.22MHz                            |
|               | Phase shifting              | delay 0                            |
|               | Behavior in case of TSD     | BUCK3 Shutdown                     |
|               | Power sequencing slot       | Regulator Start and Stop in Slot 0 |
|               | Soft start ramp             | 10.41mV/μs                         |
| LDO1          | Output voltage              | 1.2V                               |
|               | Current limitation          | 400mA                              |
|               | Behavior in case of TSD     | LDO1 Shutdown                      |
|               | Power sequencing slot       | Regulator Start and Stop in Slot 4 |
| LDO2          | Output voltage              | 1.8V                               |
|               | Current limitation          | 400mA                              |
|               | Behavior in case of TSD     | LDO2 Shutdown                      |
|               | Power sequencing slot       | Regulator Start and Stop in Slot 2 |
| Miscellaneous | Power up/down slot duration | 250μs                              |
|               | PSYNC                       | Disabled                           |
|               | PLL enabled                 | No                                 |
|               | Deep Fail Safe (autoretry)  | Infinite                           |
|               | VSUP power-up threshold     | 4.9V for Vpre < 4.5V               |
|               | Regulator assigned to VDDIO | External regulator                 |
|               | I2C address                 | 0x20                               |
|               | Device ID                   | 00000001                           |

Table 3. Fail-safe OTP configuration

| Functional block | Feature            | OTP selection |
|------------------|--------------------|---------------|
| VCOREMON         | Monitoring Voltage | 1.1V          |
|                  | OVTH               | 112%          |
|                  | UVTH               | 88%           |
|                  | OV_DGLT            | 45μs          |
|                  | UV_DGLT            | 40μs          |
|                  | SVS_CLAMP          | No SVS        |
|                  |                    |               |

Table 3. Fail-safe OTP configuration (continued)

| Functional block | Feature            | OTP selection |
|------------------|--------------------|---------------|
| VDDIOMON         | Monitoring Voltage | 3.3V          |
|                  | OVTH               | 112%          |
|                  | UVTH               | 88%           |
|                  | OV_DGLT            | 45μs          |
|                  | UV_DGLT            | 40μs          |
|                  |                    |               |
| VMON1            | OVTH               | 112%          |
|                  | UVTH               | 88%           |

|        |          |      |
|--------|----------|------|
|        | OV_DGLT  | 45µs |
|        | UV_DGLT  | 40µs |
| VMON2  | OVTH     | 112% |
|        | UVTH     | 88%  |
|        | OV_DGLT  | 45µs |
|        | UV_DGLT  | 40µs |
| VMON3  | OVTH     | 112% |
|        | UVTH     | 88%  |
|        | OV_DGLT  | 45µs |
|        | UV_DGLT  | 40µs |
| VMON4  | OVTH     | 112% |
|        | UVTH     | 88%  |
|        | OV_DGLT  | 45µs |
|        | UV_DGLT  | 40µs |
| PGOOD  | VCOREMON | Yes  |
|        | VDDIOMON | Yes  |
|        | VMON1    | Yes  |
|        | VMON2    | Yes  |
|        | VMON3    | No   |
|        | VMON4    | No   |
|        | RSTB     | Yes  |
| ABIST1 | VCOREMON | Yes  |
|        | VDDIOMON | Yes  |
|        | VMON1    | Yes  |
|        | VMON2    | Yes  |
|        | VMON3    | No   |
|        | VMON4    | No   |

Table 3. Fail-safe OTP configuration (continued)

| Functional block | Feature      | OTP selection |
|------------------|--------------|---------------|
| Safety enable    | VMON1        | Yes           |
|                  | VMON2        | Yes           |
|                  | VMON3        | No            |
|                  | VMON4        | No            |
|                  | FCCU         | No            |
|                  | ERRMON       | No            |
|                  | WATCHDOG     | Simple WD     |
|                  | FLT_RECOVERY | No            |
| I2C              | I2C address  | 0x21          |

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