Product Type	Integrated Communication Processor
NXP Part #	LS1088A, LS1084A, LS1048A, LS1044A
Package	23mm x 23mm, .8mm pitch, 780 flip-chip plastic ball grid array (FC-PBGA)
Crypto Hardware	SEC 5.1

Algorithms	**Max Key Size (bits)**
DES (ECB, CBC, OFB, CFB)	56
3DES (ECB, CBC, OFB, CFB)	168 (3-keys)
AES (ECB, CBC, CTR, CCM, CMAC, GCM, OFB, CFB, XCBC-MAC)	256
MD-5 + HMAC	(up to 512 bit keys)
SHA-1 + HMAC	(up to 512 bit keys)
SHA-224 + HMAC	(up to 512 bit keys)
SHA-256 + HMAC	(up to 512 bit keys)
SHA-384 + HMAC	(up to 512 bit keys)
SHA-512 + HMAC	(up to 512 bit keys)
Kasumi (A5/3, GEA-3, f8, f9)	128
Snow 3G	128
ZUC (EEA-1 & EIA-2)	128
RSA Digital Signature	4096-bit operands
RSA Digital Verify	4096-bit operands
ECC Digital Signature	1023-bit field or modulus size
ECC Digital Verify	1023-bit field or modulus size
FIPS compliant deterministic RNG	On chip 32-bit

Target Applications :
Combined control, data path,and application layer processing in routers, switches, gateways, and general-purpose embedded computing systems.

Export Control Info:
Harmonized Tariff (US): 8542.31.0000
ENC Status: Restricted. US EAR part 740.17(b)(2)
ECCN: 5A002A.1
CCAT: G165239

Overview:
The LS1088A, LS1084A, LS1048A, and LS1044A are members of the QorIQ Layerscape family of integrated communications processor from NXP Semiconductor.

The LS1088A incorporates (8) 64b A53 ARM Architecture CPU cores, (1) 64b DDR4 Memory Controllers, (2) 10G Ethernet and (8) 1G Ethernet controllers, along with multiple PCIe and other peripheral bus controllers.

The LS1048A incorporates (4) 64b A53 ARM Architecture CPU cores, (1) 64b DDR4 Memory Controllers, (2) 10G Ethernet and (8) 1G Ethernet controllers, along with multiple PCIe and other peripheral bus controllers.

Both the LS1088A and LS1048A incorporate the AIOP (Advanced IO Processor), a C-programmable packet processing engine.

The LS1084A incorporates (8) 64b A53 ARM Architecture CPU cores, (1) 64b DDR4 Memory Controllers, (2) 10G Ethernet and (8) 1G Ethernet controllers, along with multiple PCIe and other peripheral bus controllers.

The LS1044A incorporates (4) 64b A53 ARM Architecture CPU cores, (1) 64b DDR4 Memory Controllers, (2) 10G Ethernet and (8) 1G Ethernet controllers, along with multiple PCIe and other peripheral bus controllers.

The LS1084A and LS1044A do not incorporate the AIOP (Advanced IO Processor).

All members of this product family integrate a 20Gbps Crypto Acceleration Engine (SEC 5.1). The algorithms and key lengths supported by the SEC 5.1 are listed in the table above.

In addition to crypto algorithm processing, the SEC 5.1 supports security protocol processing off-load capability, with specific support for protocol header and trailer processing for IPsec, SSL, DTLS, SRTP, MACSec, 802.16e, and 802.11e. The SEC 5.1 is expected to achieve 5000+ public key exchanges per second.

All members of this product family also provide support for secure boot and platform assurance, including ARM TrustZone.

NOTE 1: This authorization does not authorize the export of products designed to use the encryption functionality of these chips. Such products may require a classification and/or license from the Bureau of Industry and Security (BIS) prior to export. OEMs incorporating these chips in their products should call the BIS Encryption Export Support Line at 202-482-0707 with specific questions.

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