RN00283

PN5180 Firmware Version 4.0

Rev. 1.1 — 10 April 2025 **Release notes**

Document information

Information	Content
Keywords	PN5180
Abstract	This document describes the known limitations of the PN5180 Firmware 4.0.

1 Document purpose

This document describes the known limitations of the PN5180 Firmware 4.0.

The functionality of the firmware 4.0 together with the hardware PN5180A0HN PN5180A0ET is described in the data sheet of the product PN5180A0HN/C3 PN5180A0ET/C3 ref.[1].

2 FW version history

2.1 Firmware version 3.4

Allows EMVCo 2.3.1 compliant EMD error handling.

Version information:

- EEPROM address 0x12: 0x04
- EEPROM address 0x13: 0x03

2.2 Firmware version 3.5

Allows EMVCo 2.5 compliant EMD error handling.

Version information:

- EEPROM address 0x12: 0x05
- EEPROM address 0x13: 0x03

Changes of version 3.5 compared to version 3.4:

- The EMD_CONTROL register is updated to support EMVCo 2.5.
- Adaptive Waveform Control (AWC) implemented.

2.3 Firmware version 3.6

Automatic Receiver Control added

No silicon initialized with this firmware is available. Usage of this firmware requires an update by the user.

Version information:

- EEPROM address 0x12: 0x06
- EEPROM address 0x13: 0x03

Changes of Version 3.6 compared to Version 3.5:

- Accessible EEPROM top address is changed to 0xFE.
- EEPROM functional assignment starting at address 0xD8.
- EEPROM updates to support using GPO1 during LPCD card detect and GPIO2 during wake-up from standby.
- Adaptive Receiver configuration (ARC) available: EEPROM table updates for receiver configuration.
- Energy of external RF field can be used to operate an external system-power-on Switch.

2.4 Firmware version 3.7

Not released.

2.5 Firmware version 3.8

Firmware version prepared for EMVCo 2.6

Version information:

- EEPROM address 0x12: 0x08
- EEPROM address 0x13: 0x03

Changes of Version 3.6 compared to Version 3.8

- EEPROM configuration for PLL_DEFAULT_SETTING (address 0x1C) had been updated with timer options and persistent testbus configuration added.
- LDO_OUT pin is available for output of regulated 3.3 V, configuration options added to SYSTEM_CONFIG register; SYSTEM_STATUS register is extended by bit LDO_TVDD_OK. THIS FEATURE CAN BE ENABLED ON ALL PN5180 PRODUCT VERSIONS. PRODUCTION TEST OF THIS FEATURE IS PERFORMED ON PN5180A0HN/C3 AND PN5180A0ET/C3 ONLY.
- ACTIVE_MODE_TX_RF_ENABLE added to SYSTEM_CONFIG register.
- The EMD block offers the possibility to stop and restart a CLIF Timer. This selection can be done via register. The firmware 3.8 allows usage of any timer (T0, T1 or T2) as CLIF timer.
- Prepared for EMVCo. 2.6 digital compliancy.

2.6 Firmware version 3.9

Version information:

- EEPROM address 0x12: 0x09
- EEPROM address 0x13: 0x03

Changes of Version 3.8 compared to Version 3.9:

The DPC_XI can be configured in the RAM using SYSTEM_CONFIG, which is used along with the AGC_XI in EEPROM for AGC correction. The DPC_XI in RAM can be used using enable/disable bit in EEPROM. This allows to compensate a temperature shift of the AGC to improve the accuracy of the DPC. (The temperature can be measured externally by the host µC.)

- SYSTEM_CONFIG register bits in range[12-19] are used to configure the 8 bit signed value (+/- 0 to 127).

DPC_XI value in RAM

- In EEPROM, Dynamic DPC_Xi RAM can be enabled/disabled using EEPROM Misc_Config, bit 5.

2.7 Firmware version 3.A

Version information:

- EEPROM address 0x12: 0x09
- EEPROM address 0x13: 0x03

Changes of Version 3.9 compared to Version 3.A:

Supports EMVCo2.6 and more ARC Parameters.

- By Default, the EEPROM LPCD_REFERENCE_VALUE is set to 8
- By Default, the EEPROM LPCD Selection is set to AUTO CALIBRATION.

Bit Field [1:0] 00 - Auto Calibration 01 - Self Calibration 10 & 11 - RFU.

- ARC Parameters supported: MIN_LEVELP, MINLEVEL, RX_HPCF and RX_GAIN. (MIN_LEVEL & MIN_LEVELP can vary b/w +/- 3 , whereas the actual value is 4 bit)

2.8 Firmware version 4.0

Version information:

- EEPROM address 0x12: 0x00
- EEPROM address 0x13: 0x04

Changes of Version 3.A compared to Version 4.0:

No functional difference to Firmware Version 3.A.

3 Possible problems known errors and restrictions

Known errors

none

Restrictions description

none

4 References

[1] Data sheet – PN5180 – High-performance multi-protocol full NFC frontend, supporting all NFC Forum modes (link)

5 Revision history

Table 1. Revision history

Document ID	Release date	Description
RN00283 v.1.1	10 April 2025	Previously published as "RN4342". Document security status changed to "public". Editorial changes to conform to latest NXP standards. • Section "Referenced documents" renamed to Section 4 "References". • Section 4 "References": updated.
RN4342 v.1.0	3 July 2017	• Initial version.

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