RN00280

PN5180 Firmware Version 4.1

Rev. 1.0 — 10 April 2025 **Release notes**

Document information

Information	Content
Keywords	PN5180, NFC frontend controller
Abstract	Contains information about a specific release product and component information.

1 Document purpose

This document describes the tested functionality and limitations of the firmware PN5180 FW v4.1.

It also describes the release summary, release history, known issues, work-arounds, limitations, and recommendations.

The functionality and limitations of the hardware and product support material (for example, customer development board and support software) are described in separate documents.

2 PN5180 firmware version information

PN5180 software package version (including host utilities): v4.1

PN5180 secure firmware version: v02.0B

For new designs, it is recommended to always use the latest firmware version available.

3 Features supported in this release

This section provides the features supported in this firmware/software version release.

3.1 RF protocols

Table 1. RF protocols

Feature/functionality
Reader mode A (106/212/424/848 kbit/s)
Reader mode B (106/212/424/848 kbit/s)
Reader mode FeliCa (212/424 kbit/s)
Reader mode ISO/IEC15693 (26/53/106/212Kbps) - all data rates as specified in the data sheet
Reader mode ISO/IEC18000 3M3 - all data rates as specified in the data sheet
Host card emulation / Card mode ISO/IEC 14443 A-106, A-212, A-424, A-848
Peer-Peer passive communication (ISO18092, PI106, PI212, PI424, PT106, PT212, PT424)
Peer-Peer passive communication with proprietary baud rates (PI212, PI424, PI848, PT212, PT424, PT848)

3.2 Other system features/functionality protocols

Table 2. Other system features

Feature/functionality
EMVCo 3.0 (Digital)
Low Power Card detection

3.3 Compliancy with this firmware and PNEV5180 hardware (customer development board)

Table 3. Compliancy with this firmware and PNEV5190B hardware (customer development board)

Feature/Functionality
EMVCo 3.0 L1 analog compliance

4 Version history

This section contains the firmware release version history only for PN5180 based device firmware.

Table 4. Firmware updates

SI No.	Function/feature update
Firmware version 3.4	Allows EMVCo 2.3.1 compliant EMD error handling Version information: • EEPROM address 0x12: 0x04 • EEPROM address 0x13: 0x03
Firmware version 3.5	Allows EMVCo 2.5 compliant EMD error handling Version information: • EEPROM address 0x12: 0x05 • EEPROM address 0x13: 0x03 Changes of version 3.5 compared to version 3.4: • The EMD_CONTROL register is updated to support EMVCo 2.5. • Adaptive Waveform Control (AWC) implemented
Firmware version 3.6	Automatic Receiver Control added No silicon initialized with this firmware is available. Usage of this firmware requires an update by the user. Version information: • EEPROM address 0x12: 0x06 • EEPROM address 0x13: 0x03 Changes of Version 3.6 compared to Version 3.5: • Accessible EEPROM top address is changed to 0xFE • EEPROM functional assignment starting at address 0xD8 • EEPROM updates to support using GPO1 during LPCD card detect and GPIO2 during wake-up from standby • Adaptive Receiver configuration (ARC) available: EEPROM table updates for receiver configuration • Energy of external RF field can be used to operate an external system-power-on switch
Firmware version 3.7	not released
Firmware version 3.8	Firmware version prepared for EMVCo 2.6 Version information: • EEPROM address 0x12: 0x08 • EEPROM address 0x13: 0x03 Changes of Version 3.6 compared to Version 3.8 • EEPROM configuration for PLL_DEFAULT_SETTING (address 0x1C) had been updated with timer options and persistent test bus configuration added • LDO_OUT pin is available for output of regulated 3.3 V, configuration options added to SYSTEM_CONFIG register; SYSTEM_STATUS register is extended by bit LDO_TVDD_OK. THIS FEATURE CAN BE ENABLED ON ALL PN5180 PRODUCT VERSIONS. PRODUCTION TEST OF THIS FEATURE IS PERFORMED ON PN5180A0HN/C3 AND PN5180A0ET/C3 ONLY. • ACTIVE_MODE_TX_RF_ENABLE added to SYSTEM_CONFIG register • The EMD block offers the possibility to stop and restart a CLIF Timer. This selection can be done via register. The firmware 3.8 allows usage of any timer (T0, T1, or T2) as CLIF timer. • Prepared for EMVCo. 2.6 digital compliancy

Table 4. Firmware updates*...continued*

Sl No.	Function/feature update
Firmware version 3.9	Version information: • EEPROM address 0x12: 0x09 • EEPROM address 0x13: 0x03 Changes of Version 3.8 compared to Version 3.9: The DPC_XI can be configured in the RAM using SYSTEM_CONFIG, which is used along with the AGC_XI in EEPROM for AGC correction. The DPC_XI in RAM can be used using enable/disable bit in EEPROM. This allows to compensate a temperature shift of the AGC to improve the accuracy of the DPC. (The temperature can be measured externally by the host µC.) • SYSTEM_CONFIG register bits in range[12-19] are used to configure the 8 bit signed value (+/- 0 to 127). DPC_XI value in RAM • In EEPROM, Dynamic DPC_Xi RAM can be enabled/disabled using EEPROM Misc_Config, bit 5
Firmware version 3.A	Version information: • EEPROM address 0x12: 0x09 • EEPROM address 0x13: 0x03 Changes of Version 3.9 compared to Version 3.A: Supports EMVCo2.6 and more ARC Parameters • By Default, the EEPROM LPCD_REFERENCE_VALUE is set to 8 • By Default, the EEPROM LPCD Selection is set to AUTO CALIBRATION. Bit Field [1:0] 00 - Auto Calibration 01 - Self Calibration 10 & 11 - RFU. • ARC Parameters supported: MIN_LEVELP, MINLEVEL, RX_HPCF and RX_GAIN. (MIN_LEVEL & MIN_LEVELP can vary b/w +/- 3, whereas the actual value is 4 bit)
Firmware version 4.0	Version information: • EEPROM address 0x12: 0x00 • EEPROM address 0x13: 0x04 Changes of Version 3.A compared to Version 4.0: No functional difference to Firmware Version 3.A.
Firmware version 4.1	Version information: Improved FeliCa EMD handling Fixed corner case behavior of DPC which reduced power by several gears during reception

5 Recommendations, known limitations, and precautions

This section provides the known limitations in the FW/HW recommendations.

5.1 Known limitations

- The host must read all the expected number of bytes. For example, for Read_Reg, the host shall read 4 bytes (not less).
- TxBitPhase loading incorrect for high values: The maximum allowed TxBitPhase value is 0xBF.
- Unexpected Protocol Error for TypeF frame: When receiving a TypeF frame with length byte 0xFF and first data byte 0x00, an unexpected protocol error is indicated and reception stops. This combination of bytes cannot occur in the NFC Forum and JIS X 6319 specification.

5.2 Recommendations

EGT should not be send for the last byte before EOF.

The device supports transmission of an EGT after the stop bit. The standard is interpreted in the way that EGT is transmitted for every byte.

In an update of the standards, it is now clarified that EGT must not be transmitted for the last byte (before EOF). As EGT is not needed and usually not used, this is expected to cause no issues.

6 Revision history

Table 5. Revision history

Document ID	Release date	Description
RN00280 v.1.0	10 April 2025	PN5180 firmware v4.1 release. Initial version.

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