# DSCRTCESL47RN

## DSC RTCESL 4.7 Release Notes

**Rev. 0 — 17 January 2023** **Release notes**

**Document information**

| Information | Content |
|---|---|
| Keywords | DSC, RTCESL, DSP56800EF |
| Abstract | These release notes are for the DSP56800EF Real-Time Control Embedded Software Libraries release 4.7. |

# 1 Overview

These release notes are for the DSP56800EF Real-Time Control Embedded Software Libraries release 4.7.

The purpose of this release is to support the new DSP56800EF core, which contains the Floating Point Unit (eFPU), the trigonometric math unit named CORDIC, and the new fraction, saturation, and divide instructions.

# 2 What is new

The DSP56800EF core contains:

- Floating Point Unit unit (eFPU)
- Trigonometric math unit based on the COordinate Rotation DIgital Computer (CORDIC), calculating the trigonometric function using a hardware unit.
- New divide instructions providing more precise signed or unsigned, fraction or integer, and 32/16 and 32/32 divide operators. The new instructions are used in the following functions: AMCLIB_PMSMBemfObsrvAB_F16, MLIB_DivSat_F16ll, MLIB_DivSat_F32, and MLIB_Div1QSat_F32.

# 3 Description

This release of RTCESL supports the following platforms:

- DSP56800EF

It contains the following libraries:

- MLIB
- GFLIB
- GDFLIB
- GMCLIB
- AMCLIB
- PCLIB

It is compiled on:

- CodeWarrior 11.2 (build 221129)

The following optimization is used:

- The maximum speed optimization is used for all libraries.

The following memory models are used:

- SDM - Small Data Model and Large Program Model. To achieve such configuration, uncheck all Large Data Memory Model and Huge Program Model items and check the Large Program Model item in the CodeWarrior Properties window.
- LDM - Large Data and Large Program Model. To achieve such configuration, uncheck all Small Data Memory Model and Huge Program Model Items and check the Large Data Model and Large Program Model items in the CodeWarrior Properties window.

The selected algorithms support the 16-bit and 32-bit fixed-point and floating-point types.

**This is the list of algorithms contained in this release:**

```
AMCLIB_ACIMCtrlMTPAInit_FLT
AMCLIB_ACIMCtrlMTPA_FLT
AMCLIB_ACIMRotFluxObsrvInit_FLT
AMCLIB_ACIMRotFluxObsrv_FLT
AMCLIB_ACIMSpeedMRASInit_FLT
AMCLIB_ACIMSpeedMRAS_FLT
AMCLIB_AngleTrackObsrvInit_A32
AMCLIB_AngleTrackObsrvInit_F16
AMCLIB_AngleTrackObsrv_A32ff
AMCLIB_AngleTrackObsrv_F16
AMCLIB_CtrlFluxWkngInit_F16
AMCLIB_CtrlFluxWkngInit_FLT
AMCLIB_CtrlFluxWkng_F16
AMCLIB_CtrlFluxWkng_FLT
AMCLIB_PMSMBemfObsrvABInit_F16
AMCLIB_PMSMBemfObsrvABInit_FLT
AMCLIB_PMSMBemfObsrvAB_F16
AMCLIB_PMSMBemfObsrvAB_FLT
AMCLIB_PMSMBemfObsrvDQInit_A32fff
AMCLIB_PMSMBemfObsrvDQInit_F16
AMCLIB_PMSMBemfObsrvDQ_A32fff
AMCLIB_PMSMBemfObsrvDQ_F16
AMCLIB_TrackObsrvInit_A32af
AMCLIB_TrackObsrvInit_F16
AMCLIB_TrackObsrv_A32af
AMCLIB_TrackObsrv_F16
GDFLIB_FilterExpInit_F16
GDFLIB_FilterExpInit_FLT
GDFLIB_FilterExp_F16
GDFLIB_FilterExp_FLT
GDFLIB_FilterIIR1Init_F16
GDFLIB_FilterIIR1Init_FLT
GDFLIB_FilterIIR1_F16
GDFLIB_FilterIIR1_FLT
GDFLIB_FilterIIR2Init_F16
GDFLIB_FilterIIR2Init_FLT
GDFLIB_FilterIIR2_F16
GDFLIB_FilterIIR2_FLT
GDFLIB_FilterIIR3Init_F16
GDFLIB_FilterIIR3Init_FLT
GDFLIB_FilterIIR3_F16
GDFLIB_FilterIIR3_FLT
GDFLIB_FilterIIR4Init_F16
GDFLIB_FilterIIR4Init_FLT
GDFLIB_FilterIIR4_F16
GDFLIB_FilterIIR4_FLT
GDFLIB_FilterMAInit_F16
GDFLIB_FilterMAInit_FLT
GDFLIB_FilterMA_F16
GDFLIB_FilterMA_FLT
GFLIB_Acos_F16
GFLIB_Acos_FLT
GFLIB_Asin_F16
GFLIB_Asin_FLT
GFLIB_AtanYX_A32f
GFLIB_AtanYX_F16
GFLIB_AtanYX_FLT
GFLIB_Atan_A32f
```

```
GFLIB_Atan_F16
GFLIB_Atan_FLT
GFLIB_Cos_F16
GFLIB_Cos_FLT
GFLIB_Cos_FLTa
GFLIB_CtrlBetaIPDpAWInit_F16
GFLIB_CtrlBetaIPDpAWInit_FLT
GFLIB_CtrlBetaIPDpAW_F16
GFLIB_CtrlBetaIPDpAW_FLT
GFLIB_CtrlBetaIPpAWInit_F16
GFLIB_CtrlBetaIPpAWInit_FLT
GFLIB_CtrlBetaIPpAW_F16
GFLIB_CtrlBetaIPpAW_FLT
GFLIB_CtrlPIDpAWInit_F16
GFLIB_CtrlPIDpAWInit_FLT
GFLIB_CtrlPIDpAW_F16
GFLIB_CtrlPIDpAW_FLT
GFLIB_CtrlPIpAWInit_F16
GFLIB_CtrlPIpAWInit_FLT
GFLIB_CtrlPIpAW_F16
GFLIB_CtrlPIpAW_FLT
GFLIB_DFlexRampCalcIncr_F16
GFLIB_DFlexRampCalcIncr_FLT
GFLIB_DFlexRampInit_F16
GFLIB_DFlexRampInit_FLT
GFLIB_DFlexRamp_F16
GFLIB_DFlexRamp_FLT
GFLIB_DRampInit_F16
GFLIB_DRampInit_F32
GFLIB_DRampInit_FLT
GFLIB_DRamp_F16
GFLIB_DRamp_F32
GFLIB_DRamp_FLT
GFLIB_FlexRampCalcIncr_F16
GFLIB_FlexRampCalcIncr_FLT
GFLIB_FlexRampInit_F16
GFLIB_FlexRampInit_FLT
GFLIB_FlexRamp_F16
GFLIB_FlexRamp_FLT
GFLIB_FlexSRampCalcIncr_F16
GFLIB_FlexSRampCalcIncr_FLT
GFLIB_FlexSRampInit_F16
GFLIB_FlexSRampInit_FLT
GFLIB_FlexSRamp_F16
GFLIB_FlexSRamp_FLT
GFLIB_Hyst_F16
GFLIB_Hyst_FLT
GFLIB_IntegratorInit_F16
GFLIB_IntegratorInit_FLT
GFLIB_Integrator_F16
GFLIB_Integrator_FLT
GFLIB_Limit_F16
GFLIB_Limit_F32
GFLIB_Limit_FLT
GFLIB_LowerLimit_F16
GFLIB_LowerLimit_F32
GFLIB_LowerLimit_FLT
GFLIB_Lut1DInit_FLT
GFLIB_Lut1D_F16
GFLIB_Lut1D_F32
```

```
GFLIB_Lut1D_FLT
GFLIB_LutPer1DInit_FLT
GFLIB_LutPer1D_F16
GFLIB_LutPer1D_F32
GFLIB_LutPer1D_FLT
GFLIB_RampInit_F16
GFLIB_RampInit_F32
GFLIB_RampInit_FLT
GFLIB_Ramp_F16
GFLIB_Ramp_F32
GFLIB_Ramp_FLT
GFLIB_Sin_F16
GFLIB_Sin_FLT
GFLIB_Sin_FLTa
GFLIB_Sqrt_F16
GFLIB_Sqrt_F16l
GFLIB_Sqrt_FLT
GFLIB_Tan_F16
GFLIB_Tan_FLT
GFLIB_Tan_FLTa
GFLIB_UpperLimit_F16
GFLIB_UpperLimit_F32
GFLIB_UpperLimit_FLT
GFLIB_VectorLimit1_F16
GFLIB_VectorLimit1_FLT
GFLIB_VectorLimit_F16
GFLIB_VectorLimit_FLT
GMCLIB_ClarkInv_F16
GMCLIB_ClarkInv_FLT
GMCLIB_Clark_F16
GMCLIB_Clark_FLT
GMCLIB_DecouplingPMSM_F16
GMCLIB_DecouplingPMSM_FLT
GMCLIB_DTCompLut1D_F16
GMCLIB_ElimDcBusRipFOC_F16
GMCLIB_ElimDcBusRipFOC_F16ff
GMCLIB_ElimDcBusRip_F16fff
GMCLIB_ElimDcBusRip_F16sas
GMCLIB_ParkInv_F16
GMCLIB_ParkInv_FLT
GMCLIB_Park_F16
GMCLIB_Park_FLT
GMCLIB_SvmDpwm_F16
GMCLIB_SvmExDpwm_F16
GMCLIB_SvmIct_F16
GMCLIB_SvmStd_F16
GMCLIB_SvmStdShifted_F16
GMCLIB_SvmU0n_F16
GMCLIB_SvmU7n_F16
MLIB_AbsSat_F16
MLIB_AbsSat_F32
MLIB_Abs_F16
MLIB_Abs_F32
MLIB_Abs_FLT
MLIB_Add4Sat_F16
MLIB_Add4Sat_F32
MLIB_Add4_F16
MLIB_Add4_F32
MLIB_Add4_FLT
MLIB_AddSat_F16
```

```
MLIB_AddSat_F32
MLIB_Add_A32as
MLIB_Add_A32ss
MLIB_Add_F16
MLIB_Add_F32
MLIB_Add_FLT
MLIB_Clb_U16l
MLIB_Clb_U16s
MLIB_ConvSc_A32ff
MLIB_ConvSc_F16ff
MLIB_ConvSc_F32ff
MLIB_ConvSc_FLTaf
MLIB_ConvSc_FLTlf
MLIB_ConvSc_FLTsf
MLIB_Conv_A32f
MLIB_Conv_F16f
MLIB_Conv_F16l
MLIB_Conv_F32f
MLIB_Conv_F32s
MLIB_Conv_FLTa
MLIB_Conv_FLTl
MLIB_Conv_FLTs
MLIB_Div1QSat_A32as
MLIB_Div1QSat_F16
MLIB_Div1QSat_F16ll
MLIB_Div1QSat_F16ls
MLIB_Div1QSat_F32
MLIB_Div1QSat_F32ls
MLIB_Div1Q_A32as
MLIB_Div1Q_A32ll
MLIB_Div1Q_A32ls
MLIB_Div1Q_A32ss
MLIB_Div1Q_F16
MLIB_Div1Q_F16ll
MLIB_Div1Q_F16ls
MLIB_Div1Q_F32
MLIB_Div1Q_F32ls
MLIB_DivSat_A32as
MLIB_DivSat_F16
MLIB_DivSat_F16ll
MLIB_DivSat_F16ls
MLIB_DivSat_F32
MLIB_DivSat_F32ls
MLIB_Div_A32as
MLIB_Div_A32ll
MLIB_Div_A32ls
MLIB_Div_A32ss
MLIB_Div_F16
MLIB_Div_F16ll
MLIB_Div_F16ls
MLIB_Div_F32
MLIB_Div_F32ls
MLIB_Div_FLT
MLIB_Log2_U16
MLIB_Mac4RndSat_F16
MLIB_Mac4RndSat_F32
MLIB_Mac4Rnd_F16
MLIB_Mac4Rnd_F32
MLIB_Mac4Sat_F32ssss
MLIB_Mac4_F32ssss
```

```
MLIB_Mac4_FLT
MLIB_MacRndSat_F16
MLIB_MacRndSat_F32
MLIB_MacRndSat_F32lls
MLIB_MacRnd_A32ass
MLIB_MacRnd_F16
MLIB_MacRnd_F32
MLIB_MacRnd_F32lls
MLIB_MacSat_F16
MLIB_MacSat_F32
MLIB_MacSat_F32lss
MLIB_Mac_A32ass
MLIB_Mac_F16
MLIB_Mac_F32
MLIB_Mac_F32lss
MLIB_Mac_FLT
MLIB_MnacRndSat_F16
MLIB_MnacRndSat_F32
MLIB_MnacRndSat_F32lls
MLIB_MnacRnd_A32ass
MLIB_MnacRnd_F16
MLIB_MnacRnd_F32
MLIB_MnacRnd_F32lls
MLIB_MnacSat_F16
MLIB_MnacSat_F32
MLIB_MnacSat_F32lss
MLIB_Mnac_A32ass
MLIB_Mnac_F16
MLIB_Mnac_F32
MLIB_Mnac_F32lss
MLIB_Mnac_FLT
MLIB_Msu4RndSat_F16
MLIB_Msu4RndSat_F32
MLIB_Msu4Rnd_F16
MLIB_Msu4Rnd_F32
MLIB_Msu4Sat_F32ssss
MLIB_Msu4_F32ssss
MLIB_Msu4_FLT
MLIB_MsuRndSat_F16
MLIB_MsuRndSat_F32
MLIB_MsuRndSat_F32lls
MLIB_MsuRnd_A32ass
MLIB_MsuRnd_F16
MLIB_MsuRnd_F32
MLIB_MsuRnd_F32lls
MLIB_MsuSat_F16
MLIB_MsuSat_F32
MLIB_MsuSat_F32lss
MLIB_Msu_A32ass
MLIB_Msu_F16
MLIB_Msu_F32
MLIB_Msu_F32lss
MLIB_Msu_FLT
MLIB_MulNegRndSat_A32
MLIB_MulNegRndSat_F16as
MLIB_MulNegRnd_A32
MLIB_MulNegRnd_F16
MLIB_MulNegRnd_F16as
MLIB_MulNegRnd_F32
MLIB_MulNegRnd_F32ls
```

```
MLIB_MulNegSat_A32
MLIB_MulNegSat_F16as
MLIB_MulNeg_A32
MLIB_MulNeg_F16
MLIB_MulNeg_F16as
MLIB_MulNeg_F32
MLIB_MulNeg_F32ss
MLIB_MulNeg_FLT
MLIB_MulRndSat_A32
MLIB_MulRndSat_F16
MLIB_MulRndSat_F16as
MLIB_MulRndSat_F32
MLIB_MulRndSat_F32ls
MLIB_MulRnd_A32
MLIB_MulRnd_F16
MLIB_MulRnd_F16as
MLIB_MulRnd_F32
MLIB_MulRnd_F32ls
MLIB_MulSat_A32
MLIB_MulSat_F16
MLIB_MulSat_F16as
MLIB_MulSat_F32
MLIB_MulSat_F32ss
MLIB_Mul_A32
MLIB_Mul_F16
MLIB_Mul_F16as
MLIB_Mul_F32
MLIB_Mul_F32ss
MLIB_Mul_FLT
MLIB_NegSat_F16
MLIB_NegSat_F32
MLIB_Neg_F16
MLIB_Neg_F32
MLIB_Neg_FLT
MLIB_Rcp1Q1_A32s
MLIB_Rcp1Q_A32s
MLIB_Rcp1_A32s
MLIB_Rcp_A32s
MLIB_RndSat_F16l
MLIB_Rnd_F16l
MLIB_Sat_F16a
MLIB_Sh1LSat_F16
MLIB_Sh1LSat_F32
MLIB_Sh1L_F16
MLIB_Sh1L_F32
MLIB_Sh1R_F16
MLIB_Sh1R_F32
MLIB_ShLBiSat_F16
MLIB_ShLBiSat_F32
MLIB_ShLBi_F16
MLIB_ShLBi_F32
MLIB_ShLSat_F16
MLIB_ShLSat_F32
MLIB_ShL_F16
MLIB_ShL_F32
MLIB_ShRBiSat_F16
MLIB_ShRBiSat_F32
MLIB_ShRBi_F16
MLIB_ShRBi_F32
MLIB_ShR_F16
```

```
MLIB_ShR_F32
MLIB_Sign_F16
MLIB_Sign_F32
MLIB_Sign_FLT
MLIB_Sub4Sat_F16
MLIB_Sub4Sat_F32
MLIB_Sub4_F16
MLIB_Sub4_F32
MLIB_Sub4_FLT
MLIB_SubSat_F16
MLIB_SubSat_F32
MLIB_Sub_A32as
MLIB_Sub_A32ss
MLIB_Sub_F16
MLIB_Sub_F32
MLIB_Sub_FLT
PCLIB_Ctrl2P2ZInit_F16
PCLIB_Ctrl2P2Z_F16
PCLIB_Ctrl3P3ZInit_F16
PCLIB_Ctrl3P3Z_F16
PCLIB_CtrlPIDInit_F16
PCLIB_CtrlPID_F16
PCLIB_CtrlPIInit_F16
PCLIB_CtrlPI_F16
PCLIB_CtrlPIandLPInit_F16
PCLIB_CtrlPIandLP_F16
```

This is the list of algorithms for the DSP56800EF core with the CORDIC peripheral module:

```
GFLIB_CosCORDIC_F16
GFLIB_SinCORDIC_F16
GFLIB_SqrtCORDIC_F16
GFLIB_SqrtCORDIC_F16l
GFLIB_AtanCORDIC_F16
GFLIB_AtanYX_F16
```

# 4 Revision history

**Table 1. Revision history**

| Revision number | Date | Substantive changes |
|---|---|---|
| 0 | 17 January 2023 | Initial release |

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