Freescale Semiconductor
Addendum

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Errata to MPC8569E PowerQUICC III Integrated Processor Reference Manual, Rev. 2

This errata describes corrections to the *MPC8569E PowerQUICC III Integrated Processor Reference Manual*, Revision 2. For convenience, the section number and page number of the errata item in the reference manual are provided. Items in bold are new since the last revision of this document.

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Section, Page No.	Changes
1.4.9, 1-12	In Section 1.4.9, “Enhanced Secure Digital Host Controller (eSDHC)”, remove “SDIO” reference from the first paragraph. The updated paragraph reads as follows: “The enhanced secure digital host controller (eSDHC) provides an interface between the host system and SD/MMC cards. The eSDHC acts as a bridge, passing host bus transactions to SD/MMC cards by sending commands and performing data accesses to or from the cards. It handles SD/MMC protocols at the transmission level.”
4.5, 4-28	In Section 4.5, “Initialization/Applications Information”, update the third sentence from: “Two different configurations are provided for boot from the on-chip ROM: boot from eSPI and boot from eSDHC.” to: “The only configuration provided for boot from the on-chip ROM is through eSDHC.”
4.5.1.1, 4-29	In Section 4.5.1.1, “Overview”, remove occurrence of “SDIO” from the second row of the first paragraph. The updated row reads as follows: “This device can be either a SD card or MMC card, or other variants compatible with these devices.”
4.5.2, 4-37	In Section 4.5.2, “Default e500 Addressing During System Boot”, update the first sentence from: “During boot from the on-chip ROM (for boot targets of either eSPI or SD/MMC), the user specifies 32-bit addresses for several fields (Target Address for copying the user’s code, and the Execution Starting Address).” to: “During boot from the on-chip ROM (for boot target of SD/MMC), the user specifies 32-bit addresses for several fields (Target Address for copying the user’s code, and the Execution Starting Address).”
8.3.2.1, 8-9	In Table 8-3, “Memory Interface Signals—Detailed Signal Descriptions”, update the cross-reference to point towards Section 8.4.1.36, “DDR Control Driver Register 1 (DDRCDR_1)” for the D*n*_MDIC[0:1] signal. The updated signal description reads as follows:

Table 8-3. Memory Interface Signals—Detailed Signal Descriptions

Signal	I/O	Description	
D*n*_MDIC[0:1]	I/O	Driver impedance calibration. Note that the MDIC signals require the use of resistors; MDIC0 must be pulled to GND, while MDIC1 must be pulled to GVDD. See Section 8.4.1.36, “DDR Control Driver Register 1 (DDRCDR_1),” for more information on these signals.	
		State Meaning	These pins are used for automatic calibration of the DDR IOs.
		Timing	These are driven for four DRAM cycles at a time while the DDR controller is executing the automatic driver compensation.

Section, Page No.	Changes

8.4.1.21, 8-42

In Figure 8-22, “DDR Write Leveling Control Register (DDR_WRLVL_CNTL)”, update the bit range for WRLVL_START from 27–31 to 28–31. The updated figure is shown below:

Offset 0x174 Access: Read/Write

	0	1	4	5 7	8	9 11	12	13 15	16 19	20	21 23	24 27	28 31
R W	WRLVL_EN	—		WRLVL_MRD	—	WRLVL_ODTEN	—	WRLVL_DQSEN	WRLVL_SMPL	—	WRLVL_WLR	—	WRLVL-START
Reset	All zeros												

Figure 8-22. DDR Write Leveling Control Register (DDR_WRLVL_CNTL)

In addition, for Table 8-27, “DDR_WRLVL_CNTL Field Descriptions”, update the bit range for Reserved from “24–28” to “24–27” and WRLVL_START bit range from “27–31” to “28–31”.

8.4.1.38, 8-63

In Table 8-44, “CAPTURE_ECC Field Descriptions”, update the description for ECE bit (bits 16–31) for 24:31. The updated description reads as follows:

Table 8-44. CAPTURE_ECC Field Descriptions

Bits	Name	Description
16–31	ECE	Error capture ECC. Captures the ECC bits on the data path whenever errors are detected. 16:23—8-bit ECC for the 32 bits in beats 0, 2, 4 and 6 in 32-bit bus mode; should be ignored for 64-bit bus mode 24:31— 8-bit ECC for the 32 bits in beats 1, 3, 5, and 7 in 32-bit bus mode; should be used for every beat in 64-bit bus mode

8.5, 8-69

In Section 8.5, “Functional Description”, update the third sentence of the fourth paragraph from:

“Using ECC, the DDR memory controller detects and corrects all single-bit errors within the 64- or 32-bit data bus, detects all double-bit errors within the 64- or 32-bit data bus, and detects all errors within a nibble.”

to:

“Using ECC, the DDR memory controller detects and corrects all single/double-bit errors within the data bus, and detects all errors within a nibble.”

8.5.7, 8-86

In Section 8.5.7, “DDR SDRAM Refresh”, remove the last sentence “To ensure that the latency caused ... requied by the SDRAM” from the first paragraph.

8.6.1, 8-100

In Table 8-70, “Programming Differences Between Memory Types”, update the Difference column for ODT_CFG from “LPDDR” to “DDR3”. The updated row reads as follows:

Table 8-70. Programming Differences Between Memory Types

Parameter	Description	Differences		Section/page
ODT_CFG	ODT Configuration	DDR3	Should be set to 00	8.4.1.9/8-27
		DDR2	Can be set for termination at the IOs according to system topology. Typically, if ODT is enabled, then the internal IOs should be set up for termination only during reads to DRAM.	

12.6.4.4.1, 12-92 In Table 12-38, “RAM Word Field Descriptions”, add the following note for the LAST bit (bit 31):

“UPM continue to execute RAM words until it finds LAST, irrespective of the assigned region for various patterns like RSS.”

13.7, 13-45 Replace Table 13-28, “MPC8569E DMA Paths”, with the following table:

Table 13-28. MPC8569E DMA Paths

DMA Controllers		On-Chip Targets			Off-Chip Targets				
		L2	Configuration Registers	QE	DDR	Local Bus	DUART FIFO	Serial RapidIO	PCI Express
On-chip	**eSDHC**	Y	NS	Y	Y	Y	Y	Y	Y
	4 Channel	Y	NR	Y	Y	Y	Y	Y	Y
	QE	Y	NS	Y	Y	Y	NS	Y	Y
Off-chip	**Serial RapidIO**	Y	Y	Y	Y	Y	Y	—	Y
	PCI Express	Y	Y	Y	Y	Y	Y	Y	—

Note: On-chip target configuration registers include I^2C data register.

Note: On-chip 4-channel controller can serve external masters.

Note: QE DMA can be utilized only through micro code packages.

15.5.1.17, 15-36 In Table 15-26, “PCI Express Error Capture Status Register Field Descriptions”, update bit range for GSID bit from “23–30” to “26–30”.

16.6.2.2, 16-46 In Figure 16-26, “Flow Chart for Reset of eSDHC”, update the caption to “Flow Chart for Reset of eSDHC” and replace with the following figure:

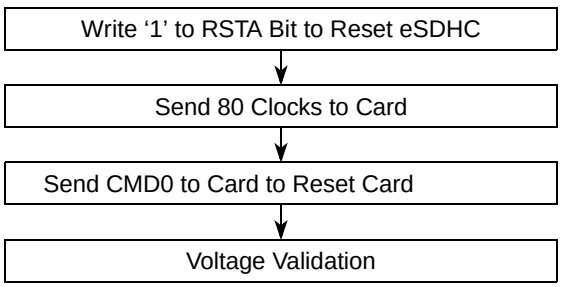

Figure 16-26. Flow Chart for Reset of eSDHC

In addition, replace the pseudocode with the following:

```
        software_reset()
{
        Configure the I/O muxes to select SD signals;
        set_bit(SYSCTL, RSTA);              // software reset the host
        set SYSCTL[DTOCV and SDCLKFS];      // get the SDHC_CLK of frequency around 400 kHz
        poll PRSSTAT[CIHB and CDIHB];       // wait until both bits are cleared
        set_bit(SYSCTRL, INTIA);            // send 80 clock ticks for card to power-up
        If the card is SD/MMC
              send_command(CMD_GO_IDLE_STATE, <other parameters>);// reset the card with CMD0
}
```

16.6.5, 16-55 In Table 16-27, “Commands for MMC/SD”, add the following row for CMD8 for SD card immediately below the row for CMD7:

Table 16-27. Commands for MMC/SD

CMD INDEX	Type	Argument	Resp	Abbreviation	Description
CMD8	bcr	[31:12] reserved bits [11:8] supply voltage(VHS) [7:0] check pattern	R7	SEND_IF_COND	Sends SD Memory Card interface condition, which includes host supply voltage information and asks the card whether card supports voltage. Reserved bits shall be set to ’0’.

In addition, for Table 16-27, “Commands for MMC/SD”, add the following note immediately after the note “Command SWITCH is for high-speed MMC cards...” and below Table 16-28, “EXT_CSD Access Modes”. The added note is shown below:

- CMD8 differs for MMC and SD cards. For SD cards, CMD8 is referred to as SEND_IF_COND. For MMC cards, CMD8 is referred to as SEND_EXT_CSD.

17.7.7.7, 17-156 In Table 17-72, “PKEU Interrupt Status Register Field Descriptions”, update the bounds of KSE (bit 54) from 1–256 to 1–512 and the bounds of DSE (bit 55) from 97–4096 to 33–4096. The updated rows reads as follows:

Table 17-72. PKEU Interrupt Status Register Field Descriptions

Bits	Name	Description
54	KSE	Key size error. Value outside the bounds of 1–512 bytes was written to the PKEU key size register 0 No error detected 1 Key size error detected
55	DSE	Data size error. Value outside the bounds 33– 4096 bits was written to the PKEU data size register 0 No error detected 1 Data size error detected

18.4.1.1, 18-7 In Table 18-3, “PORPLLSR Field Descriptions”, update the bit settings from “00110 12:1” to “01100 12:1” and from “00111 Synchronous mode” to “00110

Synchronous mode” for DDR_Ratio (bits 18–22). The updated description reads as follows:

Table 18-3. PORPLLSR Field Descriptions

Bits	Name	Description
18–22	DDR_Ratio	Establish the clock ratio between the DDR3 data rate and SYSCLK. The values correspond to the values on cfg_ddr_pll[0:2] at the negation of HRESET. Patterns not shown are reserved. 00011 3:1 00100 4:1 00101 5:1 00110 6:1 01000 8:1 01010 10:1 01100 12:1 00110 Synchronous mode

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