Errata to the MPC8540 PowerQUICC III™ Integrated Host Processor Reference Manual

This errata describes corrections to the *MPC8540 PowerQUICC III™ Integrated Host Processor Reference Manual, Rev. 1*. For convenience, the section number and page number of the errata item in the reference manual are provided.

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1 Document Errata

Section, Page	Changes
1.4.1, 1-21	In the last sentence of the first paragraph, replace ‘symmetric multiprocessing (SMP)’ with ‘distributed processing’.
1.4.1, 1-22	In Figure 1-3, change the title from “High-Performance Communication System Using Distributed Processing” to “High-Performance Communication System Using SMP”.
2.3.1, 2-11	Insert the following new Section 2.3.1 and, subsequently, renumber existing sections.

2.3.1 Accessing CCSR Memory from the e500 Core

When the local e500 processor is used to configure CCSR space, the CCSR memory space should typically be marked as Cache-Inhibited and Guarded.

In addition, many configuration registers affect accesses to other memory regions; therefore, writes to these registers must be guaranteed to have taken effect before accesses are made to the associated memory regions.

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	To guarantee that the results of any sequence of writes to configuration registers are in effect, the final configuration register write should be chased by a read of the same register, and that should be followed by a SYNC instruction. Then, accesses can safely be made to memory regions affected by the configuration register write.
4.4.2, 4-10	Correct the first sentence of the note associated with sequence step four to read as follows: "If the JTAG signals are not used, $\overline{\text{TRST}}$ may be tied active; however, it is recommended that $\overline{\text{TRST}}$ not remain asserted after negation of $\overline{\text{HREST}}$."
4.4.3, 4-11	Replace the second paragraph with the following: "All POR configuration signals have internal pull-up resistors so that if the desired setting is high, there is no need for a pull-up resistor on the board."
5.6, 5-19	In Figure 5-6, remove DVC1 and DVC2 registers.
6.1.1, 6-2	In Figure 6-1, remove DVC1 and DVC2 registers.
13.1.2, 13-2	Correct the first sub-bullet under primary bullet "Memory controller with eight memory banks" to read as follows: "— 32-bit address decoding with mask"
13.3.1.2.1, 13-13	Correct the first two sentences of the first paragraph to read as follows: "The address mask field of the option registers (OR*n*[AM]) mask up to 17 corresponding BR*n*[BA] fields. The 15 lsbs of the 32-bit internal address do not participate in bank address matching in selecting a bank for access."
13.3.1.2.1, 13-13	Remove the left-most column of Table 13-5.
13.3.1.13, 13-29	In Figure 13-16 and Table 13-19, remove register field LTEATR[XA] and change bits 28-29 to be 'Reserved'.
13.3.1.14, 13-30	In Table 13-20, correct the LTEAR[A] field description to read as follows: "Transaction address for the error. Holds the 32-bit address of the transaction resulting in an error."
13.4, 13-34	In Figure 13-20, correct the label for the arrow in the upper left corner to read "32-bit System Address".
13.4.1.1, 13-34	Correct the third sentence of the first paragraph to read as follows: "Addresses are decoded by comparing the 17 msbs of the address, masked by OR*n*[AM], with the base address for each bank (BR*n*[BA])."
13.4.1.7, 13-37	Replace the last sentence of the first paragraph with the following: "Setting LTEDR[BMD] disables bus monitor error checking (i.e. the LTESR[BM] bit is not set by a bus monitor time-out); however, the bus monitor is still active and can generate a UPM exception (as noted in Section 13.4.4.1.4, "Exception Requests") or terminate a GPCM access."

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13.4.2.4, 13-51	In Table 13-27, remove fields BR0[XBA] and OR0[XAM].
13.4.4.2, 13-66	Remove the third paragraph, beginning with “Note that the UPM memory region...”. Also, add the following note to the end of this section:

NOTE

In order to enforce proper ordering between updates to the MxMR register and the dummy accesses to the UPM memory region, two rules must be followed:

1. Since the result of any update to the MxMR register must be in effect before the dummy read or write to the UPM region, a write to MxMR should be followed immediately by a read of MxMR.

2. The UPM memory region should have the same MMU settings as the memory region containing the MxMR configuration register; both should be mapped by the MMU as Cache-Inhibited and Guarded. This prevents the e500 core from re-ordering a read of the UPM memory around the read of MxMR. Once the programming of the UPM array is complete, the MMU setting for the associated address range can be set to the proper mode for normal operation, such as cacheable and copyback.

13.5.4.3.3, 13-95	In Table 13-39, remove fields BR*n*[XBA] and OR*n*[XAM].
13.5.4.3.5, 13-96	In Table 13-43, remove fields BR*n*[XBA] and OR*n*[XAM].
14.2, 14-7	Change the fifth element of the second bullet item in the TSEC features list to read: “— 10/100 Mbps RGMII”
14.5.3.9.1, 14-89	In Table 14-96, correct ATTR[ELCWT] and ATTR[BDLWT] field values of 11 to be ‘Reserved’.
14.5.4.2, 14-92	In Figure 14-100 and Table 14-99, correct default reset values of control register fields AN Enable, Full Duplex, and Speed_1 to all be zero.
14.5.4.6, 14-98	In Figure 14-104, correct the reset value of the TBI ANEX register to be 0000_0000_0000_0100.
16.4.2.11.3, 16-74	Replace the second to the last sentence of the first paragraph with the following: “When the MPC8540 is in agent lock mode, it retries all externally-generated PCI/X configuration cycles until the ACL bit in the PCI bus function register (0x44) is cleared.”
16.4.2.11.4, 16-75	In Table 16-55, correct the table heading from “AD*n* Used in IIDSEL” to “AD*n* Used in IDSEL”.

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16.4.2.11.4, 16-75	In Table 16-55, separate entries for device number 0 and devices 1-9. Also, add the following table footnote related to IDSEL used for device number 0: "[1] No external configuration transaction takes place; rather, internal registers are accessed." In addition, insert the following table footnote related to IDSEL used for device numbers 1-9: "[2] No IDSEL line asserted. Type0 configuration transaction is run, but ends with a master abort since no device responds." Finally, renumber previous footnote accordingly.
16.5.1.3, 16-100	Insert the following sentence after the first sentence: "The purpose of this mode is to allow initial configuration on the post by the local processor before opening the port to be further configured by the external host."
17.3.2.2.3, 17-40	In Table 17-37, add the following note to the ROWAR*n*[WRTYP] field description: "**Note:** A sub-eight byte transaction that maps to an SWRITE is converted to an NWRITE. SWRITE requires the write size to be a multiple of 8 bytes."
18.4.1.11, 18-13	In Figure 18-11 and Table 18-14, correctly document bitfield 11 as 'Reserved'.
18.4.1.11, 18-14	In Table 18-14, correct the last sentence of the asserted state description for bitfield DEVDISR[E500] to read as follows: "Instruction fetching is stopped, snooping is disabled, and clocks are shut down to all functional units of the core, including the timer facilities."
18.5.1.7, 18-26	In Figure 18-20, correct the input of the NOR gate which drives internal signal core_tben, formerly noted as being driven by 'DEVDISR[TB]', to be noted as being driven by 'DEVDISR[TB] or [E500]'.
19.4.7, 19-23	In Table 19-10, insert a centered header row labeled "TSEC1 DMA Events" directly between rows for events "Receive FIFO above 3/4" and "DMA reads".
21.5.3.8.1, 21-47	In Table 21-39, correct ATTR[BDLWT] and ATTR[ELCWT] field values of 11 to be 'Reserved'.

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