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Addendum

Document Number: MPC8315ERMAD
Rev. 2.1, 09/2010

Errata to MPC8315E PowerQUICC II Pro Integrated Host Processor Family Reference Manual, Rev. 2

This errata describes corrections to the *MPC8315E PowerQUICC II Pro Integrated Host Processor Family Reference Manual*, Revision 2. For convenience, the section number and page number of the errata item in the reference manual are provided. Items in bold are new since the last revision of this document.

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Section, Page No.	Changes
4.5.2.1, 4-39	In Figure 4-13, “System PLL Mode Register,” add SVCOD field (bits 2–3) to show as follows:

Address 0x0_0A00 Access: Read only

	0	1	2 3	4 7	8	9 15	16 31
R	LBCM	DDRCM	SVCOD	SPMF	CKID	COREPLL	—
W							
Reset	*n*	*n*	*n* *n*	*n* *n* *n* *n*	*n*	*n* *n* *n* *n* *n* *n* *n*	*n* *n* *n* *n* *n* *n* *n* *n* *n* *n* *n* *n* *n* *n* *n* *n*[1]

Figure 4-13. System PLL Mode Register

1 See Table 4-35 for reset values.

In addition, add SVCOD field (bits 2–3)in Table 4-35, “System PLL Mode Register Bit Settings” to read as follows:

2–3	SVCOD	System PLL VCO division	Section 4.3.2.1.1, “System PLL VCO Division”

4.5.2.3, 4-41	Modify the first sentence of the ENCCM (bits 6–7) bit field description in Table 4-37, “SCCR Bit Descriptions” to say as follows: “Encryption core, JTAG, and I^{2}C clock mode.”

9.1, 9-2 Update Figure 9-1, “DDR Memory Controller Simplified Block Diagram,” to show as follows:

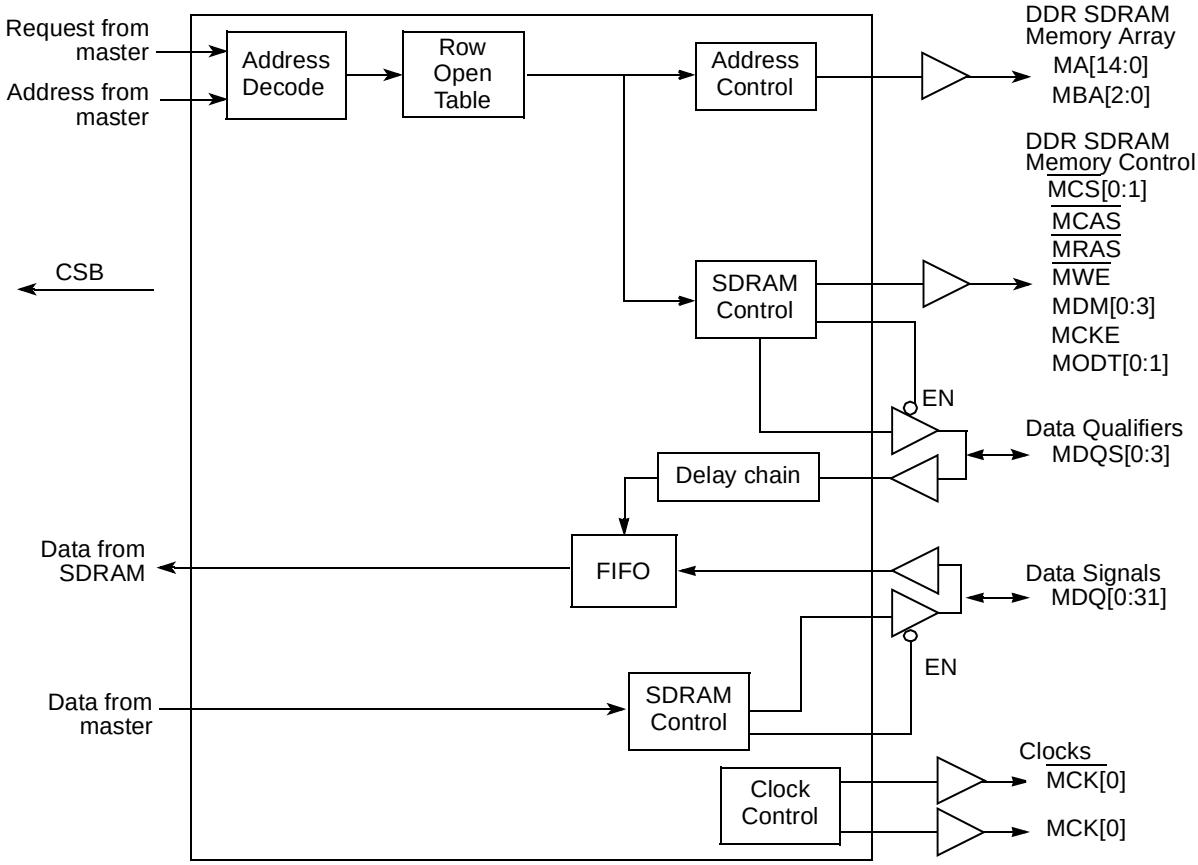

Figure 9-1. DDR Memory Controller Simplified Block Diagram

9.4.1.7, 9-18 In Figure 9-8, “DDR SDRAM Control Configuration Register (DDR_SDRAM_CFG),” make bits 11–12 as “DBW” to show as follows:

Offset 0x110 Access: Read/Write

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	MEM_EN	SREN	—	RD_EN	—	SDRAM_TYPE			—		DYN_PWR	DBW		8_BE	NCAP	—
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	2T_EN	BA_INTLV_CTL							—			PCHB8	HSE	—	MEM_HALT	BI
Reset	All zeros															

Figure 9-8. DDR SDRAM Control Configuration Register (DDR_SDRAM_CFG)

In addition, modify the following rows in Table 9-12, “DDR_SDRAM_CFG Field Descriptions,” to read as follows:

Bits	Name	Description
11–12	DBW	DRAM data bus width. 00 Reserved 01 32-bit bus is used 10 16-bit bus is used 11 Reserved
13	8_BE	8-beat burst enable. 0 4-beat bursts are used on the DRAM interface. 1 8-beat bursts are used on the DRAM interface. **Note:** In 32-bit or 16-bit mode, DDR1(SDRAM_TYPE=010) needs to be in 8-beat mode, and DDR2 (SDRAM_TYPE=011) needs to be in 4 beat mode.
27	PCHB8	Precharge bit 8 enable. 0 MA[10] is used to indicate the auto-precharge and precharge all commands. 1 Reserved

9.5, 9-32 Modify Figure 9-22, “DDR Memory Controller Block Diagram,” to show as follows:

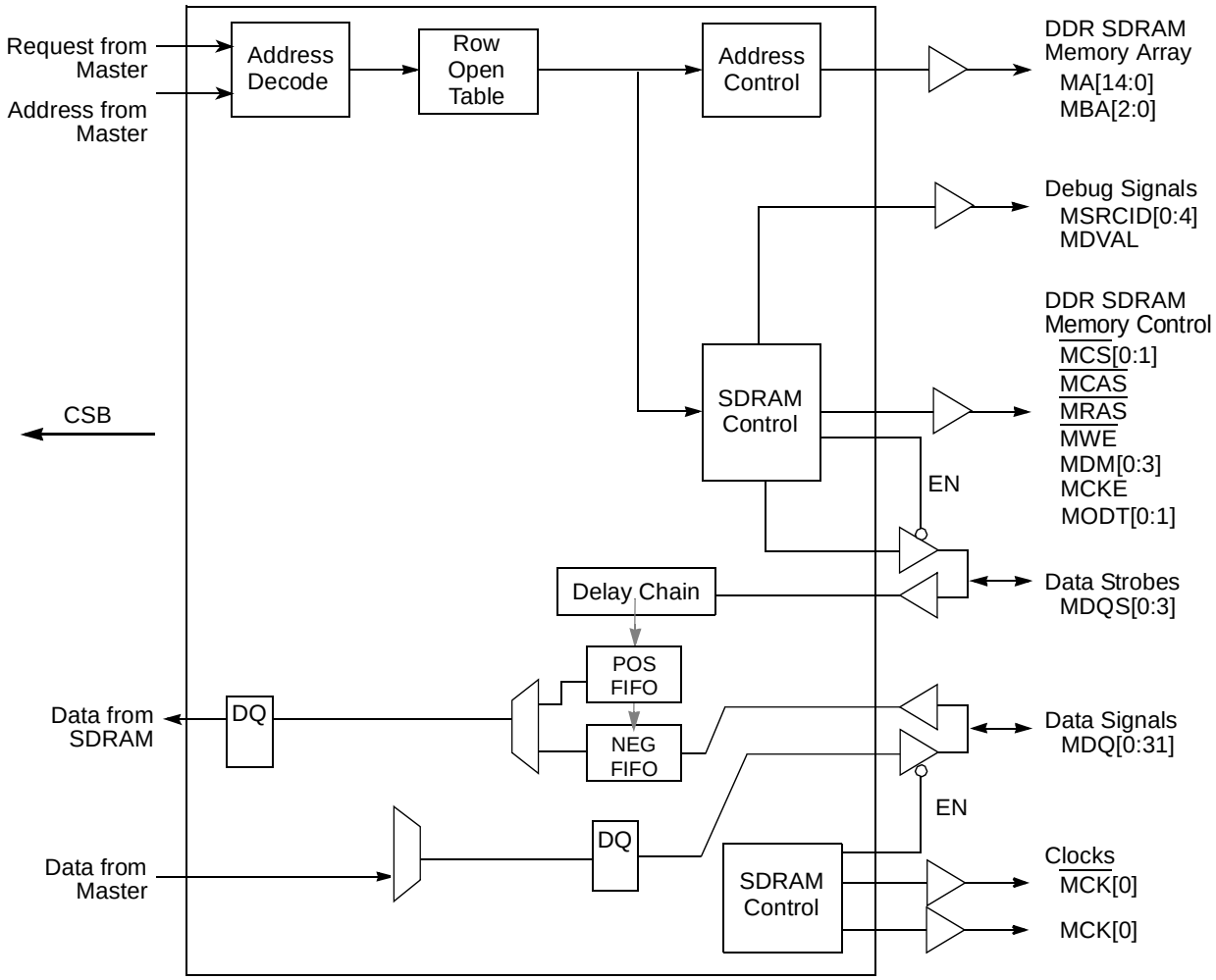

Figure 9-22. DDR Memory Controller Block Diagram

9.6, 9-53 In Table 9-39, “Memory Interface Configuration Register Initialization Parameters,” remove reference to x32_EN and 32_BE to read as follows. Note that only affected row is shown.

Name	Description	Parameter		Section/page
DDR_SDRAM_CFG	Control configuration	SREN RD_EN SDRAM_TYPE DYN_PWR 8_BE DBW	NCAP 2T_EN BA_INTLV_CTL HSE BI	9.4.1.7/9-18

Section, Page No.	Changes
10.3.1.9, 10-25	Add the following sentence to the end of first paragraph and prior to Figure 10-13, “Transfer Error Status Register (LTESR)”: “Note that error statuses are only reflected in LTESR if they have been enabled in LTEDR.”
10.3.1.10, 10-27	Modify the first sentence to say read as follows: “The transfer error check disable register (LTEDR), shown in Figure 10-14, is used to disable error/event checking, which are reported in LTESR.”
17.2, 17-3	Remove Table 17-1, “USB External Signals.” Note that the subsequent tables are re-numbered.
17.3, 17-7	In Table 17-4, “USB Interface Memory Map,” change the reset values of the following registers. Note that only affected registers are shown below.

Offset	Register	Access	Reset	Section/Page
0x14C	FRINDEX—USB frame index	R/W	All zeros	17.3.2.4/17-19
0x154	PERIODICLISTBASE—Frame list base address	R/W	All zeros	17.3.2.6/17-20
0x1A4	OTGSC—On-The-Go status and control	Mixed	0x0000_1030	17.3.2.15/17-32

17.3.2.4, 17-19	In Figure 17-11, “USB Frame Index (FRINDEX),” change reset value from “0x0000_nnnn” to “All zeros”.
17.3.2.6, 17-21	In Figure 17-12, “Periodic Frame List Base Address (PERIODICLISTBASE),” change the reset values from “0xnnnn_0000” to “All zeros.”
17.3.2.14, 17-32	In Table 17-24, “PORTSC Register Field Descriptions,” modify the following sentence in CCS (bit 0) bit field description from: “A one indicates that the device successfully attached and is operating in either high-speed or full-speed as indicated by the High Speed Port bit in this register.” to “A one indicates that the device successfully attached and is operating in either high-speed or full-speed as indicated by the PSPD field in this register.”

17.3.2.15, 17-33 In Figure 17-21, “OTG Status Control (OTGSC),” change reset value to 0x0000_1030, and add the following corresponding footnote to show as follows:

Offset 0x1A4 Access: Mixed

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	—	DPIE	1msE	BSEIE	BSVIE	ASVIE	AVVIE	IDIE	—	DPIS	1msS	BSEIS	BSVIS	ASVIS	AVVIS	IDIS
W										w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	All zeros															

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	—	DPS	1msT	BSE	BSV	ASV	AVV	ID	—			DP	OT	—	VC	VD
W																
Reset	0	0	0	1	0	0	0	0	0	0	1	1	0	0	0	0[1]

Figure 17-21. OTG Status Control (OTGSC)

[1] Simulation reset value. The reset value of this register depends upon external conditions, such as ID value and VBUS presence.

17.3.2.16, 17-35 In Table 17-26, “USBMODE Register Field Descriptions,” modify the bit field description of CM (bit 1–0) as follows:

“Controller mode

This register can only be written once after reset. If it is necessary to switch modes, software must reset the controller by writing to USBCMD[RST] before reprogramming this register.

00 Idle (default).

01 Reserved, should be cleared.

10 Device controller.

11 Host controller.

Defaults to the idle state and needs to be initialized to the desired operating mode after reset.”

17.3.2.17, 17-36 In Figure 17-23, “Endpoint Setup Status (ENDPTSETUPSTAT),” make ENDPTSETUPSTAT bits (2–0) as “w1c” as per bit field description to show the figure as follows:

Offset 0x1AC Access: w1c

	31	3	2	0
R	—		ENDPTSETUPSTAT	
W			w1c	
Reset	All zeros			

Figure 17-23. Endpoint Setup Status (ENDPTSETUPSTAT)

17.3.2.26, 17-45 In Table 17-36, “PRI_CTRL Register Field Descriptions,” add the following to the bit field decriptions of pri_lvl1(bits 28–29) and pri_lvl0(bits 30–31):

“The highest priority is 2’h3 and the lowest priority is 2’b0.”

Section, Page No.	Changes
17.3.2.27, 17-46	In Table 17-37, “SI_CTRL Register Field Descriptions,” for “rd_prefetch_val” bit field description (bit 31) modify the sentence starting from “When this input is LOW....” to read as follows: “When this input is ZERO 64 bytes are fetched, and when it is ONE 32 bytes are fetched.”
17.5.1, 17-50	Remove the following sentence occuring after Figure 17-35, “Periodic Schedule Organization”: “Split transaction interrupt, bulk and control are also managed using queue heads and queue element transfer descriptors.” In addition, update the third paragraph starting from “The periodic frame list is...” to read as follows: “The periodic frame list is a 4K-page aligned array of Frame List Link pointers. The length of the frame list is programmable. The programmability of the periodic frame list is exported to system software through the HCCPARAMS register. The length can be selected by system software as one of 8, 16, 32, 64, 128, 256, 512 or 1024 elements. Programming the size (that is, the number of elements) is accomplished by system software writing the appropriate value into Frame List Size field in the USBCMD register.”
17.5.7, 17-69	Remove the sentence starting from “Software must not use the FSTN feature.....and their use may yield undefined results” in the first paragraph: Add the following note at the end of the section, after Figure 17-42, “Frame Span Traversal Node Structure”: **NOTE** The host controller performs only read operations to the FSTN data structure.
17.5.7.2, 17-70	In Table 17-64, “FSTN Back Path Link Pointer,” update the field description of bit 0 as follows: “Terminate. 0 Link pointer is valid (that is, the host controller may use bits 31–5 as a valid memory address). This value also indicates that this FSTN is a Save-Place indicator. 1 Link pointer field is not valid (that is, the host controller must not use bits 31–5 as a valid memory address). This value also indicates that this FSTN is a Restore indicator.”
17.6.1, 17-71	Remove the following sentence in the first paragraph: “After a hardware reset, only the operational registers are at their default values.”
17.6.2, 17-72	Add the following sentence at the end of the paragraph: “The Configured Flag and Port Power Control bits are always 1’b1 in Host Mode. The PPE always follows the state of Port Power (PP) bit that is, if PP is 0, PPE will be 0 and if PP is 1, PPE will be 1.

17.6.4.1, 17-74

In Table 17-65, “Behavior During Wake-Up Events,” modify the following bit names in “Port Status and Signaling Type” column:

WKDSCNNT_E –> PORTSC[WKDS]

WKCNNT_E –> PORTSC[WKCN]

WKOC_E –> PORTSC[WKOC]

to update the table as follows:

Port Status and Signaling Type	Signaled Port Response	Device State	
		D0	not D0
Port disabled, resume K-State received	No effect	N/A	N/A
Port suspended, Resume K-State received	Resume reflected downstream on signaled port. PORTSC[FPR] is set. USBSTS[PCI] is set.	[1], [2]	[2]
Port is enabled, disabled or suspended, and the port's PORTSC[WKDS] bit, is set. A disconnect is detected.	Depending on the initial port state, the PORTSC Connect (CCS) and Enable (PE) status bits are cleared, and the Connect Change status bit (CSC) is set. USBSTS[PCI] is set.	[1], [2]	[2]
Port is enabled, disabled or suspended, and the port's PORTSC[WKDS] bit, is cleared. A disconnect is detected.	Depending on the initial port state, the PORTSC Connect (CCS) and Enable (PE) status bits are cleared, and the Connect Change status bit (CSC) is set. USBSTS[PCI] is set.	[1], [3]	[3]
Port is not connected and the port's PORTSC[WKCN] bit is a one. A connect is detected.	PORTSC Connect Status (CCS) and Connect Status Change (CSC) bits are set. USBSTS[PCI] is set.	[1], [2]	[2]
Port is not connected and the port's PORTSC[WKCN] bit is a zero. A connect is detected.	PORTSC Connect Status (CCS) and Connect Status Change (CSC) bits are set. USBSTS[PCI] is set.	[1], [3]	[3]
Port is connected and the port's PORTSC[WKOC] bit is a one. An over-current condition occurs.	PORTSC Over-current Active (OCA), Over-current Change (OCC) bits are set. If Port Enable/Disable bit (PE) is a one, it is cleared. USBSTS[PCI] is set	[1], [2]	[2]
Port is connected and the port's PORTSC[WKOC] bit is a zero. An over-current condition occurs.	PORTSC Over-current Active (OCA), Over-current Change (OCC) bits are set. If Port Enable/Disable bit (PE) is a one, it is cleared. USBSTS[PCI] is set.	[1], [3]	[3]

[1] Hardware interrupt issued if USBINTR[PCE] (port change interrupt enable) is set.

[2] PME# asserted if enabled (Note: PME Status must always be set).

[3] PME# not asserted.

17.6.12.2.1, 17-98 In Figure 17-54, “General Structure of EHCI Periodic Schedule Utilizing Interrupt Spreading,” change the notations of the nodes to show as follows:

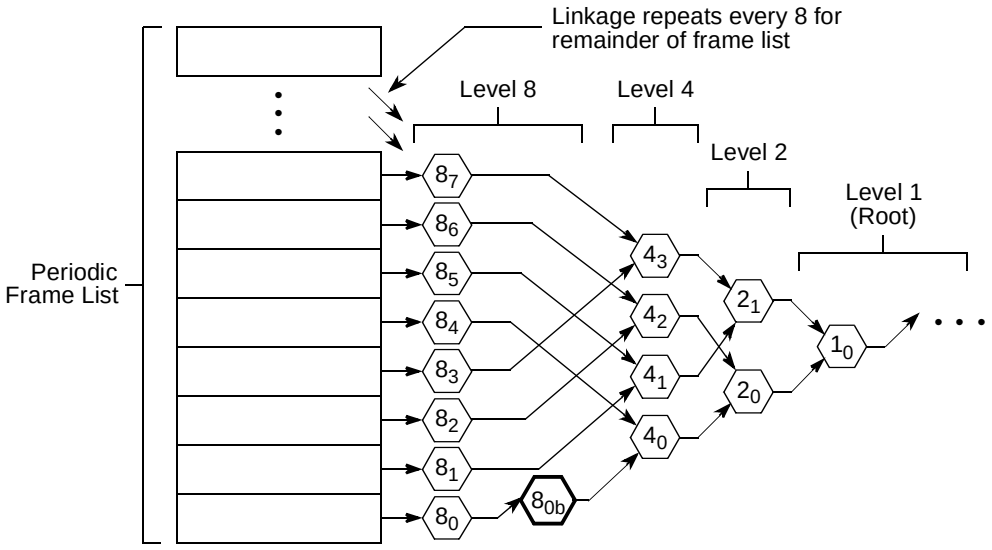

Figure 17-54. General Structure of EHCI Periodic Schedule Utilizing Interrupt Spreading

17.6.12.2.2, 17-100 In Figure 17-55, “Example Host Controller Traversal of Recovery Path via FSTNs,” change the notations of the nodes to show as follows:

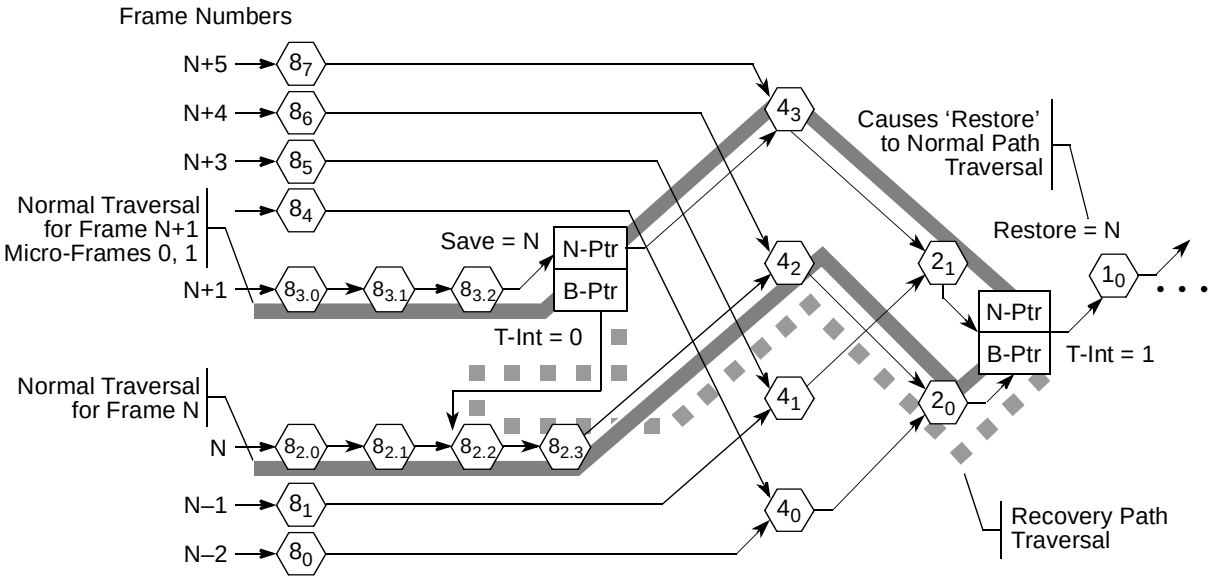

Figure 17-55. Example Host Controller Traversal of Recovery Path via FSTNs

17.6.12.2.5, 17-103 Modify Figure 17-56, “Split Transaction State Machine for Interrupt,” to show as follows:

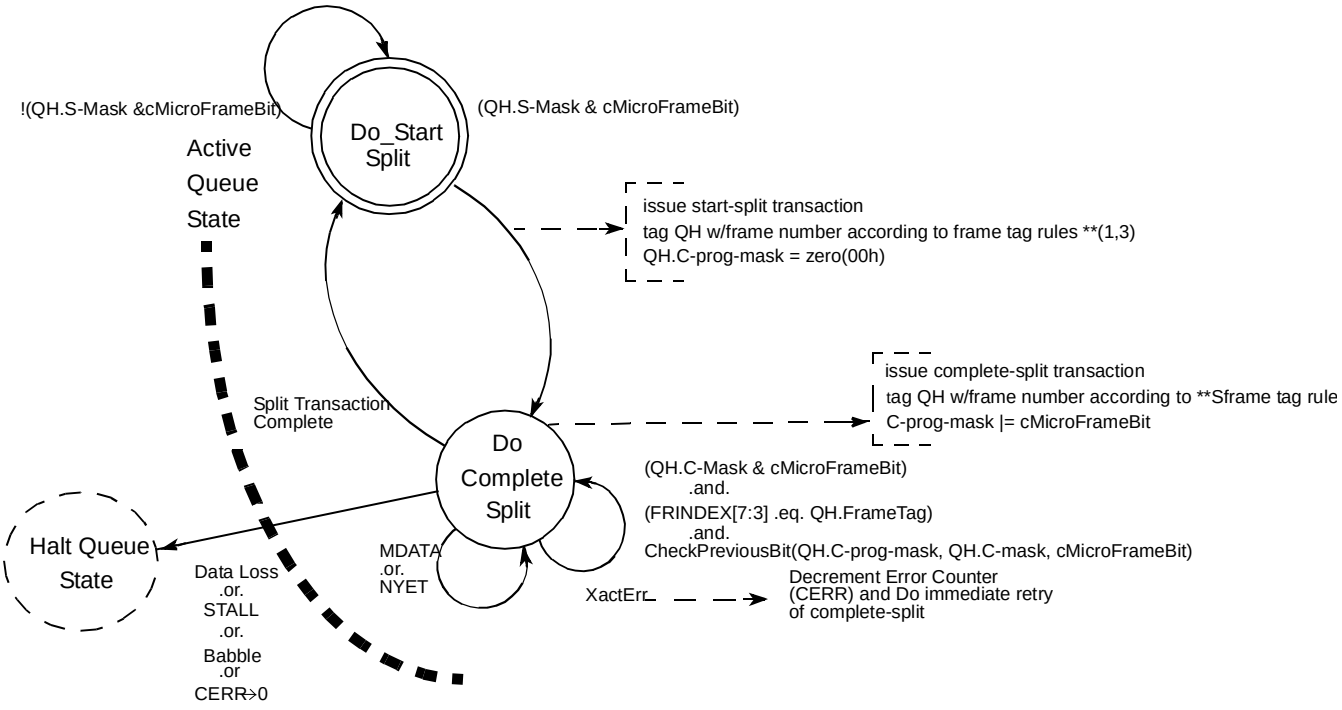

Figure 17-56. Split Transaction State Machine for Interrupt

17.6.12.3.3, 17-115 Modify Figure 17-59, “Split Transaction State Machine for Isochronous,” to show as follows:

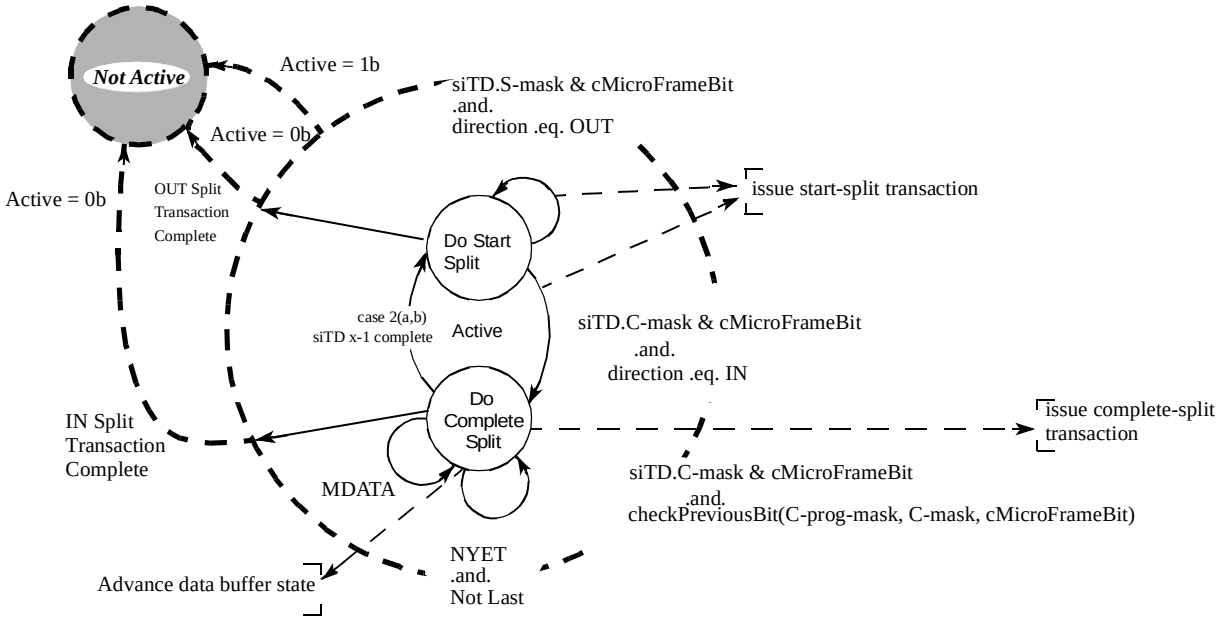

Figure 17-59. Split Transaction State Machine for Isochronous

17.8.3.2.2, 17-141 In the first sentence of the second paragraph change “data toggle” to say as “data toggle state bit” . The sentence now reads as:

“In normal operation, the USB_DR checks the DATA0/DATA1 bit against the data toggle state bit to determine if the packet is valid.”

17.8.3.3.1, 17-141 Modify the following sentence in the second paragraph from:

“This FIFO is split into virtual channels so that the leading data can be stored for any endpoint up to the maximum number of endpoints configured at device synthesis time.”

to:

“This FIFO is split into virtual channels so that the leading data can be stored for any endpoint.”

17.8.4, 17-149 In Figure 17-64, “Endpoint Queue Head Diagram,” replace “Up to 32 Elements” with “Up to 6 Elements” to show as follows:

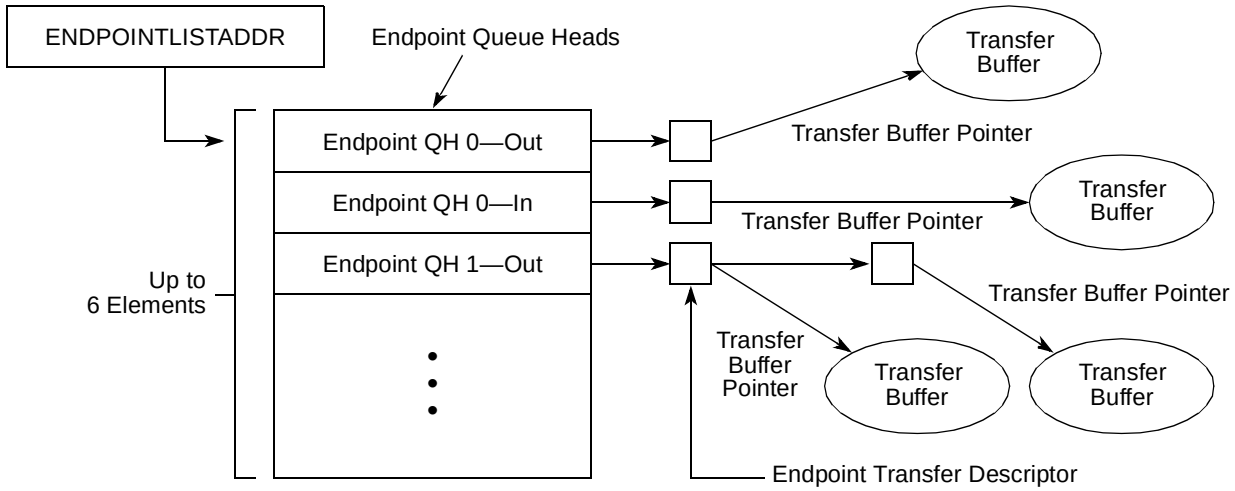

Figure 17-64. Endpoint Queue Head Diagram

17.8.5.3, 17-152 Replace the cases “Link list is empty” and “Link list is not empty” with the following:

Case 1: Link list is empty

1. Write dQH next pointer AND dQH terminate bit to ‘0’ as a single DWord operation.
2. Clear active and halt bit in dQH (in case set from a previous error).
3. Prime endpoint by writing ‘1’ to correct bit position in ENDPTPRIME.

Case 2: Link list is not empty

1. Add dTD to end of linked list.
2. Read correct prime bit in ENDPTPRIME—if ‘1’ DONE.
3. Set ATDTW bit in USBCMD register to ‘1’.
4. Read correct status bit in ENDPTSTATUS. (store in tmp. variable for later).
5. Read ATDTW bit in USBCMD register.

   If ‘0’ goto 3.

   If ‘1’ continue to 6.
6. Write ATDTW bit in USBCMD register to ‘0’.
7. If status bit read in (4) is ‘1’ DONE.
8. If status bit read in (4) is ‘0’ then Goto Case 1: Step 1.

17.9.5.1, 17-160 Modify the last sentence to read as follows:

“That is, 60-MHz transceiver clock for 8-bit physical interfaces and full-speed serial interfaces or 30-MHz transceiver clock.”

17.10, 17-162 Remove Section “Timing Diagrams.”

Section, Page No.	Changes
19.5.3.3.7, 19-57	In Table 19-33, “RQFCR Field Descriptions,” update the AND (bit 24) field description to read as follows: “AND, in combination with CLE, REJ, and PID match, determines whether the filer will accept or reject a frame, defer evaluation until the next rule, exit a cluster, or skip a rule or set of rules. If CLE is zero: 0 Match property[PID] against RQPROP. If matched, accept or reject frame based on REJ. Otherwise skip to next rule. 1 Match property[PID] against RQPROP. If matched, defer evaluation to next rule. Otherwise, skip all rules up to and including the next rule with AND = 0. If the next rule with AND = 0 has CLE = 1, then also exit cluster. If CLE is one: 0 Match property[PID] against RQPROP. If matched, accept or reject frame based on REJ. Otherwise, exit cluster. 1 Match property[PID] against RQPROP. If matched, enter cluster. Otherwise, skip all rules up to and including the next rule while CLE = 1 and AND = 0.”
19.5.3.3.8, 19-60	In Table 19-34, “RQFPR Field Descriptions,” append the following text to the TOS field description (PID = 1010, bits 24–31): “(Software should acknowledge the PIC=1 IP6 bit to distinguish proper alignment of the TOS field.)”

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Document Number: MPC8315ERMAD
Rev. 2.1
09/2010