Freescale Semiconductor
Addendum

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Rev. 1.2, 3/2008

Errata to MPC8240 Integrated Processor User's Manual, Rev. 1

This errata describes corrections to the *MPC8240 Integrated Processor User's Manual*, Revision 1. For convenience, the section number and page number of the errata item in the reference manual are provided. Items in bold are new since the last revision of this document.

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Section, Page No.	Changes

3.1, 3–2 — In Table 3-1, “Address Map B—Processor View in Host Mode,” the PCI address range for the processor address range 8000_0000 through FDFF–FFFF should read as follows:

8000_0000	FDFF_FFFF	2G	4G – 32M – 1	8000_0000–FDFF_FFFF	PCI memory space
—	—	—	—	—	—

4.8.2, 4-38 — Remove the unmarked figure that is above Table 4-33, “Bit Settings for Error Enabling Register 2 (ErrEnR2)—0xC4”) and below the introduction sentence for Table 4-33.

4.10, 4-43 — In Table 4-38, “Bit Settings for MCCR1—0xF0,” the description of bits 22–21 (DBUS_SIZ[0–1]), ‘For FPM/EDO systems only, (RAM_TYPE=1)’ should be on the same line with ‘0x 32-bit data bus.’ The description should read as follows:

22–21	DBUS_SIZ[0–1]	xx	Read-only. This field indicates the state of the ROM bank 0 data path width configuration signals [DL[0], $\overline{\text{FOE}}$] at reset as follows: For ROM/Flash chip select #0 ($\overline{\text{RCS0}}$): 00 32-bit data bus. x1 8-bit data bus. 10 64-bit data bus. For ROM/Flash chip select #1 ($\overline{\text{RCS1}}$) and (S)DRAM: 0x 32-bit data bus. For FPM/EDO systems only (RAM_TYPE=1). 1x 64-bit data bus.

4.10, 4–46 — In Table 4-40, “Bit Settings for MCCR3—0xF8,” replace the “Wait States for ROM High Impedance” table in the description for bits 31–29 with the following. Note the addition of rows for 011 and 110:

<table>
<tr><th>Bits</th><th>Name</th><th>Reset Value</th><th>Description</th></tr>
<tr><td>31–29</td><td>TS_WAIT_ TIMER[0–2]</td><td>000</td><td>Transaction start wait states timer. The minimum time allowed for ROM/Flash/Port X devices to enter high impedance is two memory system clocks. TS_WAIT_TIMER[0–2] adds wait states before the subsequent transaction starts in order to account for longer disable times of a ROM/Flash/Port X device. This delay is enforced after all ROM and Flash accesses, delaying the next memory access from starting (for example, DRAM after ROM access, SDRAM after Flash access, ROM after Flash access).
Note that this parameter is supported for SDRAM systems only. For EDO/FPM DRAM systems, TS_WAIT_TIMER[0–2] must = 000.

<table>
<tr><th rowspan="2">Bits</th><th colspan="3">Wait States for ROM High Impedance</th></tr>
<tr><th>Reads with Wide Data Path (32- or 64-Bit)</th><th>Reads with Gather Data Path in Flow-Through or Registered Buffer Mode (8-, 16-, 32-Bit)</th><th>All Writes [1, 2] and Reads with Gather Data Path in In-Line Buffer Mode (8-, 16-, 32-Bit</th></tr>
<tr><td>000</td><td>2 clocks</td><td>5 clocks</td><td>6 clocks</td></tr>
<tr><td>001</td><td>2 clocks</td><td>5 clocks</td><td>6 clocks</td></tr>
<tr><td>010</td><td>3 clocks</td><td>5 clocks</td><td>6 clocks</td></tr>
<tr><td>011</td><td>4 clocks</td><td>5 clocks</td><td>6 clocks</td></tr>
<tr><td>100</td><td>5 clocks</td><td>6 clocks</td><td>7 clocks</td></tr>
<tr><td>101</td><td>6 clocks</td><td>7 clocks</td><td>8 clocks</td></tr>
<tr><td>110</td><td>7 clocks</td><td>7 clocks</td><td>7 clocks</td></tr>
<tr><td>111</td><td>8 clocks</td><td>9 clocks</td><td>10 clocks</td></tr>
</table>
Notes:
1. In this context, Flash writes are defined as any write to $\overline{\text{RCS0}}$ or $\overline{\text{RCS1}}$.
2: For Flash writes, add the write recovery time, ROMNAL, to the given wait states for ROM high-impedance time.</td></tr>
</table>

5.4.2.3, 5-23 Replace information regarding AN1767 with AN2129, as follows: “*Instruction and Data Cache Locking on the e300 Processor Core* application note (order number: AN2129).”

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