Freescale Semiconductor
Reference Manual Addendum

MCF5485RMAD
Rev. 5, 4/2009

MCF5485 Reference Manual Errata

by: Microcontroller Solutions Group

This errata document describes corrections to the *MCF5485 Reference Manual*, order number MCF5485RM. For convenience, the addenda items are grouped by revision. Please check our website at http://www.freescale.com/coldfire for the latest updates.

The current version available of the *MCF5485 Reference Manual* is Revision 5.

Table of Contents

1 Errata for Revision 5

None to report.

2 Errata for Revision 4

Table 1. MCF5485RM Rev 4 Errata

<table>
<tr><th>Location</th><th>Description</th></tr>
<tr><td>Chapter 1</td><td>Corrected maximum frequency errors throughout. PCI: 50 MHz, FlexBus: 50 MHz, SDRAM: 100 and 200 MHz</td></tr>
<tr><td>Table 1-2/Page 1-7</td><td>Replace with the following table:
<table>
<tr><th>AD[12:8][1]</th><th>Clock Ratio</th><th>CLKIN–PCI and FlexBus Frequency Range (MHz)</th><th>Internal XLB, SDRAM bus, and PSTCLK Frequency Range (MHz)</th><th>Core Frequency Range (MHz)</th></tr>
<tr><td>00011</td><td>1:2</td><td>41.67–50.0</td><td>83.33–100</td><td>166.66–200</td></tr>
<tr><td>00101</td><td>1:2</td><td>25.0–41.67</td><td>50.0–83.33</td><td>100.0–166.66</td></tr>
<tr><td>01111</td><td>1:4</td><td>25.0</td><td>100</td><td>200</td></tr>
</table>
NOTES:
1 All other values of AD[12:8] are reserved.</td></tr>
<tr><td>Section 1.4.6.7/Page 1-10</td><td>Change last sentence to: “The two CAN controllers can interface to two separate 16 message buffer CAN networks or a single 32 message buffer CAN network.”</td></tr>
<tr><td>Table 2-1/Page 2-3</td><td>Remove extraneous overbars from the following signals: TSIZ1, TSIZ0
Add overbar to $\overline{\text{PCITRDY}}$.</td></tr>
<tr><td>Table 2-1/Page 2-6</td><td>E1MDIO entry: Remove ‘Y’ from pull-up column. This signal cannot be configured as a GPIO so there is no pull-up.
E1MDC entry: Remove ‘Y’ from pull-up column. This signal cannot be configured as a GPIO so there is no pull-up. Change I/O entry from “O:I/O” to “O”.</td></tr>
<tr><td>Table 2-2/Page 2-10</td><td>Remove extraneous overbars from the following pin/signals: A15/DSI, W23/DSPICS5, AA23/IVDD, AA25/PCS0TXD, AB26/PPSC1PSC02.
Add overbar to B13/$\overline{\text{RSTI}}$.</td></tr>
<tr><td>Table 2-4/Page 2-22</td><td>Replace with the following table:
<table>
<tr><th>AD[12:8][1]</th><th>Clock Ratio</th><th>CLKIN–PCI and FlexBus Frequency Range (MHz)</th><th>Internal XLB, SDRAM bus, and PSTCLK Frequency Range (MHz)</th><th>Core Frequency Range (MHz)</th></tr>
<tr><td>00011</td><td>1:2</td><td>41.67–50.0</td><td>83.33–100</td><td>166.66–200</td></tr>
<tr><td>00101</td><td>1:2</td><td>25.0–41.67</td><td>50.0–83.33</td><td>100.0–166.66</td></tr>
<tr><td>01111</td><td>1:4</td><td>25.0</td><td>100</td><td>200</td></tr>
</table>
NOTES:
1 All other values of AD[12:8] are reserved.</td></tr>
<tr><td>Table 2-7/Page 2-24</td><td>Swap the bit settings for AD3 in this table. When AD3 is asserted, $\overline{\text{BE}}$[3:0] are asserted for both read and write cycles. When negated, $\overline{\text{BE}}$[3:0] are asserted for write cycles only.</td></tr>
</table>

Table 1. MCF5485RM Rev 4 Errata (continued)

<table>
<tr><th>Location</th><th>Description</th></tr>
<tr><td>Section 2.2.8.2/Page 2-26</td><td>Change sentence from “This is the USB cable Vbus monitor input.“ to “This is the USB cable Vbus monitor input, which is 5 V tolerant.”</td></tr>
<tr><td>Section 7.13/Page 7-30</td><td>Change value written to D0 in first line of code from 0xA30C_8100 to 0xA70C_8100 to enable cache-inhibited, imprecise mode.</td></tr>
<tr><td>Table 10-1/Page 10-2</td><td>Replace with the following table:
<table>
<tr><th>AD[12:8][1]</th><th>Clock Ratio</th><th>CLKIN–PCI and FlexBus Frequency Range (MHz)</th><th>Internal XLB, SDRAM bus, and PSTCLK Frequency Range (MHz)</th><th>Core Frequency Range (MHz)</th></tr>
<tr><td>00011</td><td>1:2</td><td>41.67–50.0</td><td>83.33–100</td><td>166.66–200</td></tr>
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</table>
NOTES:
1 All other values of AD[12:8] are reserved.</td></tr>
<tr><td>Table 11-1/Page 11-2</td><td>Change GSRn’s Access entry to R/W as some status bits may be cleared by writing a 1 to them.</td></tr>
<tr><td>Figure 11-4/Page 11-7</td><td>Change GSRn[TEXP, PWMP, COMP, CAPT] bits’ write row to ‘w1c’ as they may be written with a 1 to clear them.</td></tr>
<tr><td>Table 12-1/Page 12-1</td><td>Change SSRn’s Access entry to R/W as some status bits may be cleared by writing a 1 to them.</td></tr>
<tr><td>Figure 12-4/Page 12-4</td><td>Change SSRn[BE, ST] bits’ write row to ‘w1c’ as they may be written with a 1 to clear them.</td></tr>
</table>

Table 1. MCF5485RM Rev 4 Errata (continued)

<table>
<tr><th>Location</th><th>Description</th></tr>
<tr><td>Table 13-1/Page 13-2</td><td>Replace table with the one below to better illustrate the interrupt priority and level assignments.
<table>
<tr><th>Interrupt Level
ICR[IL]</th><th>Priority

ICR[IP]</th><th>Supported Interrupt Sources</th></tr>
<tr><td rowspan="9">7</td><td>7</td><td rowspan="4">#8–63</td></tr>
<tr><td>6</td></tr>
<tr><td>5</td></tr>
<tr><td>4</td></tr>
<tr><td>— (Mid-point)</td><td>#7 (IRQ7)</td></tr>
<tr><td>3</td><td rowspan="4">#8–63</td></tr>
<tr><td>2</td></tr>
<tr><td>1</td></tr>
<tr><td>0</td></tr>
<tr><td rowspan="3">6</td><td>7–4</td><td>#8–63</td></tr>
<tr><td>— (Mid-point)</td><td>#6 (IRQ6)</td></tr>
<tr><td>3–0</td><td>#8–63</td></tr>
<tr><td rowspan="3">5</td><td>7–4</td><td>#8–63</td></tr>
<tr><td>— (Mid-point)</td><td>#5 (IRQ5)</td></tr>
<tr><td>3–0</td><td>#8–63</td></tr>
<tr><td rowspan="3">4</td><td>7–4</td><td>#8–63</td></tr>
<tr><td>— (Mid-point)</td><td>#4 (IRQ4)</td></tr>
<tr><td>3–0</td><td>#8–63</td></tr>
<tr><td rowspan="3">3</td><td>7–4</td><td>#8–63</td></tr>
<tr><td>— (Mid-point)</td><td>#3 (IRQ3)</td></tr>
<tr><td>3–0</td><td>#8–63</td></tr>
<tr><td rowspan="3">2</td><td>7–4</td><td>#8–63</td></tr>
<tr><td>— (Mid-point)</td><td>#2 (IRQ2)</td></tr>
<tr><td>3–0</td><td>#8–63</td></tr>
<tr><td rowspan="3">1</td><td>7–4</td><td>#8–63</td></tr>
<tr><td>— (Mid-point)</td><td>#1 (IRQ1)</td></tr>
<tr><td>3–0</td><td>#8–63</td></tr>
</table></td></tr>
<tr><td>Chapter 17</td><td>Change instances throughout of 4-1-1-1 to 3-1-1-1, 4-2-2-2 to 3-2-2-2, and 3-1-1-1 to 2-1-1-1.</td></tr>
<tr><td>Section 17.1.1/Page 17-1</td><td>Change FlexBus maximum operating frequency from 66 MHz to 50 MHz.</td></tr>
<tr><td>Figure 17-28/Page 17-28</td><td>Remove internal termination dashed lines for $\overline{\text{FBCS}}$, $\overline{\text{BE/BWE}}$, $\overline{\text{TBST}}$, and $\overline{\text{OE}}$ signals.</td></tr>
<tr><td>Figure 17-32/Page 17-30</td><td>Remove internal termination dashed lines for $\overline{\text{FBCS}}$, $\overline{\text{BE/BWE}}$, $\overline{\text{TBST}}$, and $\overline{\text{OE}}$ signals.</td></tr>
<tr><td>Figure 17-34/Page 17-31</td><td>Remove internal termination dashed lines for $\overline{\text{FBCS}}$, $\overline{\text{BE/BWE}}$, $\overline{\text{TBST}}$, and $\overline{\text{OE}}$ signals.</td></tr>
<tr><td>Table 21-2/Page 21-8</td><td>Change MAXMB description from “This 6-bit field...” to “This 4-bit field...”</td></tr>
</table>

Table 1. MCF5485RM Rev 4 Errata (continued)

Location	Description
Section 22.4.4.5/Page 22-8	Add the following at the end of the RNG section: **CAUTION** There is no known cryptographic proof showing that this is a secure method of generating random data. In fact, there may be an attack against the random number generator if its output is used directly in a cryptographic application (the attack is based on the linearity of the internal shift registers). In light of this, it is highly recommended to use the random data produced by this module as an input seed to a NIST-approved (based on DES or SHA-1) or cryptographically-secure (RSA generator or BBS generator) random number generation algorithm. It is also recommended to use other sources of entropy along with the RNG to generate the seed to the pseudorandom algorithm. The more random sources combined to create the seed the better. The following is a list of sources which can be easily combined with the output of this module. • Current time using highest precision possible • Mouse and keyboard motions (or equivalent if being used on a cell phone or PDA) • Other entropy supplied directly by the user **NOTE** See Appendix D of the NIST Special Publication 800-90 “Recommendation for Random Number Generation Using Deterministic Random Bit Generators” for more information: • http://csrc.nist.gov
Table 27-2/Page 27-4	Correct PSCRFCR and PSCTFCR from 8 bits to 32 bits wide in memory map.
Section 27.7.2	Correct PSCRFCR and PSCTFCR values from 0F to 0C00_0000 throughout examples. Change WRITE TAG = 00 to WFR = 0 throughout examples.
Table 27-41/Page 27-49	In step #1, change value of PSCSICR to 00 and remove the RxDCD sub-row as this bit is not implemented. In step #6, change value of PSCACR to 01 and remove the IEC1 sub-row as this bit is not implemented.
Table 27-44/Page 27-52	In step #6, remove the IEC1 sub-row as this bit is not implemented.
Section 28.7.2.4/Page 28-21	Change second sentence from “The TX FIFO holds from 1 to 16 longwords...” to “The TX FIFO holds from 1 to 4 longwords...”
Section 28.7.2.5/Page 28-22	Change second sentence from “The RX FIFO holds from 1 to 16 received...” to “The RX FIFO holds from 1 to 4 received...”
Chapter 30	Add note to beginning of chapter: **CAUTION** The MCF548x devices contain a silicon errata that affects the usage of the USB device controller. Please see *MCF5485 Device Errata* (MCF5485DE) at http://www.freescale.com/coldfire for details.
Section 30.3.4.5.2/Page 30-54	Add the following to the end of step #5: “In the case of a Control Read, an empty Data OUT packet is used in the status stage to indicate a successful transfer. To accomplish this, the TXZERO bit in the EP*n*OUTSR should also be set.”
Table 31-4/Page 31-6	Correct MIB block counters end addresses to MBAR + 0x92FF and MBAR + 0x9AFF
Table 32-1/Page 32-1	Remove extraneous overbars from the following signals: SDDATA31, SDADDR4, SDDATA16, SDDQS2, VSS, EVDD, USBVDD, SDBA1, SDBA0.

Table 1. MCF5485RM Rev 4 Errata (continued)

Location	Description
Figure 32-1/Page 32-8	Remove extraneous overbars from the following pin/signals: B5/SDDQS2, B6/SDDATA21, C6/SDVDD, D4/SDDATA16, D6/VSS. Change F1 from ‘SDDDATA10’ to ‘SDDATA10’ (remove extra D). Change B3 from ‘SDDDATA18’ to ‘SDDATA18’ (remove extra D).
Figure 32-2/Page 32-9	Remove extraneous overbars from the following pin/signals: A15/DSI/TDI, A16/TCK, A18/MTMOD1, A19/PLLVDD, A21/PSTDDATA1, A23/PSTDDATA7, B15/TMS, B22/E1RXCLK, C15/DSCLK, C21/VSS, C25/SCL, E24/EVDD, H23/IVDD, H24/EVDD.
Figure 32-3/Page 32-10	Remove extraneous overbars from the following pin/signals: P4/IVDD, AF2/AD25
Figure 32-4/Page 32-11	Remove extraneous overbars from the following pin/signals: U24/EVDD, V26/PCIAD30, AA25/PSC0TXD, AC18/VSS, AC20/IVDD, AC26/PSC2TXD, AE18/USBVDD, AE21/PSC3RXD, AF18/USBRBIAS, AF21/TIN2, AF22/TIN0.
Figure 32-5/Page 32-12	Remove extraneous overbars from the following pin/signals: B5/SDDQS2, B6/SDDATA21, C6/SDVDD, D4/SDDATA16, D6/VSS. Change F1 from ‘SDDDATA10’ to ‘SDDATA10’ (remove extra D). Change B3 from ‘SDDDATA18’ to ‘SDDATA18’ (remove extra D).
Figure 32-6/Page 32-13	Remove extraneous overbars from the following pin/signals: A15/DSI/TDI, A16/TCK, A18/MTMOD1, A19/PLLVDD, A21/PSTDDATA1, A23/PSTDDATA7, B15/TMS, C21/VSS, C25/SCL, E24/EVDD, H23/IVDD, H24/EVDD.
Figure 32-7/Page 32-14	Remove extraneous overbars from the following pin/signals: P4/IVDD, AF2/AD25.
Figure 32-8/Page 32-15	Remove extraneous overbars from the following pin/signals: U24/EVDD, V26/PCIAD30, AA25/PSC0TXD, AC18/VSS, AC20/IVDD, AC26/PSC2TXD, AE18/USBVDD, AE21/PSC3RXD, AF18/USBRBIAS, AF21/TIN2, AF22/TIN0.
Figure 32-9/Page 32-16	Remove extraneous overbars from the following pin/signals: B5/SDDQS2, B6/SDDATA21, C6/SDVDD, D4/SDDATA16, D6/VSS. Change F1 from ‘SDDDATA10’ to ‘SDDATA10’ (remove extra D). Change B3 from ‘SDDDATA18’ to ‘SDDATA18’ (remove extra D).
Figure 32-10/Page 32-17	Remove extraneous overbars from the following pin/signals: A15/DSI/TDI, A16/TCK, A18/MTMOD1, A19/PLLVDD, A21/PSTDDATA1, A23/PSTDDATA7, B15/TMS, B22/E1RXCLK, C15/DSCLK, C21/VSS, C25/SCL, E24/EVDD, H23/IVDD, H24/EVDD.
Figure 32-11/Page 32-18	Remove extraneous overbars from the following pin/signals: P4/IVDD, AF2/AD25
Figure 32-12/Page 32-19	Remove extraneous overbars from the following pin/signals: U24/EVDD, V26/PCIAD30, AA25/PSC0TXD, AC18/VSS, AC20/IVDD, AC26/PSC2TXD, AE21/PSC3RXD, AF18/USBRBIAS, AF21/TIN2, AF22/TIN0. Change figure title from “MCF5485/5484 Lower Right....” to “MCF5481/5480 Lower Right....”
Section 32.6/Page 32-20	Update package drawing. See http://www.freescale.com and do a keyword search for 98ARS23880W for the updated drawing.

3 Errata for Revision 3

Table 2. MCF5485RM Rev 3 Errata

<table>
<tr><th>Location</th><th>Description</th></tr>
<tr><td>Section 29.1.2/Page 29-1</td><td>Added the following note at the end of the features list:
NOTE
The USB 2.0 device controller requires a minimum XLB/system clock frequency of 66 MHz.</td></tr>
<tr><td>Section 29.1.3.1/Page 29-2</td><td>Added the following note at the end of this section:
NOTE
The USB 2.0 device controller requires a minimum XLB/system clock frequency of 66 MHz.</td></tr>
<tr><td>Section 25.1.3/Page 25-3</td><td>Replaced the Comm Timer External Clock table with the following
Table 25-1 Comm Timers External Clock
<table>
<tr><th>Channel</th><th>External Signal</th></tr>
<tr><td>0</td><td>PSC0BCLK</td></tr>
<tr><td>1</td><td>PSC1BCLK</td></tr>
<tr><td>2</td><td>PSC2BCLK</td></tr>
<tr><td>3</td><td>PSC3BCLK</td></tr>
<tr><td>4</td><td>TIN0</td></tr>
<tr><td>5</td><td>TIN1</td></tr>
<tr><td>6</td><td>TIN2</td></tr>
<tr><td>7</td><td>TIN3</td></tr>
</table></td></tr>
<tr><td>—</td><td>Added FIFO Controller chapter that describes the features of the FIFO controller implemented on many of the communication peripherals.</td></tr>
<tr><td>Section 29.2.1/Page 29-5</td><td>Added the following additional note below the existing note:
8- and 16-bit registers (offsets 0xB000 to 0xB3FF) should not be accessed until the MCF548x is connected to a USB with a stable VBUS. The interrupt generated at the end of the reset signalling (USBISR[RSTSTOP]) can be used as an idication of a stable USB connection.</td></tr>
</table>

Table 2. MCF5485RM Rev 3 Errata (continued)

<table>
<tr><th>Location</th><th>Description</th></tr>
<tr><td>Section 29.2.4.4/Page 29-33</td><td>Changed the INT bit description to:

Interrupt. This bit is set and cleared by the application and is only relevant for interrupt IN endpoints. When an interrupt IN token is received, the USB device controller will use this bit to determine how to respond. If cleared, a NAK response will be sent. If set, the USB device controller will send a data packet if data is available or a NAK if no data is available.
0 No interrupt pending on this endpoint (default).
1 Interrupt pending on this endpoint.

Changed the TXZERO bit description to:

Transmit a zero byte packet. For control endpoints, this bit should only be set by the application and cleared by the USB device controller. For non-control endpoints, the application must set this bit prior to sending a zero-byte packet to the host, and clear this bit after the zero-byte data packet has been successfully transmitted to the host.
0 NOP (default).
1 Transmit a zero-byte packet

Changed the CCOMP bit description to:

Control command complete. Relevant only for control endpoints. For those commands that do not need application intervention, the application can ignore the CCOMP bit. It will be reset in the setup phase and set in the status phase automatically. It will remain set until the next setup token for the particular endpoint is received. For commands that require application intervention, the application must set this bit when it completes the activity for the command. This bit should not be cleared by the application.
0 Control command in process (default).
1 Control command completed.</td></tr>
<tr><td>Section 29.2.5.2/Page 29-36</td><td>Updated FIFOHI and FIFOLO descriptions:

<table>
<tr><td>5</td><td>FIFOHI</td><td>FIFO high. When configured as an OUT FIFO, this indicates that the number of bytes in the FIFO has surpassed the high level alarm value.</td></tr>
<tr><td>4</td><td>FIFOLO</td><td>FIFO low. When configured as an IN FIFO, this indicates that the number of bytes in the FIFO has fallen below the FIFO low level alarm value.</td></tr>
</table>
</td></tr>
</table>

Table 2. MCF5485RM Rev 3 Errata (continued)

Location	Description
Section 29.3/Page 29-50	Made minor layout changes throughout the Functional Description section. Some major updates include the addition of some clarified Handshake information and the addition of a section on "Sending Zero-Length Packets": A packet with a payload size less than *wMaxPacketSize* is used to indicate the end of a transfer. For transfers with a total payload that is evenly divisible by *wMaxPacketSize*, a zero-length packet (ZLP) may need to be transferred to indicate to the Host that the transfer has ended. To send a zero-length packet on an endpoint other then endpoint zero (EP0), the following steps should be followed: 1. Wait for the EOF event for the packet with the last data payload. This will ensure that the IN endpoint's FIFO is empty. 2. Set the TXZERO bit in the EP0SR or EP*n*INSR. 3. Clear the TXZERO bit immediately after the ZLP has been sent. The USBAISR[ACK] event and EPINFO register can be monitored to determine that the ZLP from the active endpoint was properly received. It is important that the FIFO be empty when the TXZERO bit is set. Once set, the USB Device Controller will send a ZLP even if valid data is present in the FIFO. It is also important that the application clears the TXZERO bit as soon as possible after the ZLP is sent. The USB 2.0 Device Controller will continue to send ZLPs in response to IN tokens for the same endpoint until the TXZERO bit is cleared. For EP0, the TXZERO bit should only be set by the application. The USB 2.0 Device Controller will clear the TXZERO bit automatically.

4 Errata for Revision 2.1

Table 3. MCF5485RM Rev 2.1 Errata

Location	Description
Throughout	Replace all instances of MAPBGA with PBGA, as this is the correct package that the devices are available in.
Throughout	Fix missing bit numbers above register diagrams throughout.
Figure 2-1/Page 2-2	• Replace all PPSCL*n* entries in the figure with PPSC1PSC0*n*. There is no PPSCL port. • $\overline{\text{PSC0CTS}}$ pin: Change GPIO entry from PPSCL2 to PPSC1PSC03. • $\overline{\text{PSC0RTS}}$ pin: Change GPIO entry from PPSCL3 to PPSC1PSC02. • $\overline{\text{PSC1CTS}}$ pin: Change GPIO entry from PPSCL6 to PPSC1PSC07. • $\overline{\text{PSC1RTS}}$ pin: Change GPIO entry from PPSCL7 to PPSC1PSC06. • $\overline{\text{PSC2CTS}}$ pin: Change GPIO entry from PPSCH2 to PPSC3PSC23. • $\overline{\text{PSC2RTS}}$ pin: Change GPIO entry from PPSCH3 to PPSC3PSC22. • $\overline{\text{PSC3CTS}}$ pin: Change GPIO entry from PPSCH6 to PPSC3PSC27. • $\overline{\text{PSC3RTS}}$ pin: Change GPIO entry from PPSCH7 to PPSC3PSC26.
Table 2-1/Page 2-3	Add column to indicate whether the signal has a pull-up resistor. These signals have a pull-up resistor at all times: DSCLK/TRST, BKPT/TMS, DSI/TDI These signals have a pull-up resistor whenever configured for general-purpose input (default state after reset): PCIBR[4:3], PCIGNT[4:3], E1MDIO, E1MDC, E1TXCLK, E1TXEN, E1TXD[3:0], E1COL, E1RXCLK, E1RXDV, E1RXD[3:0], E1CRS, E1TXER, E1RXER

Table 3. MCF5485RM Rev 2.1 Errata (continued)

Location	Description
Table 2-1/Page 2-3	Remove overbars from the following signals: FBADDR1, FBADDR0, SDDATA, SDADDR, SDBA, TIN3, TOUT3
Table 2-1/Page 2-3	In entry AD6, remove overbar from $\overline{\text{ALE}}$ and change description from “Transfer start” to “Address latch enable”
Table 2-1/Page 2-6	Add overbars to IRQ[6:5].
Table 2-2/Page 2-11	• Replace PPSCL*n* entries under the GPIO column with PPSC1PSC0*n*. There is no PPSCL port. • Replace PPSCH*n* entries under the GPIO column with PPSC3PSC2*n*. There is no PPSCH port.
Table 2-2/Page 2-11	The GPIO bit number for each of the UART control signals are incorrect for Table 2-2. However, they are correct for Table 2-1: • Y23/$\overline{\text{PSC1RTS}}$ pin: Change GPIO entry from PPSCL7 to PPSC1PSC06. • AB23/$\overline{\text{PSC3RTS}}$ pin: Change GPIO entry from PPSCH7 to PPSC3PSC26. • AB26/$\overline{\text{PSC0RTS}}$ pin: Change GPIO entry from PPSCL3 to PPSC1PSC02. • AC19/$\overline{\text{PSC2CTS}}$ pin: Change GPIO entry from PPSCH2 to PPSC3PSC23. • AD26/$\overline{\text{PSC2RTS}}$ pin: Change GPIO entry from PPSCH3 to PPSC3PSC22. • AE23/$\overline{\text{PSC0CTS}}$ pin: Change GPIO entry from PPSCL2 to PPSC1PSC03. • AF23/$\overline{\text{PSC3CTS}}$ pin: Change GPIO entry from PPSCH6 to PPSC3PSC27. • AF25/$\overline{\text{PSC1CTS}}$ pin: Change GPIO entry from PPSCL6 to PPSC1PSC07.
Table 2-2/Page 2-12	Remove overbars from the following signals: IVDD, TCK, PLLVDD, PSTDDATA1, PSTDDATA7, SDDATA21, PSTDDATA2, E1RXCLK, E1RXD2, SDVDD, SDDATA31, SDADDR4, DSCLK, VSS, EVDD, PCIAD29, PCIAD30, SCL, SDDATA16, AD17, AD20, E1CRS, E0TXD2, TOUT2, TOUT1, PSC2TXD, ALE, E0TXD3, SDBA1, SDBA0, USBVDD, PSC3RXD, AD25, USBRBIAS, TIN1, TIN2, TIN0
Table 2-2/ Page 2-12	Add overbars to the following signals: IRQ3, IRQ2
Table 2-4/Page 2-24	Replace table with the following: **Table 4. MCF548x Divide Ratio Encodings** **AD[12:8][1]** / **Clock Ratio** / **CLKIN–PCI and FlexBus Frequency Range (MHz)** / **Internal XLB, SDRAM bus, and PSTCLK Frequency Range (MHz)** / **Core Frequency Range (MHz)** 00011 / 1:2 / 41.6–50.0 / 83.33–100 / 166.66–200 00101 / 1:2 / 25.0–41.5 / 50.0–83.0[2] / 100.0–166.66 01111 / 1:4 / 25.0 / 100 / 200 NOTES: 1 All other values of AD[12:8] are reserved. 2 Note that DDR memories typically have a minimum speed of 83 MHz. Some vendors specifiy down to 75 MHz. Check with the memory component specifications to verify.

Table 3. MCF5485RM Rev 2.1 Errata (continued)

Location	Description
Section 2.2.6.1/Page 2-24	Add the following after Table 2-4:

Figure 1 correlates CLKIN, internal bus, and core clock frequencies for the 1x–4x multipliers.

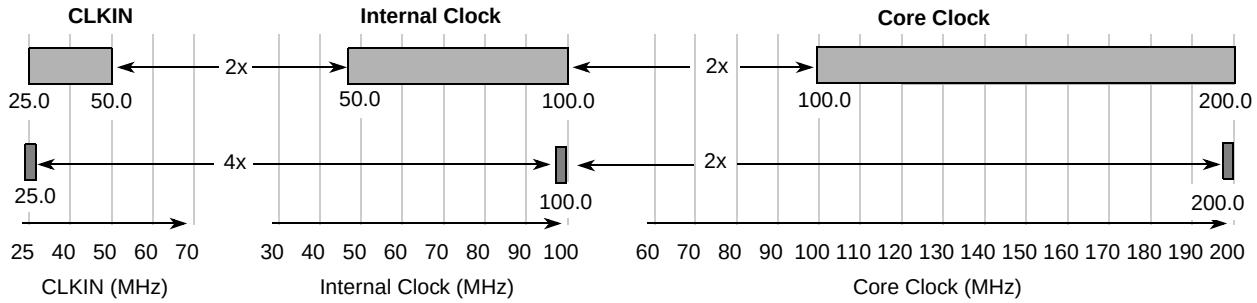

Figure 1. CLKIN, Internal Bus, and Core Clock Ratios

Section 3.8.1/Page 3-40	Change the second sentence of the first paragraph from “The second holds the 32-bit program counter address of the faulted instruction.“ to “The second holds the 32-bit program counter address of the faulted or interrupted instruction.”
Table 3-23/Page 3-44	The “Interrupt exception” entry’s description is outdated. Change from “Interrupt exception processing, with interrupt recognition and vector fetching, includes uninitialized and spurious interrupts as well as those where the requesting device supplies the 8-bit interrupt vector. Autovectoring can optionally be configured through the system interface module (SIM).” to “Please refer to Chapter 13 ‘Interrupt Controller.’”
Table 10-1/Page 10-3	Add missing table using Table 4 from this document.

Table 3. MCF5485RM Rev 2.1 Errata (continued)

Location	Description
Section 10.2/Page 10-5	Insert the following section before section 10.2 “XL Bus Arbiter”.

10.2 PLL

10.2.1 PLL Memory Map/Register Descriptions

Table 5. System PLL Memory Map

MBAR Offset	Name	Byte0	Byte1	Byte2	Byte3	Access
0x300	System PLL Control Register	SPCR				R/W

10.2.2 System PLL Control Register (SPCR)

The system PLL control register (SPCR) defines the clock enables used to control clocks to a set of peripherals. Unused peripherals can have their clock stopped, reducing power consumption. In addition, the SPCR contains a read-only bit for the system PLL lock status. At reset, the clock enables are set, enabling all system PLL gated output clocks.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	PLLK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	COR EN	CRY ENB	CRY ENA	CAN1 EN	0	PSC EN	0	USB EN	FEC1 EN	FEC0 EN	DMA EN	CAN0 EN	FB EN	PCI EN	MEM EN
W																
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Addr MBAR + 0x300

Figure 2. System PLL Control Register (SPCR)

Table 6. SPCR Field Descriptions

Bits	Name	Description
31	PLLK	System PLL Lock Status - Read-only lock status of the system PLL. 1 PLL has obtained frequency lock 0 PLL has not locked
30-15	—	Reserved, should be cleared.
14	COREN	Core & Communications Sub-System Clock Enable - Controls clocks for the CF4 Core, System SRAM, CommBus Arbiter, I2C, Comm Timers, and External DMA modules
13	CRYENB	Crypto Clock Enable B - Controls the fast clock to the SEC
12	CRYENA	Crypto Clock Enable A - Controls the slow clock to the SEC
11	CAN1EN	CAN1 Clock Enable
10	—	Reserved, should be cleared.
9	PSCEN	PSC Clock Enable - Controls clock for all PSC modules.
8	—	Reserved, should be cleared.
7	USBEN	USB Clock Enable
6	FEC1EN	FEC1 Clock Enable
5	FEC0EN	FEC0 Clock Enable
4	DMAEN	Multi-channel DMA Clock Enable
3	CAN0EN	CAN0 Clock Enable
2	FBEN	FlexBus Clock Enable
1	PCIEN	PCI Bus Clock Enable
0	MEMEN	Memory Clock Enable - Controls clocks of the SDRAM controller module

Table 3. MCF5485RM Rev 2.1 Errata (continued)

Location	Description
Table 10-2/Page 10-9	Bits BA, DT, and AT: The 0 and 1 are switched. Setting each bit enables operation, while clearing disables operation. The 0 and 1 (or the corresponding descriptions) need to be swapped for all three bits.
Section 11.4.2/Page 11-9	Remove all text from bullet item #2 starting with “This scenario works for all pulses except....” This errata does not apply to this processor.
Section 13.1.1/Page 13-2	Correct the cross-reference link at top of page that reads “Section 3.8.1, ‘Exception Stack Frame Definition.’”
Table 15-27/Page 15-26	In the bit 7-6, PAR1_E1MDC entry, change ‘11’ bit setting description from: “E1MDC pin configured for FEC1 MDC function” to “E1MDC pin configured for FEC1 E1MDC function” to be consistent with rest of section.
Table 15-34/Page 15-33	Remove extraneous “/” from “DSPICS0//$\overline{SS}$” in second sentence of the PAR_CS0 bit description.
Table 16-1/Page 16-2	Extend SSCR entry to include bytes 2 & 3 as well as bytes 0 and 1, since it is a 32 bit register.
Section 17.6.5.4.2/Page 17-26	Change “transfer start” to “address latch enable” in second sentence.
Section 21.4.9/Page 21-30	Figure 21-14 and Table 21-18 are missing. Add them as shown below and correct the cross-references to them.

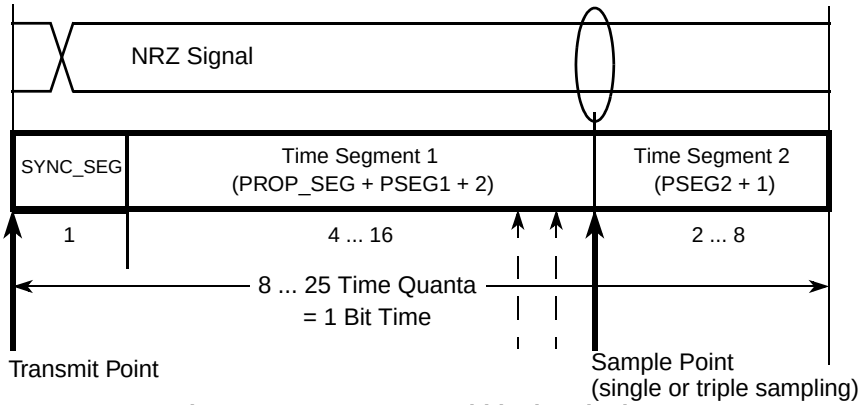

Figure 21-14. Segments within the Bit Time

Table 21-18. Time Segment Syntax

Syntax	Description
SYNC_SEG	System expects transitions to occur on the bus during this period.
Transmit Point	A node in transmit mode transfers a new value to the CAN bus at this point.
Sample Point	A node samples the bus at this point. If the three samples per bit option is selected, then this point marks the position of the third sample.

Table 3. MCF5485RM Rev 2.1 Errata (continued)

<table>
<tr><th>Location</th><th>Description</th></tr>
<tr><td>Section 21.4.9/Page 21-30</td><td>Add the following table below the note at the end of the section and correct the cross-reference pointing to it:
Table 21-19. CAN Standard Compliant Bit Time Segment Settings
<table>
<tr><th>Time Segment 1</th><th>Time Segment 2</th><th>Re-synchronization Jump Width</th></tr>
<tr><td>5 .. 10</td><td>2</td><td>1 .. 2</td></tr>
<tr><td>4 .. 11</td><td>3</td><td>1 .. 3</td></tr>
<tr><td>5 .. 12</td><td>4</td><td>1 .. 4</td></tr>
<tr><td>6 .. 13</td><td>5</td><td>1 .. 4</td></tr>
<tr><td>7 .. 14</td><td>6</td><td>1 .. 4</td></tr>
<tr><td>8 .. 15</td><td>7</td><td>1 .. 4</td></tr>
<tr><td>9 .. 16</td><td>8</td><td>1 .. 4</td></tr>
</table></td></tr>
<tr><td>Section 22.5/Page 22-8</td><td>Split various 64-bit registers into two 32-bit registers labeled ‘High’ and ‘Low’ in memory map table as well as the following sections. Changed registers include: EUACR, SIMR, SISR, SICR, EUASR, CCPSRn.</td></tr>
<tr><td>Table 23-5/Page 23-8</td><td>The JTAG IR codes are incorrect. Replace table with the following:
<table>
<tr><th>Instruction</th><th>IR[5:0]</th><th>Instruction Summary</th></tr>
<tr><td>EXTEST</td><td>000000</td><td>Selects boundary scan register while applying fixed values to output pins and asserting functional reset</td></tr>
<tr><td>SAMPLE</td><td>000001</td><td>Selects boundary scan register for shifting, sampling, and preloading without disturbing functional operation</td></tr>
<tr><td>IDCODE</td><td>011101</td><td>Selects IDCODE register for shift</td></tr>
<tr><td>CLAMP</td><td>011111</td><td>Selects bypass while applying fixed values to output pins and asserting functional reset</td></tr>
<tr><td>HIGHZ</td><td>111101</td><td>Selects bypass register while tri-stating all output pins and asserting functional reset</td></tr>
<tr><td>ENABLE</td><td>000010</td><td>Selects TEST_CTRL register</td></tr>
<tr><td>BYPASS</td><td>111111</td><td>Selects bypass register for data operations</td></tr>
</table></td></tr>
<tr><td>Section 23.4.3.4/Page 23-9</td><td>Remove section, as the TEST_LEAKAGE instruction is not supported.</td></tr>
<tr><td>Section 23.4.3.7/Page 23-9</td><td>Remove section, as the LOCKOUT_RECOVERY instruction is not supported.</td></tr>
<tr><td>Table 24-20/Page 24-22</td><td>Correct Base Address Mask Register 1 mnemonic from EREQMASK0 to EREQMASK1.</td></tr>
<tr><td>Section 24.3.4.2/Page 24-22</td><td>Correct overbar in first sentence. From “After $\overline{\text{DREQ is asserted}}$, this register contains...” to “After $\overline{\text{DREQ}}$ is asserted, this register contains...”</td></tr>
</table>

Table 3. MCF5485RM Rev 2.1 Errata (continued)

<table>
<tr><th>Location</th><th>Description</th></tr>
<tr><td>Section 25.1.2/Page 25-3</td><td>Add the following section after section 24.1.2:

24.1.3 Comm Timer External Clock[7:0]
The comm timer external clock is the alternate clock signal and is provided by the user. The user must write a 1 to CTCR[S] in the variable channel and write a 1001 to CTCR[S] within the fixed channel to select this signal. If this signal is selected, all timing will be with respect to this clock signal. This signal is restricted to being half the frequency or less of the system bus clock.
Table 4-7. Comm Timers External Clock
<table><tr><th>Timer Channel</th><th>External Signal</th></tr><tr><td>0</td><td>TIN0</td></tr><tr><td>1</td><td>TIN1</td></tr><tr><td>2</td><td>TIN2</td></tr><tr><td>3</td><td>TIN3</td></tr><tr><td>4</td><td>PSC3BCLK</td></tr><tr><td>5</td><td>PSC2BCLK</td></tr><tr><td>6</td><td>PSC1BCLK</td></tr><tr><td>7</td><td>PSC0BCLK</td></tr></table></td></tr>
<tr><td>Table 25-2/Page 25-5</td><td>In the S bit description change the 1001 setting from “Reserved” to “External clock”</td></tr>
<tr><td>Table 25-3/Page 25-7</td><td>The S bit field is incorrect. Bits 31-29 should be reserved, and only bit 28 should be the S bit. And the S bit description should be:
Clock enable source select. Selects the clock rate for the fixed timer channels. The clock rate for the timer is the internal system clock divided by an 8-bit prescaler.
1 External Clock
0 Sysclk
Note: The external bus clock cannot be an faster than half the frequency of the system clock.</td></tr>
<tr><td>Section 26.1/Page 26-1</td><td>Fix broken cross-reference to Figure 26-1.</td></tr>
<tr><td>Table 26-13/Page 26-20</td><td>In description of TXRDY change PSCTFALARM to PSCTFAR</td></tr>
<tr><td>Section 26.3.3.24/Page 26-30</td><td>Change bit 30 of PSCRFCRn/PSCTFCRn register to reserved, as the WFR field is only one-bit wide.</td></tr>
<tr><td>Table 26-30/Page 26-31</td><td>In description of ALARM change instance of “less than alarm bytes” to “more than alarm bytes” and change instance of “more than alarm bytes” to “less than alarm bytes”.</td></tr>
<tr><td>Figure 26-22/Page 26-33</td><td>Remove shading from W field as the PSCRFARn and PSCTFARn registers are R/W accessible.</td></tr>
<tr><td>Section 26.4/Page 26-44</td><td>Add section 15.3.7 “PSC FIFO System” from the MPC5200 User’s Manual to before section 26.4.9 “Looping Modes.” Change the following text to apply to the MCF548x:
MPC5200 → MCF548x
BestComm → Multichannel DMA
MR1 → PSCMR1n
SR→ PSCSRn
ORERR → ERR</td></tr>
<tr><td>Figre 27-1/Page 27-1</td><td>Change IFDR to I2FDR and IADR to I2ADR in figure.</td></tr>
<tr><td>Section 27.3.2.1/Page 27-3</td><td>Change instances of I2AR to I2ADR.</td></tr>
<tr><td>Section 27.3.2.3/Page 27-5</td><td>Change I2ICR to I2CR throughout section.</td></tr>
<tr><td>Chapter 27</td><td>After section 27.3.2.4, change instances of R/W to R/$\overline{W}$ throughout chapter.</td></tr>
</table>

Table 3. MCF5485RM Rev 2.1 Errata (continued)

Location	Description
Section 28.6.1/Page 28-5	Remove instances of MDIS bit as it is not present on this version of the DSPI.
Table 29-3/Page 29-13	USBCR[APPLOCK] bit description, the bit setting numbers are incorrrect. When cleared (0), APPLOCK is deasserted. When set (1), APPLOCK is asserted.
Table 29-29/Page 29-33	Endpoint status register's PSTALL entry: the last sentence should be "Setting this bit also sets USBAISR[EPSTALL]." instead of "Setting this bit also sets USBAISR[EPHALT]."
Table 29-37/Page 29-39	EP*n*ISR[EOT] bit description, add a note to the last sentence of the first paragraph stating "The EOT interrupt will not assert for an isochronous OUT packet that experiences a PID sequencing error."
Section 29.4.3.1/Page 29-54	Add a section below USB Packets entitled "Handshakes" with the following paragraphs: "The USB device will return a NYET handshake packet to an OUT transaction if there is already data present in the FIFO and there are less than 2*MAXPACKETSIZE bytes free in the FIFO. In cases where the FIFO depth is larger than 2*MAXPACKETSIZE (i.e. 3x or 4x), the following behavior will occur. If after a transfer that returned a NYET handshake there is at least 1*MAXPACKETSIZE of free space in the FIFO, the device will ACK the first PING request from the host and accept another MAXPACKETSIZE transfer from the host. The device will again send a NYET handshake. The only time the device will NAK a PING is when there is less than 1*MAXPACKETSIZE of free space in the FIFO."
Table 30-41/Page 30-45	Change bit description of the FECFRST[SW_RST] bit to "Software Reset - This bit controls the soft reset of the FEC FIFOs. A soft reset will reset the FIFO pointers and byte counters but not the status and control registers. To cause a soft reset this bit should be set and then cleared by application software." Change bit description of the FECFRST[RST_CTL] bit to "Reset control - Setting this bit allows the FEC controller to perform a soft reset of the FIFOs when the FEC is disabled (ECR[ETHER_EN] cleared)."
Table 31-1/Page 31-1	Add column to indicate whether the signal has a pull-up resistor. These signals have a pull-up resistor at all times: DSCLK/TRST, BKPT/TMS, DSI/TDI These signals have a pull-up resistor whenever configured for general-purpose input (default state after reset): PCIBR[4:3], PCIGNT[4:3], E1MDIO, E1MDC, E1TXCLK, E1TXEN, E1TXD[3:0], E1COL, E1RXCLK, E1RXDV, E1RXD[3:0], E1CRS, E1TXER, E1RXER
Table 31-1/Page 31-1	Ball P3 should be SD_VDD instead of EVDD.
Table 31-1/Page 31-1	The GPIO bit number for each of the UART control signals are incorrect for Table 31-1. However, they are correct for Table 2-1: • Y23/$\overline{\text{PSC1RTS}}$ pin: Change GPIO entry from PPSCL7 to PPSC1PSC06. • AB23/$\overline{\text{PSC3RTS}}$ pin: Change GPIO entry from PPSCH7 to PPSC3PSC26. • AB26/$\overline{\text{PSC0RTS}}$ pin: Change GPIO entry from PPSCL3 to PPSC1PSC02. • AC19/$\overline{\text{PSC2CTS}}$ pin: Change GPIO entry from PPSCH2 to PPSC3PSC23. • AD26/$\overline{\text{PSC2RTS}}$ pin: Change GPIO entry from PPSCH3 to PPSC3PSC22. • AE23/$\overline{\text{PSC0CTS}}$ pin: Change GPIO entry from PPSCL2 to PPSC1PSC03. • AF23/$\overline{\text{PSC3CTS}}$ pin: Change GPIO entry from PPSCH6 to PPSC3PSC27. • AF25/$\overline{\text{PSC1CTS}}$ pin: Change GPIO entry from PPSCL6 to PPSC1PSC07.

Table 3. MCF5485RM Rev 2.1 Errata (continued)

Location	Description
Table 31-1/Page 31-5	Remove overbar from $\overline{\text{ALE}}$ at location AD6.
Table 31-1/Page 31-7	• Replace PPSCL*n* entries under the GPIO column with PPSC1PSC0*n*. There is no PPSCL port. • Replace PPSCH*n* entries under the GPIO column with PPSC3PSC2*n*. There is no PPSCH port.
Figure 31-3/Page 31-11	Remove overbar from $\overline{\text{ALE}}$ at location AD6.
Figure 31-7/Page 31-15	Remove overbar from $\overline{\text{ALE}}$ at location AD6.
Figure 31-11/Page 31-19	Remove overbar from $\overline{\text{ALE}}$ at location AD6.

5 Revision History

Table 8 provides a revision history for this document.

Table 8. Revision History Table

Rev. Number	Substantive Changes	Date of Release
0	Initial release. • Added ball P3 errata • Added DSPI MDIS errata • Added four USB chapter errata: USBCR[APPLOCK], PSTALL, EP*n*ISR[EOT], and handshakes section addition. • Added SDDATA and SDADDR errata. • Added I2ICR→I2CR errata. • Added MAPBGA→PBGA errata.	08/2005
1	Added many errata: • Missing bit numbers in register diagrams • Add/remove overbars to Table 2-1 & 2-2 • Correct ALE signal name, and remove overbars throughout • Fix clock divide ratio tables • Add clock frequency correlation figure • Add PLL memory map section • Removal of GPT errata • Removal of extra “/” in PAR_CS0 bit description • Add section regarding Comm Timer external clock • Change CTCR*n*[S] bit description and diagram • Figure 26-1 broken cross-reference • Correct PSCISR*n*[TXRDY] and PSCRFSR*n*,PSCTFSR*n*[ALARM] descriptions • Make PSCRFAR*n* and PSCTFAR*n* register diagrams R/W • Add section from MPC5200UM • Change I2AR → I2ADR • Change R/W → R/W_b • Change FECFRST[SW_RST,RST_CTL] bit descriptions	09/2005

Table 8. Revision History Table (continued)

Rev. Number	Substantive Changes	Date of Release
2	• Added PPSCL*n* and PPSCL*n* errata for Table 2-2 and Table 31-1 • Added UART control signal's GPIO bit number errata in Table 2-2 and Table 31-1 • Added JTAG IR codes errata • Added FlexCAN chapter's missing tables and figure. • Added PAR_E1MDC bit description errata. • Added interrupt exception description errata in the ColdFire core chapter. • Added broken cross-reference at beginning of Chapter 13. • Added exception stack frame's second longword clarification. • Added I^2C block diagram's register-naming errata. • Added DMA Base Address Mask Register 1 mnemonic errata. • Added extraneous overbar in DMA chapter.	12/2005
3	• Added XARB_CFG[BA,DT,AT] bit setting errata. • Added SSCR register width errata. • Added SEC 64-bit registers errata. • Added PSCRFCR*n*/PSCTFCR*n*[30] bit errata.	1/2006
The following errata were added to Rev 3 of the MCF5485RM		
4	• Added errata regarding minimum system clock for proper operation of the USB controller. • Added FIFO controller chapter errata. • Added Comm Timer External Clock table errata. • Added note regarding register access until USB is stable errata. • Added EP*n*OUTSR and EP*n*INSR bit field description errata. • Added EP*n*ISR bit field description errata.	7/2006
The following errata were added to Rev 4 of the MCF5485RM		
4.1	• Added extraneous and missing overbars errata to signals table and pinout diagrams. • Added USBVBUS errata. • Added FEC MIB counter memory map errata. • Added internal termination figure errata for longword write bursts. • Added FlexBus chapter wait states errata. • Added interrupt level/priority table. • Added USB Device Requests step 5 errata. • Added PSC examples errata. • Added GSR*n* and SSR*n* register access errata. • Added clocking options table errata. • Added MAXMB bit description errata. • Added clarification to multiple CAN controllers in overview chapter. • Added E1MDIO and E1MDC signal table errata. • Added AD3 bit setting errata in overview chapter. • Added cache initialization sequence errata.	5/2007
5	• Added package drawing errata. • Added Flexbus, PCI, and SDRAM maximum operating frequency errata. • Added RNG caution and note. • Added DSPI FIFO size errata. • Added PSC PSCRFCR and PSCRFCR register size and example settings errata. • Added MCF5485RM rev 5 section.	4/2009

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
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