Freescale Semiconductor
Reference Manual Addendum

MCF5275RMAD
Rev. 2.2, 05/2007

MCF5275 Reference Manual Errata

by: Microcontroller Division

This errata document describes corrections to the *MCF5275 Reference Manual*, order number MCF5275RM. For convenience, the addenda items are grouped by revision. Please check our website at http://freescale.com/coldfire for the latest updates.

The current version available of the *MCF5275 Reference Manual* is Revision 2.

Table of Contents

1 Errata for Revision 2

Table 1. MCF5275RM Rev 2 Errata

Location	Description
Table 1-1/Page 1-2	Change “CIM = Chip Configuration Module + Reset Controller Module” to “Chip Configuration Module + Reset Controller Module”.
Figure 1-1/Page 1-3	Change instance of CIM to “CCM and Reset Controller”.
Section 1.3.1/Page 1-7	Change “Chip Integration Module (CIM)” to “Chip Configuration Module (CCM)”. Move Reset sub-bullet (and its sub-bullets) up one level.
Table 3-1/Page 3-4	Remove last sentence in C bit field description.
Table 3-5/Page 3-8	Change PC’s Written with MOVEC entry to “No”.
Section 3.4/Page 3-9	Change last bullet to “Use of separate system stack pointers for user and supervisor modes”
Section 3.5/Page 3-10	Change last sentence in fourth paragraph (step 2) to “The IACK cycle is mapped to special locations within the interrupt controller's address space with the interrupt level encoded in the address."
Figure 4-9/Page 4-14	Add minus sign to the exponent so that it is “–(i + 1 – N)”.
Table 5-3/Page 5-7	Change reset value of ACR0, ACR1 to “See Section” since some of the bits are undefined after reset.
Figure 5-2/Page 5-7	Change CACR fields to R/W, since they may be read via the debug module.
Table 5-5/Page 5-10	For split instruction/data cache entry, swap text in parantheses in the description field. Instruction cache uses the upper half of the arrays, while data cache uses the lower half.
Figure 5-3/Page 5-11	Change reset value of ACR: Bits 31-16, 14-13, 6-5, and 2 are undefined, and other bits are cleared. Change ACR fields to R/W, since they may be read via the debug module.
Section 5.2.1.2/Page 5-11	Change note to: **NOTE** Peripheral (IPSBAR) space should not be cached. The combination of the CACR defaults and the two ACR*n* registers must define the non-cacheable attribute for this address space.
Figure 6-1/Page 6-2	Change RAMBAR fields to R/W, since they may be read via the debug module.
Section 11.2.1.1/Page 11-3	After the first paragraph add the following note: **NOTE** Accessing reserved IPSBAR memory space could result in an unterminated bus cycle that causes the core to hang. Only a hard reset will allow the core to recover from this state. Therefore, all bus accesses to IPSBAR space should fall within a module's memory map space.
Table 12-9/Page 12-19	Change footnote from “...of the RCSC field in the CIM reset configuration register.” to “... of the RCR[RCSC] field in the reset controller.”

Table 1. MCF5275RM Rev 2 Errata (continued)

<table>
<tr><th>Location</th><th>Description</th></tr>
<tr><td>Table 13-1/Page 13-2</td><td>Replace table with the one below to better illustrate the interrupt priority and level assignments.
<table>
<tr><th>Interrupt Level ICR[IL]</th><th>Priority

ICR[IP]</th><th>Supported Interrupt Sources</th></tr>
<tr><td rowspan="10">7</td><td>7</td><td rowspan="4">#8–63</td></tr>
<tr><td>6</td></tr>
<tr><td>5</td></tr>
<tr><td>4</td></tr>
<tr><td>— (Mid-point)</td><td>#7 (IRQ7)</td></tr>
<tr><td>3</td><td rowspan="4">#8–63</td></tr>
<tr><td>2</td></tr>
<tr><td>1</td></tr>
<tr><td>0</td></tr>
<tr><td rowspan="3">6</td><td>7–4</td><td>#8–63</td></tr>
<tr><td>— (Mid-point)</td><td>#6 (IRQ6)</td></tr>
<tr><td>3–0</td><td>#8–63</td></tr>
<tr><td rowspan="3">5</td><td>7–4</td><td>#8–63</td></tr>
<tr><td>— (Mid-point)</td><td>#5 (IRQ5)</td></tr>
<tr><td>3–0</td><td>#8–63</td></tr>
<tr><td rowspan="3">4</td><td>7–4</td><td>#8–63</td></tr>
<tr><td>— (Mid-point)</td><td>#4 (IRQ4)</td></tr>
<tr><td>3–0</td><td>#8–63</td></tr>
<tr><td rowspan="3">3</td><td>7–4</td><td>#8–63</td></tr>
<tr><td>— (Mid-point)</td><td>#3 (IRQ3)</td></tr>
<tr><td>3–0</td><td>#8–63</td></tr>
<tr><td rowspan="3">2</td><td>7–4</td><td>#8–63</td></tr>
<tr><td>— (Mid-point)</td><td>#2 (IRQ2)</td></tr>
<tr><td>3–0</td><td>#8–63</td></tr>
<tr><td rowspan="3">1</td><td>7–4</td><td>#8–63</td></tr>
<tr><td>— (Mid-point)</td><td>#1 (IRQ1)</td></tr>
<tr><td>3–0</td><td>#8–63</td></tr>
</table></td></tr>
<tr><td>Table 13-2/Page 13-5</td><td>In footnote, remove mention of the SWIACK register, as it is not supported in the global IACK space.</td></tr>
<tr><td>Table 13-3/Page 13-6</td><td>Added global IACK addresses for the L1IACK–L7IACK registers in the IPSBAR offset column, 0xFE4–0xFFC.</td></tr>
<tr><td>Section 13.2.1.7/Page 13-16</td><td>Change last paragraph to: “In addition to the IACK registers within each interrupt controller, there are global LnIACK registers. A read from one of the global LnIACK registers returns the vector for the highest priority unmasked interrupt within a level for all interrupt controllers. There is no global SWIACK register. However, reading the SWIACK register from each interrupt controller returns the vector number of the highest priority unmasked request within that controller.”</td></tr>
<tr><td>Figure 14-3/Page 14-4</td><td>Figure incorrectly shows that EPDDR is 16-bits wide. Change to an 8-bit register with each EPDDn bit a one-bit field from bits 7–1 to match Table 15-4.</td></tr>
<tr><td>Figure 15-2/Page 15-5</td><td>Re-labeled the WS states in the timing diagram. The first should be IWS to indicate that the length of this wait state is determined by CSCR[IWS]. The rest of the wait states should be IWS/SWWS to indicate that either CSCR[IWS] or CSCR[SWWS] determine the length of the wait state depending on the value of CSCR[AA].</td></tr>
</table>

Table 1. MCF5275RM Rev 2 Errata (continued)

Location	Description
Figure 15-3/Page 15-5	Re-labeled the WS states in the timing diagram. The first should be IWS to indicate that the length of this wait state is determined by CSCR[IWS]. The rest of the wait states should be IWS/SRWS to indicate that either CSCR[IWS] or CSCR[SRWS] determine the length of the wait state depending on the value of CSCR[AA]. Change Write labels on the data signals to Read.
Table 17-8/Page 17-17	Change note in SDCR[DQS_OE] field description from "**Note:** For 01 and 10 settings, some 32-bit DDR devices only have a single $\overline{\text{SD\_DQS}}$ pin. Enable one of the signals and disable the other. Then short both pins external to the device." to "**Note:** Some 16-bit DDR devices only have a single $\overline{\text{SD\_DQS}}$ pin. Therefore, use the 01 or 10 settings and short both pins external to the device."
Section 17.5.3/Page 17-17	Add the following after the first two paragraphs: **NOTE** In DDR mode, the memory controller counts the delay in DDR_CLKOUT × 2 DDR_CLKOUT—memory controller clock—is the speed of the SDRAM interface and is equal to the internal bus clock. DDR_CLKOUT × 2—double frequency of DDR_CLKOUT—DDR uses both edges of the bus-frequency clock (DDR_CLKOUT) to read/write data.
Table 17-9/Page 17-18	Change SDCFG1[SRD2RW] field description equation from "SRD2RW = Burst Length/2" to "SRD2RW = CASL + Burst Length/2 + 1" with a suggested value of 0x7.
Table 17-9/Page 17-19	Add the following examples to the ACT2RW and PRE2ACT field descriptions: "EXAMPLE: If t_{RCD} = 20ns and DDR_CLKOUT = 75 MHz 20ns / 13.3 ns = 1.5; round to 2; write 0x1. Count value is in DDR_CLKOUT periods."
Section 17.5.4/Page 17-19	Change "CLKOUT" in last sentence to "DDR_CLKOUT."
Table 17-10/Page 17-19	Change BWT2RW equation from: BWT2RW = (BurstLength / 2 + t_{WR}) to: BWT2RW = (BurstLength / 2 + t_{WR} / t_{DDR_CLKOUT})
Table 17-10/Page 17-20	Change BRD2WT field description from "Write 0xB for best performance. All values less than 0xB are reserved." to "For DDR, suggested value = 0x7."
Section 17.7/Page 17-23	Many corrections with the DDR SDRAM example: Change example to two 16M x 16-bit DDR SDRAM operating at 75 MHz DDR_CLKOUT frequency. Update SDRAM example specifications to the following: CAS latency: 2 Clock cycle time (t_{ck}): 7.5ns (min) ACTV-to-read/write delay (t_{RCD}): 15ns (min) 18ns (max) Write recovery timer (t_{WR}): 15ns Precharge command to ACTV command (t_{RP}): 15 ns (min) 18ns (max) Auto refresh command period (t_{RFC}): 72ns (min) 75ns (max) Average periodic refresh interval (t_{REFI}): 7.8 µs
Section 17.7.1/Page 17-25	Change SDMR0 setting from 0x03FC_0001 to 0x07FC_0001.

Table 1. MCF5275RM Rev 2 Errata (continued)

Location	Description
Section 17.7.2/Page 17-25	Change SDCFG1 from 0x2361_1630 to 0x7361_1530. SRD2RW field using proper equation of CASL + bustlength/2 + 1 = 2 + 8/2 + 1 = 7 Change other equations to use a t_{DDR_CLKOUT} of 13.3ns since the example uses a 75 MHz frequency. However the only value this affects is REF2ACT which results in a setting of 5 instead of 6.
Section 17.7.3/Page 17-26	Change SDCFG2 from 0x2433_0000 to 0x4677_0000. The burst length used in the equations should be 8 instead of 4. The correct recommended value of BRD2WT is 0x7.
Table 17-17/Page 17-26	Change BWT2RW entry's description to: BWT2RW = BurstLength / 2 + t_{WR} / t_{DDR_CLKOUT} = 8/2 + 15/8.3 = 4 + 1.8 = 5.8, rounded up to 6
Section 17.7.4/Page 17-27	Change SDCR from 0xC109_0002 to 0xC108_0002. Change RCNT equation to use a t_{DDR_CLKOUT} of 13.3ns since the example uses a 75 MHz frequency. This changes the value from 9 to 8.
Section 17.7.6/Page 17-29	Change SDMR from 0x049D_0000 to 0x048D_0000. Correct BLEN from 0x7 to 0x3.
Section 17.7.7/Page 17-30	Change SDCR from 0xC109_0002 to 0xC108_0002. Change RCNT equation to use a t_{DDR_CLKOUT} of 13.3ns since the example uses a 75 MHz frequency. This changes the value from 9 to 8.
Section 17.8/Page 17-31	Change section number to Section 17.7.8. Change SDCR from 0xC109_0004 to 0xC108_0004. Change RCNT equation to use a t_{DDR_CLKOUT} of 13.3ns since the example uses a 75 MHz frequency. This changes the value from 9 to 8.
Section 17.8.1/Page 17-32	Change section number to Section 17.7.9. Change SDMR from 0x009D_0000 to 0x008D_0000. Correct BLEN from 0x7 to 0x3.
Section 17.8.2/Page 17-33	Change section number to Section 17.7.10. Change SDCR from 0x510D_0C00 to 0x5108_0C00. Change RCNT equation to use a t_{DDR_CLKOUT} of 13.3ns since the example uses a 75 MHz frequency. This changes the value from 9 to 8.

Table 1. MCF5275RM Rev 2 Errata (continued)

Location	Description
Section 17.8.3/Page 17-34	Change section number to Section 17.7.11. Change code sequence to the following as a result of the above changes: Basic Configuration and Initialization: move.l #0x00000000, d0 //Initialize SDBAR0 move.l d0, SDBAR0 move.l #0x03FC0001, d0 //Initialize SDMR0 move.l d0, SDMR0 move.l #0x73611530, d0 //Initialize SDCFG1 move.l d0, SDCFG1 move.l #0x46770000, d0 //Initialize SDCFG2 move.l d0, SDCFG2 Precharge Sequence and enable write to SDMR: move.l #0xC1080002, d0 //Initialize SDCR, send PALL, enable SDMR move.l d0, SDCR move.l #0x0, a0 //dummy write move.l #0xdeadbeef, (a0) Write Extended Mode Register: move.l #0x40010000, d0 //Write LEMR to enable DLL move.l d0, SDMR move.l #0x0, a0 //dummy write move.l #0xdeadbeef, (a0) Write Mode Register and Reset DLL: move.l #0x048D0000, d0 //Write LMR and reset DLL move.l d0, SDMR move.l #0x0, a0 //dummy write move.l #0xdeadbeef, (a0) Precharge Sequence: move.l #0xC1080002, d0 //Send PALL move.l d0, SDCR move.l #0x0, a0 //dummy write move.l #0xdeadbeef, (a0) Refresh Sequence: move.l #0xC1080004, d0 //Send first REF command move.l d0, SDCR move.l #0x0, a0 //dummy write move.l #0xdeadbeef, (a0) move.l #0xC1080004, d0 //Send second REF command move.l d0, SDCR move.l #0x0, a0 //dummy write move.l #0xdeadbeef, (a0) Write Mode Register and Clear Reset DLL: move.l #0x008D0000, d0 //Write LMR and clear reset DLL move.l d0, SDMR move.l #0x0, a0 //dummy write move.l #0xdeadbeef, (a0) Enable Auto Refresh and Lock SDMR: move.l #0x51080C00, d0 //Enable auto refresh and clear MODE_EN move.l d0, SDCR move.l #0x0, a0 //dummy write move.l #0xdeadbeef, (a0)
Figure 18-1/Page 18-2	Remove this figure as it is incorrect for this device. The second figure on page 18-3 (with $\overline{\text{DREQ3}}$) is correct
Section 18.4/Page 18-13	Remove last sentence in this section starting with “BCR*n* decrements...” since SAA bit is not supported.
Section 18.4.4.1/Page 18-16	Remove instances of eTPU in this section. Change $\overline{\text{DREQ}}$[32:0] to $\overline{\text{DREQ}}$[3:0]. Remove third sentence in second paragraph.
Figure 18-9/Page 18-17	Change CLKIN to CLKOUT Add overbars to TS, CS, and TA.

Table 1. MCF5275RM Rev 2 Errata (continued)

Location	Description
Section 18.4.4.1/Page 18-17	Remove all text and figures in this section starting with “Since bus timings...”
Table 19-1/Page 19-5	Correct MIB block counters end addresses to IPSBAR + 0x12FF and IPSBAR + 0x20FF
Table 19-3/Page 19-8	Add RMON_R_DROP*n* with an IPSBAR Offset of 0x1280 & 0x2080 and a description of ‘Count of frames not counted correctly’.
Section 19.3.6/Page 19-38	Add the following subsection entitled “Duplicate Frame Transmission”: The FEC fetches transmit buffer descriptors (TxBDs) and the corresponding transmit data continuously until the transmit FIFO is full. It does not determine whether the TxBD to be fetched is already being processed internally (as a result of a wrap). As the FEC nears the end of the transmission of one frame, it begins to DMA the data for the next frame. In order to remain one BD ahead of the DMA, it also fetches the TxBD for the next frame. It is possible that the FEC will fetch from memory a BD that has already been processed but not yet written back (that is, it is read a second time with the R bit still set). In this case, the data is fetched and transmitted again. Using at least three TxBDs fixes this problem for large frames, but not for small frames. To ensure correct operation for either large or small frames, one of the following must be true: • The FEC software driver ensures that there is always at least one TxBD with the ready bit cleared. • Every frame uses more than one TxBD and every TxBD but the last is written back immediately after the data is fetched. • The FEC software driver ensures a minimum frame size, *n*. The minimum number of TxBDs is then (Tx FIFO Size ÷ (*n* + 4)) rounded up to the nearest integer (though the result cannot be less than three). The default Tx FIFO size is 192 bytes; this size is programmable.
Figure 29-8/Page 29-7	Move SKMR[CTRM,DKP] bit fieldsfrom 11–7 to 12–8.
Table 29-2/Page 29-8	Correct bit locations for CTRM and DKP fields: 31–13 Reserved 12–9 CTRM 8 DKP 7–5 Reserved
Table 31-13/Page 31-13	Add the following note to the PBR[Address] field description: **Note:** PBR[0] should always be loaded with a 0.
Table 31-21/Page 31-36	Change CSR’s initial state to 0x0090_0000.

2 Errata for Revision 1.1

Table 2. MCF5275RM Rev 1.1 Errata

Location	Description
Table 2-1/Page 2-5	FEC0_RXER and FEC1_RXER direction should be input, FEC0_TXEN and FEC1_TXEN direction should be output.
Table 2-1/Page 2-6	The GPIO signal name for the $\overline{\text{U1RTS}}$ entry should be swapped with $\overline{\text{U1CTS}}$. The same is true for $\overline{\text{U0RTS}}$ and $\overline{\text{U0CTS}}$ as well. Here are the correct assignments: $\overline{\text{U1CTS}}$: PUARTL5 $\overline{\text{U1RTS}}$: PUARTL4 $\overline{\text{U0CTS}}$: PUARTL1 $\overline{\text{U0RTS}}$: PUARTL0
Table 2-8/Page 2-12	FEC*n*_RXER direction should be input.
Table 7-3/Page 7-7	Footnote should read: “In 1:1 mode for the MCF5275, $f_{sys} = 2 \times f_{ref\_1:1}$”
Table 9-8/Page 9-8	Default output pad drive strength should be partial instead of full.
Table 9-8/Page 9-9	Footnote #2: Changed which pins do not affect reset configuration: “The D[31:26, 23:22, 18:17, 15:0] pins do not affect reset configuration.”
Table 12-1/Page 12-6	FEC0_RXER and FEC1_RXER direction should be input, FEC0_TXEN and FEC1_TXEN direction should be output.
Table 12-1/Page 12-7	The GPIO signal name for the $\overline{\text{U1RTS}}$ entry should be swapped with $\overline{\text{U1CTS}}$. The same is true for $\overline{\text{U0RTS}}$ and $\overline{\text{U0CTS}}$ as well. Here are the correct assignments: $\overline{\text{U1CTS}}$: PUARTL5 $\overline{\text{U1RTS}}$: PUARTL4 $\overline{\text{U0CTS}}$: PUARTL1 $\overline{\text{U0RTS}}$: PUARTL0
Table 12-15/Page 12-27	In bits 3–0 of the PAR_FECI2C register the settings for assigning the I2C_SDA and I2C_SCL pins to be UART2 transmit and receive functions are incorrect. Replace with the following bit settings table: **PAR_SDA** / **PAR_SCL** 00: GPIO / GPIO 01: U2RXD / U2TXD 10: GPIO / GPIO 11: I2C_SDA / I2C_SCL
Figure 12-45/Page 12-28	Combine bits 5–4 and bits 1–0 and rename the two fields to PAR_U1CTL and PAR_U0CTL respectively. Pinmuxing for the $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ signals cannot be controlled independently.

Table 2. MCF5275RM Rev 1.1 Errata (continued)

<table>
<tr><th>Location</th><th>Description</th></tr>
<tr><td>Table 12-16/Page 12-29</td><td>For bits 5–4 and 1–0, CTS and RTS pinmuxing for UART0 and UART1 cannot be controlled independently.
To enable the GPIO on U0CTS and U0RTS pins, PAR_UART[1:0] should be set to ‘00’; to enable primary function on these pins PAR_UART[1:0] should be set to '11’.
Similarly, to enable GPIO on U1CTS and U1RTS, PAR_UART[5:4] should be set to ‘00’; to enable primary function on these pins PAR_UART[5:4] should be set to ‘11’.
Combinations of ‘01’ and ‘01’ are not valid.
Therefore, the following table rows for bits 5–4 and 1–0 should be used:
<table>
<tr><th>Bits</th><th>Field</th><th>Description</th></tr>
<tr><td>5–4</td><td>PAR_U1CTL</td><td>U1CTS and U1RTS pin assignment. These two bits configure the U1CTS and U1RTS pins for primary function or GPIO.
00 U1CTS and U1RTS pins configured for GPIO
01 Reserved
10 Reserved
11 U1CTS and U1RTS pins configured for UART1 control functions.</td></tr>
</table>
<table>
<tr><th>Bits</th><th>Field</th><th>Description</th></tr>
<tr><td>1–0</td><td>PAR_U0CTL</td><td>U0CTS and U0RTS pin assignment. These two bits configure the U0CTS and U0RTS pins for primary function or GPIO.
00 U0CTS and U0RTS pins configured for GPIO
01 Reserved
10 Reserved
11 U0CTS and U0RTS pins configured for UART0 control functions.</td></tr>
</table>
</td></tr>
<tr><td>Section 13.2.1.6/Page 13-12</td><td>Include the text

It is the responsibility of the software to program the ICRnx registers with unique and non-overlapping level and priority definitions. Failure to program the ICRnx registers in this manner can result in undefined behavior. If a specific interrupt request is completely unused, the ICRnx value can remain in its reset (and disabled) state.

in section description and as a note in Figure 13.9.</td></tr>
<tr><td>Throughout Chapter 15</td><td>Replace instances of D[19:18] with D[20:19].</td></tr>
<tr><td>Figure 21-1/Page 21-2</td><td>Change value in divide by box to 4096 instead of 8192.</td></tr>
<tr><td>Figure 26-17/Page 26-18</td><td>Remove 16-bit divider blocks from both timer inputs, as it is not available when using an external clock source.</td></tr>
<tr><td>Section 26.4.1.2.2/Page 26-19</td><td>Change equation to: Baudrate = f_{extc}/(16 or 1), since the 16-bit divider is not available when using an external clock source.</td></tr>
<tr><td>Table 30-7/Page 30-15</td><td>Replace entries with “Bytes 5-7 + Parity” with “Bytes 5-8” to reduce confusion. The parity is included in the last bit of each byte, not the 8th byte.</td></tr>
</table>

3 Errata for Revision 1

Table 3. MCF5275RM Rev 1 Errata

Location	Description
Throughout	Remove overbar from DACK*n* signals, as they are not asserted low.
Throughout	Fix discrepancies regarding core and internal bus frequencies. Max core frequency is 166 MHz and max internal bus frequency is 83 MHz.
Throughout	Replace $\overline{\text{RSTI}}$ with $\overline{\text{RESET}}$ and $\overline{\text{RSTO}}$ with $\overline{\text{RSTOUT}}$.
Figure 2-1/Page 2-2	Remove VSTBY signal from figure.
Table 2-1/Page 2-3	Change $\overline{\text{RCON}}$ pin location for the 196 MAPBGA device from N11 to M6. Change USB_CLK pin location for the 196 MAPBGA device from G12 to F12. Change FEC0_TXCLK pin location for the 256 MAPBGA device from C1 to C3.
Table 2-15/Page 2-18	Added entry in table for PSTCLK output signal. “PSTCLK indicates when the development system should sample PST and DDATA values.”
Figure 3-7/Page 3-18	The reset value of D1[DCSIZ] is 0x0 and the reset value of D1[RAM1SIZ] is 0x8. Table 3-11 is correct.
Table 6-1/Page 6-3	In SPV bit field description, fix cross-reference to Section “Memory Base Address Register (RAMBAR)”. It should be Section 11.2.1.2 instead of 8.4.2.
Section 7.1.3.5/Page 7-6	The PLL cannot be stopped when the device enters stop mode. Remove paragraphs 3-6 and add in their place “During stop mode, the PLL continues to run. The external CLKOUT signal may be enabled or disabled when the device enters stop mode, depending on the LPCR[STPMD] bit settings. The external CLKOUT output pin may be disabled to lower power consumption via the SYNCR[DISCLK] bit. The external CLKOUT pin function is enabled by default at reset.”
Table 7-5/Page 7-9	The first equation in footnote #1 in the MFD bit description field is incorrect. It should be: “$f_{sys} = f_{ref} \times 2(MFD + 2)/2^{RFD}$” instead of $f_{sys/2}$.
Table 7-5/Page 7-9	The second equation in footnote #1 in the MFD bit description field is incorrect. It should be: “$f_{ref} \times 2(MFD + 2) \leq 166MHz$” instead 83MHz
Section 7.4.3/Page 7-15	First paragraph, the default core frequency is one and a half times the reference frequency after reset instead of two times the reference frequency. An MFD = 0b001 is 6x not 2x.
Table 7-11/Page 7-30	Delete 4th and 5th rows on this page, as the PLL cannot be disabled in stop mode.
Table 8-4/Page 8-4	The description of bits 2-0 is missing from the LPCR Field Description table. These should be included with the following description: “Reserved, should be cleared.”
Section 8.3.2.3/Page 8-6	Corrected second paragraph since the core watchdog cannot reset the device. Second paragraph should read “When enabled, the core watchdog can bring the device out of low-power mode via a core watchdog interrupt. This system setup must meet the conditions specified in Section 8.3.1, “Low-Power Modes” for the core watchdog interrupt to bring the part out of low-power mode.
Section 8.3.2.16/Page 8-10	The PLL cannot be stopped when the device enters stop mode. Remove paragraphs 2-5 and add in their place “During stop mode, the PLL continues to run. The external CLKOUT signal may be enabled or disabled when the device enters stop mode, depending on the LPCR[STPMD] bit settings.”
Table 9-1/Page 9-2	Reset config override signals should be D[25:24, 21:19, 16] instead of D[26:24, 21, 19:16].
Section 9.2.3/Page 9-2	Section title should be “D[25:24, 21:19, 16]...” instead of “D[26:24, 21, 19:16]...”

Table 3. MCF5275RM Rev 1 Errata (continued)

<table>
<tr><th>Location</th><th>Description</th></tr>
<tr><td>Figure 9-2/Page 9-4</td><td>Change the CCR[LOAD] bit to reserved, as it is not functional on the device.
Change reset value to 0x0028.</td></tr>
<tr><td>Table 9-4/page 9-4</td><td>Remove the CCR[LOAD] bit.</td></tr>
<tr><td>Figure 9-3/Page 9-5</td><td>Unreserved RCON register bits should be read only.</td></tr>
<tr><td>Table 9-7/Page 9-8</td><td>Reset config override signals should be D[25:24, 21:19, 16] instead of D[26:24, 21, 19:16].</td></tr>
<tr><td>Table 9-8/Page 9-8</td><td>Chip mode heading should be D16 only, since D26 & D17 have no affect on the selected chip mode. Master mode (default) is selected by asserting D16. Deasserting D16 during $\overline{\text{RCON}}$ assertion at reset places the device in a reserved mode.</td></tr>
<tr><td>Table 9-8/Page 9-8</td><td>Remove “RCON[2]=0” in boot device default configuration field.</td></tr>
<tr><td>Table 9-8/Page 9-9</td><td>“Chip select configuration“ entry for setting D[25:24]=11, should read “PADDR[7:5] = $\overline{\text{CS}}$[6:4]” instead of “PADDR[7:6] = $\overline{\text{CS}}$[6:4]”</td></tr>
<tr><td>Table 9-8/Page 9-9</td><td>Remove “RCON[7:6]=10” from clock mode default configuration field. Footnote added: “There is no default configuration for clock mode selection. The actual values for the CLKMOD pins must always be driven during reset. Once out of reset, the CLKMOD pins have no effect on the clock mode selection.”</td></tr>
<tr><td>Table 9-8/Page 9-9</td><td>Footnote #2: Changed which pins do not affect reset configuration: “The D[31:26, 23:22, 20:17] pins do not affect reset configuration.”</td></tr>
<tr><td>Section 9.4.2/Page 9-9</td><td>The MODE field is in the RCON register instead of the CCR.</td></tr>
<tr><td>Table 9-9/Page 9-9</td><td>Remove MODE[2] and MODE[1] columns since the MODE field is only one bit wide and also D26 and D17 have no affect on chip configuration mode selection.</td></tr>
<tr><td>Table 13-13/Page 13-15</td><td>The interrupt source assignment for the USB sources in incorrect. They should be as follows:
<table>
<tr><th>Source</th><th>Module</th><th>Flag</th><th>Source Description</th><th>Flag Clearing Mechanism</th></tr>
<tr><td>43</td><td>USB</td><td>USB</td><td>USB Interrupt</td><td>writing a ’1’ to the appropriate bit in USB_INTR</td></tr>
<tr><td>44</td><td></td><td>EP0</td><td>Endpoint 0</td><td>writing a ’1’ to the appropriate bit in USB_EP0_INTR</td></tr>
<tr><td>45</td><td></td><td>EP1</td><td>Endpoint 1</td><td>writing a ’1’ to the appropriate bit in USB_EP1_INTR</td></tr>
<tr><td>46</td><td></td><td>EP2</td><td>Endpoint 2</td><td>writing a ’1’ to the appropriate bit in USB_EP2_INTR</td></tr>
<tr><td>47</td><td></td><td>EP3</td><td>Endpoint 3</td><td>writing a ’1’ to the appropriate bit in USB_EP3_INTR</td></tr>
</table></td></tr>
<tr><td>Figure 14-9/Page 14-16</td><td>DACKn is only asserted for a single clock cycle. All other signals (TS, CS, TA, R/$\overline{\text{W}}$, and A[23:0] are subsequently moved one cycle sooner.</td></tr>
<tr><td>Section 15.2.1/Page 15-1</td><td>An overbar should be placed over the CS[7:0] in the section heading.
The last sentence should read: “Port size for $\overline{\text{CS0}}$ is configured by the logic levels of D[20:19] when $\overline{\text{RSTOUT}}$ negates and $\overline{\text{RCON}}$ is asserted.”</td></tr>
<tr><td>Table 15-6/Page 15-8</td><td>In the CSMRn[BAM] bit description, the first example BAM bit setting is incorrect. Change from 0x0008 to 0x0001.</td></tr>
</table>

Table 3. MCF5275RM Rev 1 Errata (continued)

Location	Description
Table 17-8/Page 17-17	In the RCNT field description, the last line of the example should be: RCNT = floor(5 × 83/64) - 1 =0x04 Correct CLKOUT value and move closing parenthesis.
Table 17-9/Page 17-18	PRE2ACT bit field description; $t_{DDRCLKOUT}$ is incorrect. Should be 1/83 MHz.
Section 17.7/Page 17-23	Change “75MHz DDR_CLKOUT frequency” to “83MHz DDR_CLKOUT frequency (12ns period)”.
Throughout Section 17.7	Correct t_{DDR_CLKOUT} in all equations; should be 12ns instead of 8.3ns. This affects the table entries as well as the actual values calculated for the registers.
Table 17-20/Page 17-29	Correct BLEN entry. Burst length can only be 8, BLEN = 111.
Table 17-23/Page 17-32	Correct BLEN entry. Burst length can only be 8, BLEN = 111.
Chapter 19	The maximum buffer size of the FEC is 2032 bytes. Replace all instances of 2047 with 2032. R_BUF_SIZE is at bit position 10:4 in the EMRBR register. Therefore the maximum setting is $7F0 which equals 2032.
Figure 19-24/Page 19-28	Change the EMRBR*n* register addresses to “IPSBAR + 0x1188 (FEC0) & IPSBAR + 0x1988 (FEC1)” instead of “IPSBAR + 0x11B8 (FEC0) & IPSBAR + 0x19B8 (FEC1)”.
Figure 20-6/Page 20-9	DADR field is only 10 bits wide (USB_DAR[9:0]) not 11 bits. Correct figure and corresponding bit description table.
Table 24-3/Page 24-6	The MODE16 bit field description should read: “Selects the increment mode for the timer. MODE16 = 1 is intended to exercise the upper bits of the 32-bit timer in diagnostic software without requiring the timer to count through its entire dynamic range. When set, the counter’s upper 16 bits mirror its lower 16 bits. All 32 bits of the counter are still compared to the reference value.”
Section 24.3.2/Page 24-11	Correct example for 83 MHz.
Section 28.4.1/Page 28-15	Swap steps 4 & 5 and change “...(without padding) in bits” to “...(without padding) in bytes”.
Section 28.4.2.1/Page 28-16	Swap steps 4 & 5.
Section 28.4.2.2/Page 28-16	Swap steps 4 & 5.
Section 28.4.2.3/Page 28-17	Swap steps 8 & 9.
Section 28.4.3/Page 28-18	Swap steps 8 & 9.
Section 28.4.4/Page 28-18	Swap steps 6 & 7.
Section 28.4.5/Page 28-18	Swap steps 7 & 8.
Figure 30-8/Page 30-7	Change SKMR[CTRM] bit field to straddle bits 11–8.
Table 30-2/Page 30-8	Change the first 4 SKMR bit fields bit numbers to 31–12, 11–8, 7, & 6–5.
Section 30.3.1/Page 30-19	Remove last sentence of section, as this refers to internal logic only.
Section 30.4.1/Page 30-20	Swap steps 9 & 10.
Section 30.4.2/Page 30-20	Swap steps 9 & 10. Swap steps 23 & 24.
Table 32-1/Page 32-2	Change CLKOUT to PSTCLK.
Figure 32-2/Page 32-2	Change CLKOUT to PSTCLK.
Figure 32-41/Page 32-48	Change pin 24 from CLKOUT to PSTCLK.

4 Revision History

Table 4 provides a revision history for this document.

Table 4. Revision History Table

Rev. Number	Substantive Changes	Date of Release
1.0	• Initial release.	11/2004
1.1	• Added D1 reset value errata. • Added FEC max buffer size errata.	01/2005
1.2	• Added FEC EMRBR*n* address errata.	03/2005
1.3	• Added core and internal bus frequency errata. • Added $\overline{\text{RSTI}}$/$\overline{\text{RSTO}}$ errata. • Added VSTBY errata. • Added multiple PSTCLK errata. • Added SPV bit field cross-reference errata. • Added multiple errata regarding the PLL unable to be stopped during stop mode. • Added MFD bit field errata. • Added Section 7.4.3 default core frequency errata. • Added CCR[LOAD] bit errata. • Added core watchdog reset errata. • Added chip select configuration entry errata. • Added USB interrupt source number errata. • Added CSMR*n*[BAM] example errata. • Added RCNT field description equation errata. • Added t_{DDR_CLKOUT} errata. • Added BLEN errata. • Added USB_DAR[DADR] bit field length errata. • Added DMA Timer MODE16 bit errata. • Added DMA Timer example errata. • Added MDHA & SKHA application examples errata. • Added the SKMR[CTRM] bit field errata.	04/2005
The below errata were added for MCF5275RM Revision 1.1		
1.4	• Added D[19:18]->D[20:19] errata. • Corrected previous errata with Table 9-8, Footnote #2	07/2005
1.5	• Added ERXER and ETXER direction errata in Chapter 2 and 12. • Added default output pad drive strength • Added Table 7-3 footnote errata. • Added SKHA parity errata. • Added UART external clock source, 16-bit divider errata.	08/2005
1.6	• Added GPIO signal names for the UART control signals errata. • Added PAR_FECI2C's I2C_SDA and I2C_SCL bit setting error.	11/2005
1.7	• Added PAR_UART register errata for the UART0 and UART1 control signals.	12/2005
1.8	• Added ICR*n*x note regarding unique and non-overlapping level and priority definitions. • Added watchdog timer divide-by value errata.	07/2006

Table 4. Revision History Table (continued)

Rev. Number	Substantive Changes	Date of Release
The below errata were added for MCF5275RM Revision 2		
2.1	• Added RMON_R_DROP counter errata. • Added SDCR[DQS_OE] note errata. • Added SDCFG1 section notes. • Added SDCFG1[SRD2RW] description errata. • Added DDR example errata.	11/2006
2.2	• Added various core, EMAC, cache, SRAM and debug chapter errata. • Added CLKIN to CLKOUT errata. • Added FEC MIB counter memory map errata. • Added “Duplicate Frame Transmission” section to FEC chapter. • Added secondary wait state timing diagram errata. • Added SKMR[CTRM,DKP] errata. • Added CIM/CCM errata. • Added EPDDR figure errata. • Added DMA figure overbars errata. • Added DMA figure errata. • Added SDRAM’s BWT2RW equation errata. • Added DMA external request and acknowledge operation section errata. • Added DMA SAA bit errata. • Added interrupt level/priority table. • Added IPSBAR note in SCM chapter. • Added global IACK space errata.	05/2007

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