

Freescale Semiconductor Reference Manual Addendum

MCF52259RMAD Rev. 1, 12/2011

MCF52259 Reference Manual Errata

by: Microcontroller Solutions Group

This errata document describes corrections to the *MCF52259 Reference Manual*, order number MCF52259RM. For convenience, the addenda items are grouped by revision. Please check our website at http://www.freescale.com for the latest updates.

The current available version of the *MCF52259 Reference Manual* is Revision 4.

Table of Contents

1	Errata for Revision 4	2
2	Revision History	3





Errata for Revision 4

1 Errata for Revision 4

Table 1. MCF52259 Reference Manual Rev. 4 Errata

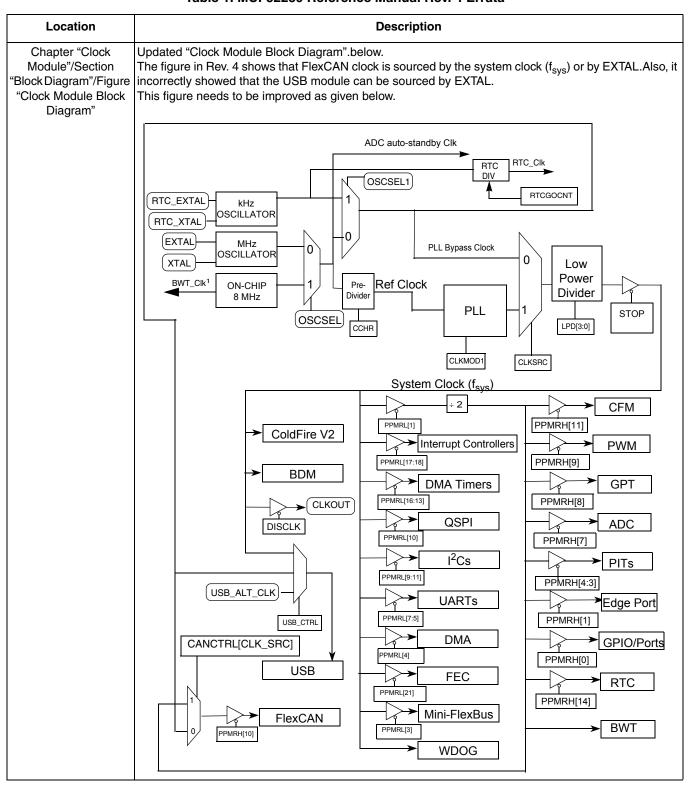




Table 1. MCF52259 Reference Manual Rev. 4 Errata (continued)

Location	Description
Chapter "Universal Serial Bus,OTG Capable Controller "/Section "USB Control Register(USB_CTRL)" /Table"USB_CTRL field descriptions"	In Table "USB_CTRL field descriptions", in field "1-0 CLK_SRC", the clock source is incorrectly described as follows: 00 USB_ALT_CLK pin (External clock that can feed in from PTG0) 01 External OSC on EXTAL pin 10 Reserved 11 System clock source (MCGPLLSCLK) It should be as follows: 00 USB_ALT_CLK pin (External clock that can feed in from PTG0) 01 PLL Bypass Clock 10 Reserved 11 System clock source (f _{sys})
Chapter "FlexCAN"/Section "FlexCAN Control Register (CANCTRL)"/Table "CANCTRL field descriptions"/Equation 32-1	In Equation 32-1, the S clock frequency equation is incorrectly shown as $S \ clock \ frequency = \frac{f_{SVS} \ or \ EXTAL}{PRESDIV + 1}$ It should be as follows: $S \ clock \ frequency = \frac{f_{SVS/2} \ or \ PLL \ bypass \ clock}{PRESDIV + 1}$
Chapter "FlexCAN"/Section "FlexCAN Control Register (CANCTRL)"/Table "CANCTRL field descriptions"	In Table "CANCTRL field descriptions", bit 13 "CLK_SRC", the clock source is incorrectly described as 0 Clock source is EXTAL 1 Clock source is the internal bus clock, f _{sys} It should be as follows: 0 Clock source is PLL bypass clock 1 Clock source is the internal bus clock, f _{sys/2}
Chapter "FlexCAN"/Section "FlexCAN Control Register (CANCTRL)"/Figure "CAN engine clocking scheme"	In Figure "CAN engine clocking scheme "Oscillator Clock (EXTAL)" needs to be changed to PLL bypass clock In Equation 32-6, a. fsys needs to be changed to f _{sys/2} b. "EXTAL" needs to be changed to PLL bypass clock

2 Revision History

Table 2 provides a revision history for this document.

Table 2. Revision History Table

Rev. Number	Substantive Changes	Date of Release
1.0	Initial release. Incorporated changes in the following chapters: Clock Module Universal Serial Bus, OTG Capable Controller FlexCAN	12/2011

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MCF52259RMAD Rev. 1 12/2011