Freescale Semiconductor, Inc.

MOTOROLA

*Microprocessor and Memory
Technologies Group*

MC68306

UPDATE TO
MC68306 Integrated EC000 Processor User's Manual

October 7, 1995

This update to the initial release of the MC68306UM/AD User's Manual and the MC68306UMAD/AD User's Manual Addendum provides corrections to the original text, plus additional information not included in the original. This document and other information on this product is maintained on the AESOP BBS, which can be reached at (800)843-3451 (from the US and Canada) or (512)891-3650. Configure the modem for up to 14.4K baud, 8 bits, 1 stop bit, and no parity. Terminal software should support VT100 emulation. Internet access is provided by telneting to pirs.aus.sps.mot.com [129.38.233.1] or through the World Wide Web at http://pirs.aus.sps.mot.com.

1. System Register Naming Conventions

In section 5, pages 5-1 through 5-17, none of the registers have standardized abbreviations. Below is a table which provides the abbreviated names for all of the MC68306 system registers. These are the standard names that will be used in assembly and C header files. Some registers have 32-bit names and two 16-bit names which overlap the upper and lower, (High and Low) 16 bits of the register.

Address	Abbreviation	Name
FFFFFFC0/1/2/3	CSC0	Chip Select Configuration Register 0
FFFFFFC0/1	CSC0H	Chip Select Configuration Register 0 (High Half)
FFFFFFC2/3	CSC0L	Chip Select Configuration Register 0 (Low Half)
FFFFFFC4/5/6/7	CSC1	Chip Select Configuration Register 1
FFFFFFC4/5	CSC1H	Chip Select Configuration Register 1 (High Half)
FFFFFFC6/7	CSC1L	Chip Select Configuration Register 1 (Low Half)
FFFFFFC8/9/A/B	CSC2	Chip Select Configuration Register 2
FFFFFFC8/9	CSC2H	Chip Select Configuration Register 2 (High Half)
FFFFFFCA/B	CSC2L	Chip Select Configuration Register 2 (Low Half)
FFFFFFCC/D/E/F	CSC3	Chip Select Configuration Register 3
FFFFFFCC/D	CSC3H	Chip Select Configuration Register 3 (High Half)
FFFFFFCE/F	CSC3L	Chip Select Configuration Register 3 (Low Half)
FFFFFFD0/1/2/3	CSC4	Chip Select Configuration Register 4
FFFFFFD0/1	CSC4H	Chip Select Configuration Register 4 (High Half)
FFFFFFD2/3	CSC4L	Chip Select Configuration Register 4 (Low Half)
FFFFFFD4/5/6/7	CSC5	Chip Select Configuration Register 5

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FFFFFFD4/5	CSC5H	Chip Select Configuration Register 5 (High Half)
FFFFFFD6/7	CSC5L	Chip Select Configuration Register 5 (Low Half)
FFFFFFD8/9/A/B	CSC6	Chip Select Configuration Register 6
FFFFFFD8/9	CSC6H	Chip Select Configuration Register 6 (High Half)
FFFFFFDA/B	CSC6L	Chip Select Configuration Register 6 (Low Half)
FFFFFFDC/D/E/F	CSC7	Chip Select Configuration Register 7
FFFFFFDC/D	CSC7H	Chip Select Configuration Register 7 (High Half)
FFFFFFDE/F	CSC7L	Chip Select Configuration Register 7 (Low Half)
FFFFFFE0/1/2/3	DBC0	DRAM Bank Configuration Register 0
FFFFFFE0/1	DBC0H	DRAM Bank Configuration Register 0 (High Half)
FFFFFFE2/3	DBC0L	DRAM Bank Configuration Register 0 (Low Half)
FFFFFFE4/5/6/7	DBC1	DRAM Bank Configuration Register 1
FFFFFFE4/5	DBC1H	DRAM Bank Configuration Register 1 (High Half)
FFFFFFE6/7	DBC1L	DRAM Bank Configuration Register 1 (Low Half)
FFFFFFF0	PADAT	Port A Data Register
FFFFFFF1	PBDAT	Port B Data Register
FFFFFFF2	PADDR	Port A Data Direction Register
FFFFFFF3	PBDDR	Port B Data Direction Register
FFFFFFF4	PAPR	Port A Pins Register
FFFFFFF5	PBPR	Port B Pins Register
FFFFFFF8/9	ISR	Interrupt Status Register
FFFFFFFA/B	ICR	Interrupt Control Register
FFFFFFFC	DREF	DRAM Refresh Register
FFFFFFFD	BTPR	Bus Timeout Period Register
FFFFFFFE	SYSR	System Register
FFFFFFFF	TVR	Timer Vector Register

These names should be added to each of the register section titles. All tables should also reflect the standardized naming conventions. Below are some example title changes:

5.2.3   Bus timeout Period Register (BTPR)
5.2.5.1 Port Pins Register (PxPR)
5.2.7.2 DRAM Bank Configuration Register (High Half) (DBCxH)

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