Wireless Base Station Transceiver: Baseband Processing

Overview

Today's networking infrastructure systems are characterized by separate voice, fax, and data subsystems over independent real-time voice (circuit switched) and data (packet) networks. The industry is moving to next generation systems that are based on a configurable open architecture platform supporting a universal port combination of real-time voice, fax, and data on a packet-switched network.

The baseband functionality of a Wireless Base Station Transceiver includes:

> Separating received signals into channels by combining correct time slots or coded messages

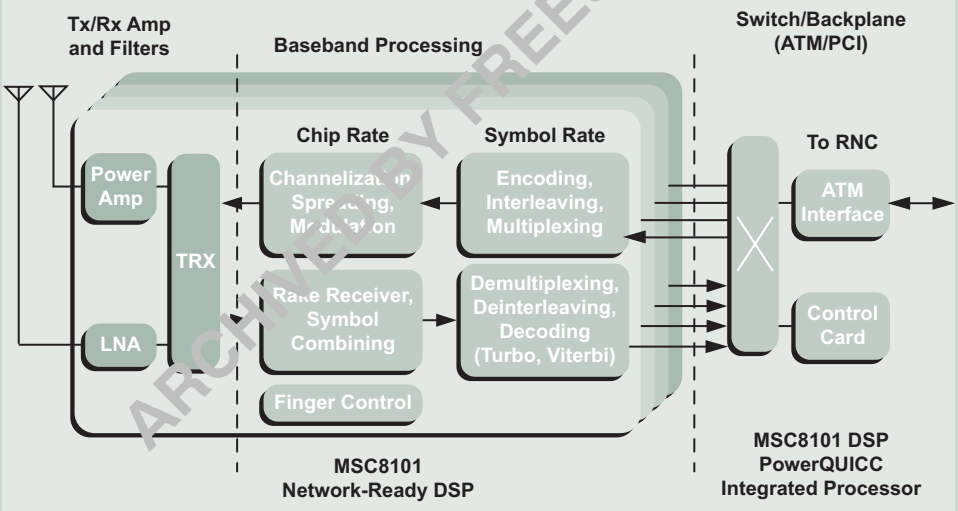
> Sending these signals to the Base Station Controller for compression

> Changing to another channel when directed by the BSC

> Converting channels back into analog, combining multiple voice channels, up-converting to IF, filtering, and amplifying signals for transmission to mobile subscribers

As demand for mobile services beyond voice drives next-generation data primary systems, the base station must handle the more complex processing, modulation, and coding requirements of significantly-higher data rates and the new air interface schemes which support them.

2G/3G WIRELESS NETWORK DIAGRAM



Key Benefits

> High-performance silicon, software, and design tools support complex processing and high data rates

> Power-efficient architecture

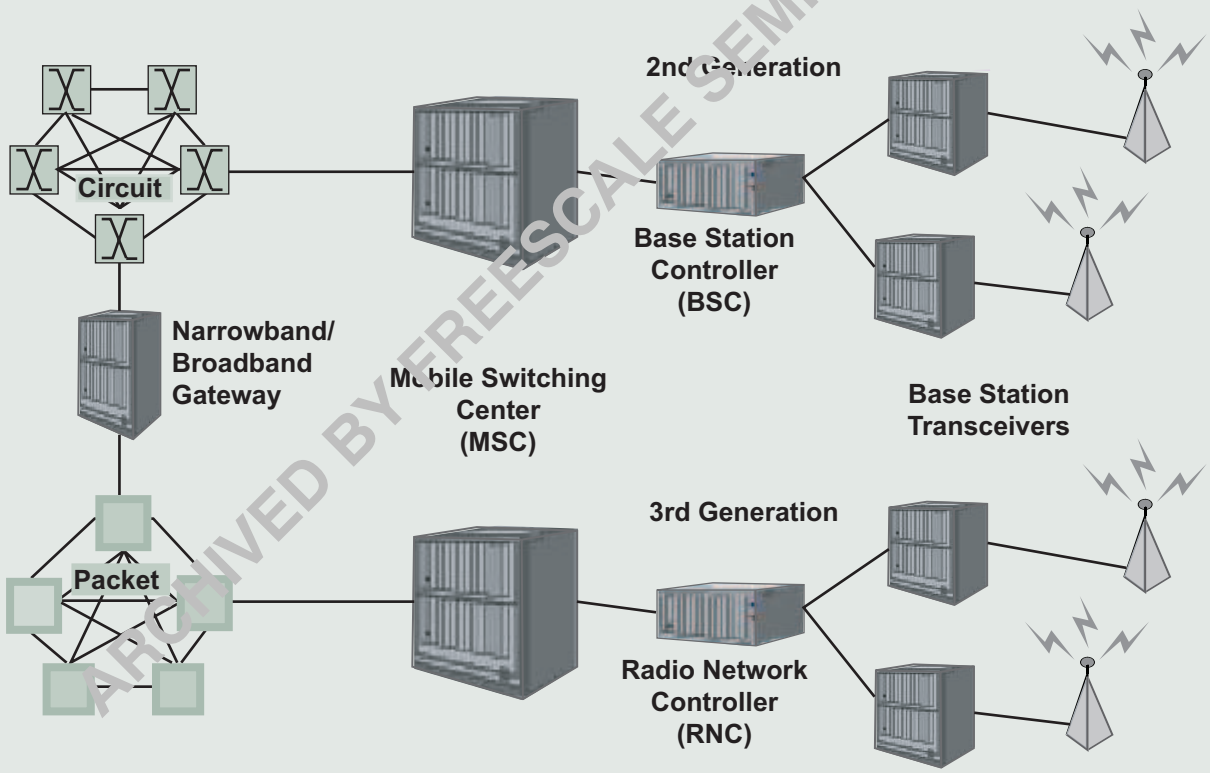
Freescale Ordering Information

Part Number	Product Highlights	Additional Information
XC8101M1375C	332-Pin FC-BGA package; 275 MHz; 1375 MMACS; 137 MHz CPM, 63 MHz System Bus; 275 MHz EFCOP	1.6 V core, 3.3 V I/O; 512K-bytes unified program and data memory configurable by the application, 4 ALUs, EFCOP, CPM, System Integration Unit. 16-channel DMA, 64-bit 60x compatible system bus. Suited for networking infrastructure applications such as 2.5G and 3G wireless infrastructure, IP telephony (voice, fax, modem, and video IP gateways). ATM Edge/Carrier switching and transmissions and centralized DSP services (compression and echo cancellation).
XC56321FC200	196-Pin FC-BGA package; 200 MHz; 400 MMACS; 200 MHz EFCOP	1.6 V core, 3.3 V I/O; 576K-bytes of on-chip memory (32-112K words program; 160-80K words data); 8 memory switch options; optional 1K words instruction cache
XPC8260 PowerQUICC II	CPU/CPM/Bus Speed (MHz); 166/133/66 (HFB); 200/133/66 (IFB); 200/166/66 (IHB)	Supports fast Ethernet HDLC channels and OC-3 ATM up to 200 MHz CPU, 166 MHz CPM, 66 MHz Bus

Design Challenges

As networks move from circuit switched to packet switched, base station solutions must support the intense demands of next-generation telecommunications. Today's fixed-platform systems often have closed proprietary architectures. Next-generation systems will be based on a configurable open architecture platform that supports a universal port combination of real-time voice, fax, and data on a packet-switched network. Chip-rate and symbol-rate processing in these systems demand very high-performance digital signal processors (DSPs). In addition, the network interface to the radio network controller (RNC)—ATM and T1/E1—requires support for industry standard broadband protocols.

NEXT-GENERATION WIRELESS BASE STATION BLOCK DIAGRAM



Freescale Semiconductor Solution

To meet the needs of the wireless market, Freescale Semiconductor believes it is vital to provide more than silicon to our customers. The building blocks for tomorrow's solutions include silicon, software, and design tools.

Signal Processing

Freescale Semiconductor offers two DSP architectures to meet baseband processing requirements for the base station transceiver:

> The SC140 is the quad arithmetic logic unit (ALU) StarCore architecture that is used in Freescale Semiconductor's MSC810x DSP family:
  - MSC8101, with up to 1500 MMACS of performance, integrates an on-chip 32-bit RISC protocol machine, allowing connectivity to standard network backbones such as ATM, fast Ethernet, and fast TDM highways.
  - MSC8102 consists of four SC140 cores featuring up to 6000 MMACS of performance and 1436KB of on-chip static RAM (SRAM) memory.

  The SC140 core features 1200 MMACS of performance. It is high-level-language friendly and features a comprehensive set of software tools. Application software modules for GSM, CDMA, and TDMA vocoders, and 3G cellular infrastructure are available from Freescale Semiconductor and third-party vendors.

> 24-bit DSP56300 DSP family devices are widely used today in multi-channel voice and data products (up through 2.5G). These pin-compatible DSPs enable customers to rapidly implement new telecommunications standards and bring new products to market.

Network Interface

Network interface and station control requirements may also be served by the PowerQUICC™ family of integrated communications processors, which pioneered the dual-processor architecture:

> A core ISA CPU handles system tasks with a variety of onboard peripherals and a standard bus interface.

> A specially designed RISC communication processor, with integrated support for multiple protocols, manages serial communication channels.

This architecture significantly enhances system performance and efficiency and saves on power consumption. In addition, the established code base and broad third-party support from Freescale Semiconductor's Smart Network Alliance Program members further enable cost-efficient solutions and accelerated time-to-market for base station equipment suppliers.

Development Tools

Tool Type	Product Name	Vendor	Description
RTOS and API	OSE RTOS RTXC	OSE Systems (www.enea.com) Lineo (www.lineo.com)	RTOS and API
Software Development, Integration, and Debug Environment	MULTI CodeWarrior StarCore C++/C software Development Tool Suite Tornado	Green Hills (www.ghs.com) Metrowerks (www.metrowerks.com) TASKING (www.tasking.com) Wind River Systems (www.windriver.com)	Software Development, Integration, and Debug Environment
Co-Simulation	Signal Processing Worksystems (SPW) N2C Design System Seamless Coverification	Cadence (www.cadence.com) CoWare (www.coware.com) Mentor Graphics (www.mentorgraphics.com)	Co-Simulation
System Level Modeling and Simulation	System Level Design N2C Design System MATLAB, Simulink COSSAP	Cadence (www.cadence.com) CoWare (www.coware.com) Matlab (www.matlab.com) Synopsys (www.synopsys.com)	System Level Modeling and Simulation
Device Simulator	PrimeLayer Communications Suite	PrimeLayer Software, Inc. (www.primelayer.com)	Device Simulator
Hardware Development Environment	MSC8101ADS	Metrowerks (www.metrowerks.com)	Hardware Development Environment
Device Driver Software	DriveWay-MSC8101 PrimeLayer Communications Suite	Aisys (www.aisysinc.com) PrimeLayer Software, Inc. (www.primelayer.com)	Device Driver Software

Third Party Support

Vendor	Product	Contact Information
Signals and Software Limited	Embedded commu-nications software including speech coders, modems and echo cancellers for applications such as cellular and PCS telephones, pagers, and wireless base stations.	www.sasl.com
Lake Communications	Lake Genus Suite of DSP algorithms provides many common modem and vocoder combinations using a common API, enabling easy integration into products.	www.lakecommunications.com

Notes

Learn More: Contact the Technical Information Center at +1-800-521-6247 or +1-480-768-2130.
For more information about Freescale products, please visit **www.freescale.com**.

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