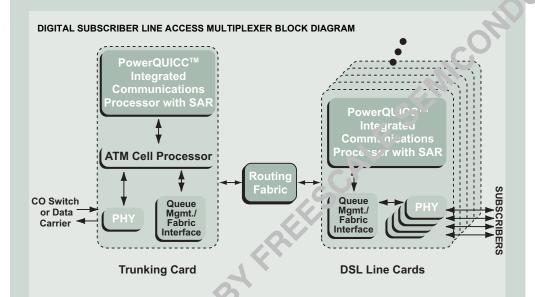
# Digital Subscriber Line Access Multiplexer (DSLAM)

### Overview

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The digital subscriber line access multiplexer (DSLAM) is a network element defined to support high-bandwidth access to the public network. With the ability to support data and voice services over existing subscriber lines, the DSLAM can assist local phone service providers and ISPs in minimizing cost while maximizing efficiency of their networks. Multiplexing technology, based on time division multiplexing (TDM), or switch-based schemes like frame relay, IP, or ATM, reduces the number of physical connections to the backbone.



#### Key Benefits

- > Supports transmission voice and data <u>over</u> existing twisted-pair copper infract, upture using DSL transpeivers
- Separates voice from data, routing them onto separate networks
- Internet access, remote work station LAN/WAN access, frame relay, and native ATM all supported with DSLAM
- > Serves as a VPN gateway
- > Subscriber side of xDSL solution considered a security gateway



Freescale Ordering Information

Freescale Oru	ering mormation		
MPC850	PowerQUICC Integrated Communications Processor	<ul> <li>&gt; 80MHz maximum speed</li> <li>&gt; 2K-bytes cache-L1 instructional</li> <li>&gt; 1K-byte cache-L1 data</li> <li>&gt; 8-entry translation look aside buffers</li> </ul>	www.freescale.com/netcomm
MPC857T	PowerQUICC Integrated Communications Processor	<ul> <li>&gt; 80MHz maximum speed</li> <li>&gt; 4K-bytes cache-L1 Instructional</li> <li>&gt; 4K-bytes cache-L1 data</li> <li>&gt; 59 parallel bits</li> </ul>	www.freescale.com/netcomm
MPC860	PowerQUICC Integrated Communications Processor	<ul> <li>&gt; 80MHz maximum speed</li> <li>&gt; 4K-bytes cache-L1 instructional (DE, DT, EN, SR, and T)</li> <li>&gt; 16K-byte cache-L1 instructional (DP and P)</li> <li>&gt; 4K-byte cache-L1 data (DE, DT, EN, SR, and T)</li> <li>&gt; 8K-byte cache-L1 data (DP and P)</li> <li>&gt; 32-entry translation look aside buffers</li> </ul>	www.freescale.cc m, het.omm
MPC862	PowerQUICC Integrated Communications Processor	<ul> <li>&gt; Enhanced ATM functionality</li> <li>&gt; New features available in "enhanced SAR" (ESAR) model</li> </ul>	v ww.freescale.com/netcomm

## Design Challenges

The combination of interfaces and services present a difficult challenge to DSLAM implementation, especially in light of time-to-market constraints. In the asynchronous traffic mode (ATM)-based DSLAM, the interface between the DSLAM and the network will be an official carrier (OC) level-12 (OC-12), OC-3, or DS3, compliant with the ATM Forum's UNI specification. The DSLAM should support statistical multiplexing, traffic management (TM), cell buffering, cell queuing, priority schemes, and fairness algorithms in accordance with the ATM Forum's TM specification.

Traditional approaches require separate hardware and general purpose CPUs for each interface type and protive if resulting in many individual designs, along with limited reusation software. In addition, designers and termination of VPN (IPSec) tunates.

## Freescale Serviconductor Solution Freescale Semiconductor's

PowerQUICC<sup>™</sup> Integrated Communications Processors feature a unique dual-processor architecture, a core CPU compliant with the PowerPC instruction-set architecture that handles system tasks with a variety of on-board peripherals, and a standard bus interface. Additionally, they feature a specially designed RISC communications processor with integrated support for multiple proceeds to manage serial communications channels. All members of procescale Semiconductor's leading PowerQUICC II family of integrated communications processors are easily upgraded through download microcode packages. These innovative proceed packages provide the ideal mix of control and data plane functionality, enabling our customers to resuce time-to-market by focusing on ralue-added product elements.

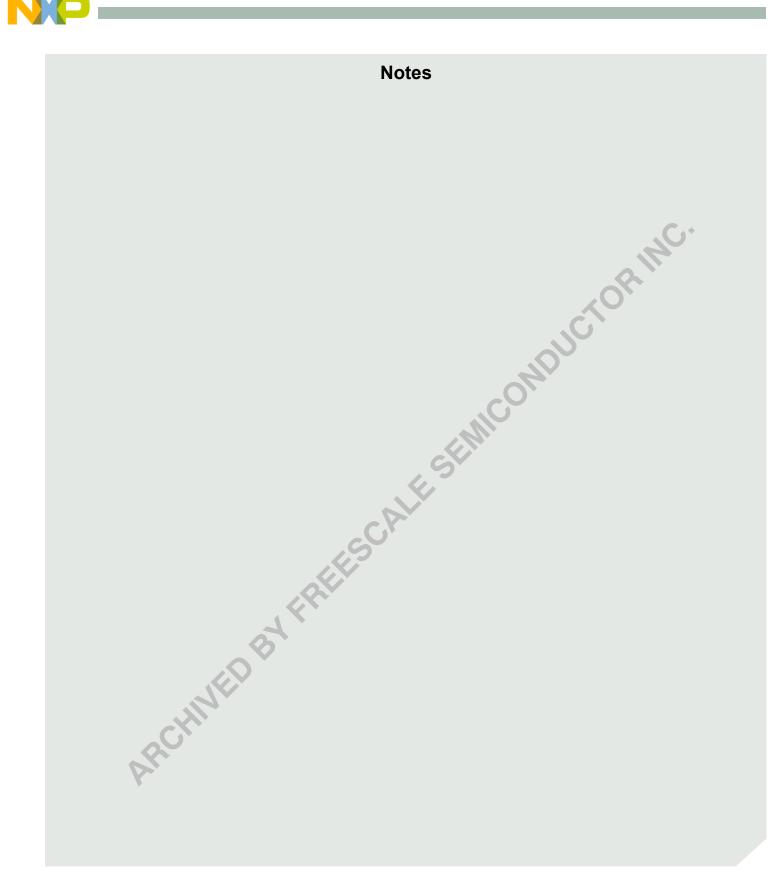
This architecture significantly enhances system performance, security and efficiency, saving energy consumption, up to full rate OC-3 VPN (IPSec) support through the use of a MPC185 Security Processor. The MPC185 Security Processor is easily integrated into PowerQUICC II systems via the 60x bus. The MPC185 achieves high performance through 60x bus mastering and immediate access to system memory. By avoiding data transfers across bridges and secondary buses, the MPC185 provides PowerQUICC II system designers with the ultimate security chip set for midrange VPN and DSLAM applications.

The Figure shown on page 1 illustrates the trunking card connecting the DSLAM to the central office ATM switch for data services and to the Public Switched Telephone Network (PSTN) for voice services. The PowerQUICC Integrated Communications Processor handles call setup, tear-down, and card management functions. If the control path requires a low-bit-rate segmentation and reassembly (SAR) function to support CO-to-DSLAM signaling or intra-DSLAM communications, several PowerQUICC family members integrate this important function to offer cost-effective, and highly integrated solutions.

> The DSL line card provides the subscriber interface to the DSLAM. Its anatomy is very similar to the trunking card, providing many of the same features, so the PowerQUICC II family is also an ideal solution. For applications requiring less than full rate, full duplex OC-3 performance, PowerQUICC with multi-service platform (MSP) microcode allows most ATM switching functionality inside the device, significantly lowering design cost.



		Description	
lardware MPC8XXFADSMB	Freescale Semiconductor	For MPC8xx Fam	ily Application Development System Motherboard
Development MPC8260ADS-P	Freescale Semiconductor	MPC8260 Application Development System	
owerQUICC Integrated ommunications Processors MPC850 family, including the MPC850SR MPC857T with enhanced ATM support	<ul> <li>MPC860 family, inclu MPC860SAR</li> <li>MPC862 with enhance</li> <li>MPC8255, MPC8260 MPC8265 and MPC8 PowerQUICC II next- family</li> </ul>	ced ATM support 0, MPC8264, 8266	<ul> <li>PowerQUICC and PowerQUICC II microcodes packages provide enhanced forwarding plane features MPC180/184/185 Security Processors.</li> </ul>
Related Documentation			A O
	Description		
G1007	Network and Communications Processors	Product Selector Guide	
	Software and Development Tools Product		



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