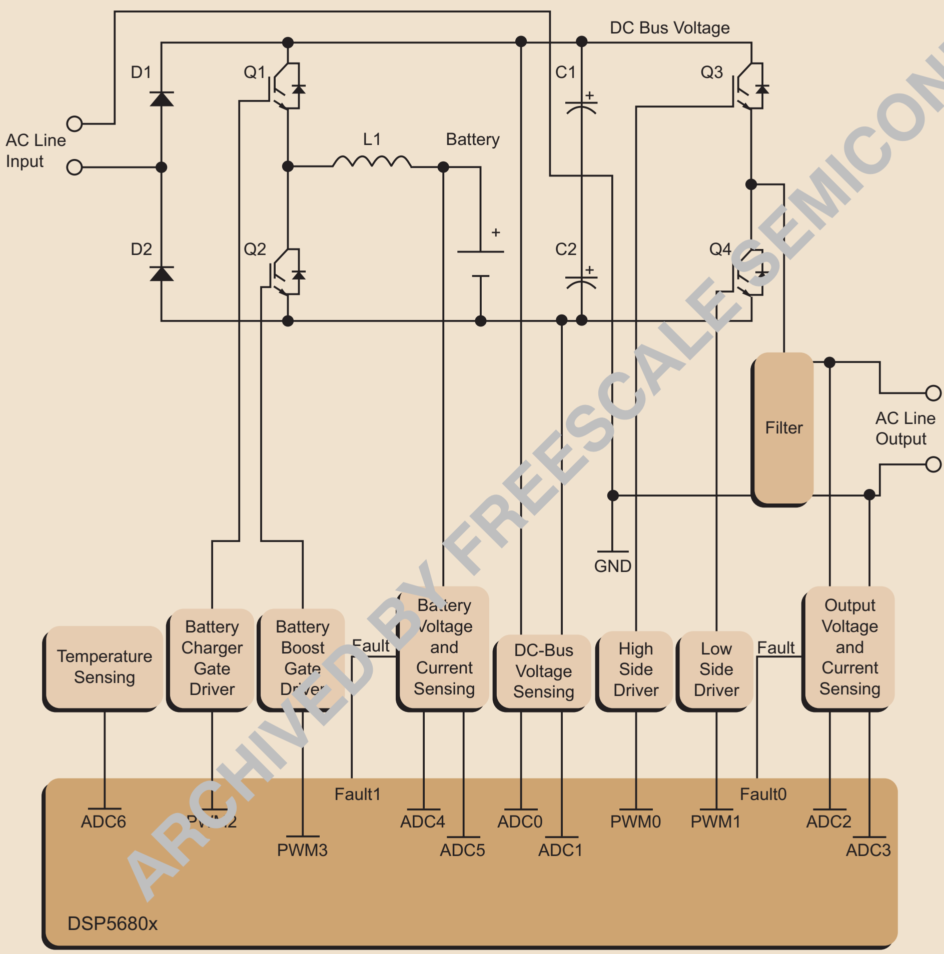
Uninterruptable Power Supply (UPS)

Overview

An uninterruptable power supply (UPS) system provides backup power supply for an application in the event of an electrical outage. Combining a microcontroller unit (MCU) and digital signal processor (DSP) in a single chip allows creation of a digital UPS offering higher performance at lower cost.

ONLINE UPS CONTROLLED BY DSP56F80X



Key Benefits

- Combines the calculation ability of a DSP with the controller function of an MCU on a single chip
- Offers unique configuration of peripherals and on-board memory at low cost
- On-chip CAN bus and SCIs allow UPS connection into a local network
- Out-of-the-box software components designed to expedite time-to-market and reduce development costs

Freescale Ordering Information

Part Number	Product Highlights	Additional Information
DSP56F803	80 MHz, 40 MIPS, CAN, SCI, SPI, ADC, PWMs, Quadrature Decoder, Quad Timer and > 31.5K Program Flash > 512K Program RAM > 4K Data Flash > 2K Data RAM	MCU-friendly instruction set, OnCE for debug, on-chip relaxation oscillator, 2K BootFLASH, external memory expansion, and up to 16 GPIO available in a 100-pin LQFP
DSP56F805	80 MHz, 40 MIPS, CAN, SCIs, SPI, ADC, PWMs, Quadrature Decoder, Quad Timer and > 31.5K Program Flash > 512K Program RAM > 4K Data Flash > 2K Data RAM	MCU-friendly instruction set, OnCE for debug, on-chip relaxation oscillator, 2K BootFLASH, external memory expansion, and up to 32 GPIO available in a 144-pin LQFP
DSP56F807	80 MHz, 40 MIPS, CAN, SCIs, SPI, ADCs, PWMs, Quadrature Decoder, Quad Timer and > 60K Program Flash > 2K Program RAM > 8K Data Flash > 4K Data RAM	MCU-friendly instruction set, OnCE for debug, on-chip relaxation oscillator, 2K BootFLASH, external memory expansion, and up to 32 GPIO available in both a 160-pin LQFP and 160 MAPBGA
MC56F8300 Family	60 MHZ, 60 MIPS, up to 576KB Flash, 36KB RAM, and Off-Chip Memory, SCI, SPI, ADC, PWM, Quadrature Decoder, Quad Timer, FlexCAN, GPIO, COP/ Watchdog, PLL, MCU-style software stack support, JTAG/OnCE for debug, temperature sensor	www.freescale.com
MC56F8100 Family	40 MHZ, 40 MIPS, up to 544KB Flash, 32KB RAM, and Off-Chip Memory, SCI, SPI, ADC, PWM, Quadrature Decoder, Quad Timer, FlexCAN, GPIO, COP/ Watchdog, PLL, MCU-style software stack support, JTAG/OnCE for debug	www.freescale.com

Design Challenges

Although the UPS has traditionally been designed as analog circuitry, digital UPSs are now preferred. These devices use low-cost MCUs or DSPs and offer sophisticated control algorithms with highly flexible software, the ability to add user interfaces, reduce components, introduce testing procedures, and increase reliability.

Several basic UPS topologies exist, differentiated by function during a power outage. The online UPS offers the greatest reliability and continuity of power supply. During normal operation, the load is connected to an inverter powered by a battery and/or another inverter. If a power outage occurs, the inverter is supplied by the battery with no switching or switching delay.

Freescale Semiconductor Solution

The Freescale Semiconductor Digital Signal Controllers are well-suited for digital UPS control, combining the DSP's calculation ability with the MCU's controller function on a single chip. Each of the family members offers a unique configuration of peripherals and on-board memory.

The figure on page 1 shows an online UPS controlled by Freescale Semiconductor DSP56F80x. This design produces an optimal UPS system through use of a single DSP56F80x controller. The controller monitors all necessary parameters, such as voltage, current, and temperature, and controls individual subsystems. The sensing blocks contain simple circuitry that brings the measurements within the range of the analog-to-digital converters (ADCs). Details of basic blocks, peripheral utilization, and a brief software description follow.

AC/DC Converter

An AC/DC converter generates the DC bus voltage of the UPS. The rectifier supplies both the AC output current and the battery-charging current. The simplest AC/DC converter is a standard half-bridge rectifier, containing two diodes (D1, D2), and requires no control means. The advantage is a simple but reliable design. The drawback is a nonsinusoidal input current with high harmonic content and electromagnetic interference (EMI) that becomes more apparent in high-power systems. If sinusoidal input current is required, implement a DSP-controlled active power factor correction (PFC) circuit.

DC/AC Inverter

The DC/AC inverter generates AC output voltage, which must be sinusoidal with specific frequency (50 Hz or 60 Hz) and amplitude (equal to the main line voltage). The inverter contains two power switches in a half-bridge configuration with antiparallel diodes (Q3, Q4). Both power devices (isolating gate bipolar transistors, or IGBTs) are controlled by the device through drivers using pulse width modulation (PWM). When filtered, sinusoidal output voltage is generated. The limitation of this topology is the amplitude of the generated sinusoidal voltage that depends on the DC bus voltage level. The AC UPS output voltage is approximately equal to the AC UPS input voltage:

$$V_{rms\_out} \cong V_{rms\_in}$$

The power devices and the output filter create a voltage drop of several volts, which is within the AC voltage tolerance. If a more precise output voltage is required, a voltage transformer can be added to the UPS output. The voltage level of the battery is not critical, because the DC/DC boost converter (see below) can increase the voltage to the required DC bus voltage level.

The device generates sinusoidal modulated complementary PWM pulses on channels PWM 0 and PWM 1. Due to the limited turn-on and turn-off time of the power switches, the dead-time inserted between complementary switching instances disables burn-out of the inverter. To be out of the audible noise, the switching PWM frequency must be about 16–20 kHz. The DSP56F80x on-chip PWM module with dedicated hardware circuitry meets these requirements, containing complementary PWM channels with dead-time, protection block, and other features.

The algorithm controls the output voltage using voltage control loop, current control loop, and sine wave generation. The algorithm requires voltage and current feedback, so simple voltage and current sensors detect the appropriate analog values. The on-chip ADC reads voltage on ADC2 and current on ADC3 in appropriate instances given by the control loop time constants. The inverter also contains circuitry to protect against output overcurrent. Output current is compared with the maximum allowed value, and the generated fault signal is fed to the fault input, Fault 0. If overcurrent is detected, the inverter is disabled and the main relay switches on the AC bypass.

DC/DC Converter

The DC/DC converter accommodates two basic functions: charging the battery when required and providing the appropriate level of DC bus voltage for the inverter if the main line is disconnected. Often battery voltage is lower than DC bus voltage, so the DC/DC converter increases the voltage appropriately. The hardware circuitry contains an IGBT half-bridge with antiparallel diodes. Both transistors of the half-bridge are controlled from the PWM unit. The PWM channels are set to independent edge-aligned mode, which controls the power switches individually. Overcurrent protection circuitry is available. The PWM unit can control the fault handling from individual fault inputs separately, so even if the DC/DC converter faults, the DC/AC inverter operation continues if DC bus voltage is present. The battery is protected from high temperature: its temperature is sensed by the ADC (ADC6) and fault state is evaluated. The IGBT half-bridge is used for both charging and boost operations as described below:

- **Battery Charger.** The battery charger charges the battery from the DC bus. The battery's voltage and charging current are sensed by the voltage sensor (ADC5) and the current sensor (ADC4) connected to the ADC. The control algorithm controls the charging current through PWM module on the upper power switch (Q1) of the bridge (PWM2). The lower switch (Q2) is permanently switched off in this mode.
- **Boost Converter.** The boost converter supplies the DC bus from the battery through inductance L1. The boost current and DC bus voltage are sensed by the voltage (ADC0, ADC1) sensors and current (ADC4) sensor. The control algorithm controls the DC bus voltage through PWM module on the lower power switch (Q2) of the bridge (PWM3). The upper switch (Q1) is permanently switched off in this mode of operation, so it operates as a standard boost converter.

Development Tools			
Tool Type	**Product Name**	**Vendor**	**Description**
Software	CW568X	Freescale Semiconductor	CodeWarrior™ Development Studio for 56800/E Controllers with Processor Expert (Metrowerks)
Software	Processor Expert	Freescale Semiconductor	Software infrastructure that allows development of efficient, high-level software applications that are fully portable and reusable across all 56800/E family of processors.
Software	CWDSP56800	Freescale Semiconductor	CodeWarrior Software Development Tools for 56800 (Metrowerks)
Hardware	56F800DEMO	Freescale Semiconductor	56F800 Demonstration Kit
Hardware	DSP56F803EVM	Freescale Semiconductor	Evaluation Module for the 56F803
Hardware	DSP56F805EVM	Freescale Semiconductor	Evaluation Module for the 56F805
Hardware	DSP56F807EVM	Freescale Semiconductor	Evaluation Module for the 56F807
Hardware	MC56F8300DSK	Freescale Semiconductor	56F8300 Developers Start Kit
Hardware	MC56F8367EVM	Freescale Semiconductor	Evaluation Module for the 56F834x, 56F835x, 56F836x
Development Kit	DSPOSRTOS	Freescale Semiconductor	Emulation Support for 56F80x Processors (Requires Ethernet Network)

Disclaimer

This document may not include all the details necessary to completely develop this design. It is provided as a reference only and is intended to demonstrate the variety of applications for the device.

Learn More: Contact the Technical Information Center at +1-800-521-6274 or +1-480-768-2130.
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SG2070
REV 4
6/2005

June2005