PB_PF5103

Power management integrated circuit (PMIC) for high-performance applications

Rev. 1.1 — 18 December 2023 **Product brief**

Document information

Information	Content
Keywords	PF5103, power management, integrated circuit (PMIC), high performance, ASIL B, automotive, functional safety
Abstract	The PF5103 integrates multiple high-performance buck regulators and LDO regulators. It can operate as a standalone point-of-load regulator IC, or as a companion chip to a larger PMIC.

1 Introduction

This product brief is intended to provide overview/summary information for evaluating a product for design suitability. It is intended for quick reference only and should not be relied upon to contain detailed and full information.

Some of the content in this product brief is extracted from the product's full data sheet. In case of any inconsistency or conflict, the full data sheet prevails.

For detailed and full information, see the relevant PF5103 full data sheet, available via the NXP website at https://www.nxp.com.

2 General description

The PF5103 integrates multiple high-performance buck regulators and LDO regulators. It can operate as a standalone point-of-load regulator IC or as a companion chip to a larger power management integrated circuit (PMIC).

Built-in One-Time-Programmable (OTP) memory stores key startup configurations, drastically reducing external components typically used to set output voltage and sequence of regulators. Regulator parameters are adjustable through high-speed I^2C after startup, offering flexibility for different system states.

Functional safety features, developed according to ISO 26262 specifications, enable the device to reach safety levels up to ASIL B.

3 Feature and benefits

The PF5103 is a PMIC designed to be the primary core power supply for NXP high-end ADAS application processors.

- Buck regulators
  - SW1, SW2 and SW3: 0.5 V to 3.3 V; 3500 mA; 1.5 % accuracy
  - Dynamic voltage scaling
  - Configurable as dual- and triple-phase regulator
  - Programmable current limit
  - Spread-spectrum and manual tuning of switching frequency
- LDO regulators
  - LDO1: 0.75 V to 3.3 V; 200 mA; 1.5 % accuracy
  - LDO2: 0.75 V to 3.3 V; 500 mA; 1.5 % accuracy
- PGOOD output and monitor
- Clock synchronization through configurable input sync pin
- System features
  - Advanced state machine for seamless processor interface
  - High-speed I^2C interface support (up to 3.4 MHz)
  - Programmable soft-start sequence and power-down sequence
  - Programmable regulator configuration
- OTP memory for device configuration
- Monitoring circuit to fit ASIL B safety level
  - Independent voltage monitoring with programmable fault protection
  - Advance thermal monitoring and protection
  - Watchdog monitoring and programmable internal watchdog counter
  - I^2C Cyclic Redundancy Check CRC and write protection mechanism
  - Analog built-in self-test (ABIST)

4 Applications

- Automotive – RADAR, infotainment, domain controllers
- High-end consumer and industrial

5 Ordering information

Table 1. Ordering information

Type number[1]	Package		
	Name	Description	Version
PPF5103AMBA0ES[2]	HWQFN28	HWQFN28, plastic thermal enhanced very thin quad flat pack; no leads, wettable flank, 28 terminals, 0.5 mm pitch, 4.5 mm x 4.5 mm x 0.53 mm body	SOT2089-1(SC)
PPF5103AMMA0ES[3]			

[1] To order parts in tape and reel, add the R2 suffix to the part number.
[2] Safety grade: ASIL B
[3] Safety grade: QM

6 Block diagram

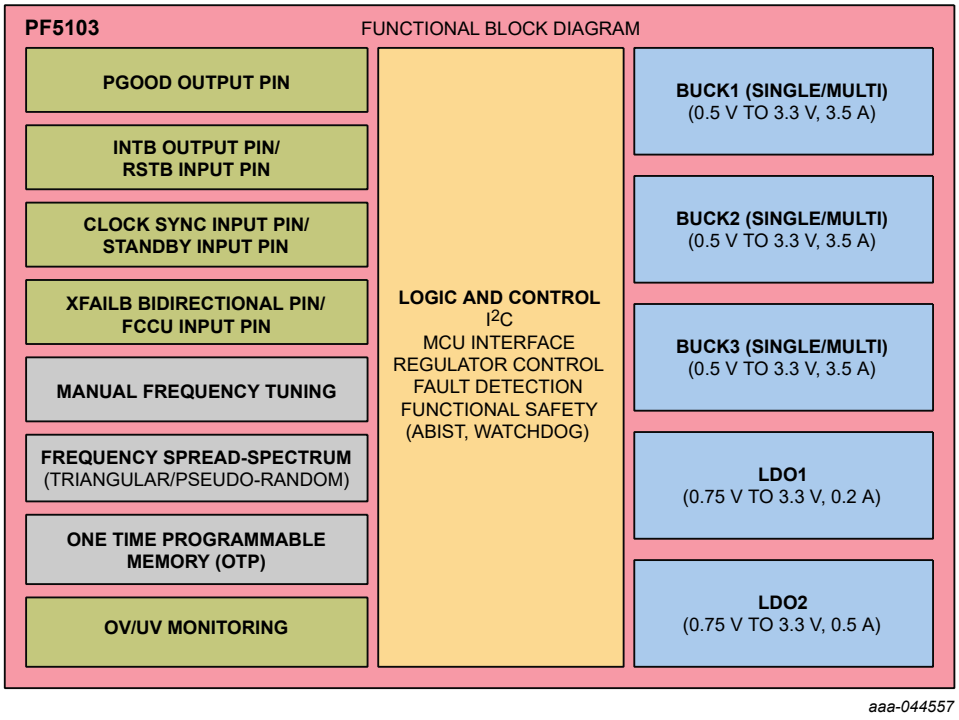

Figure 1. PF5103 block diagram

7 Pinning information

7.1 Pinout

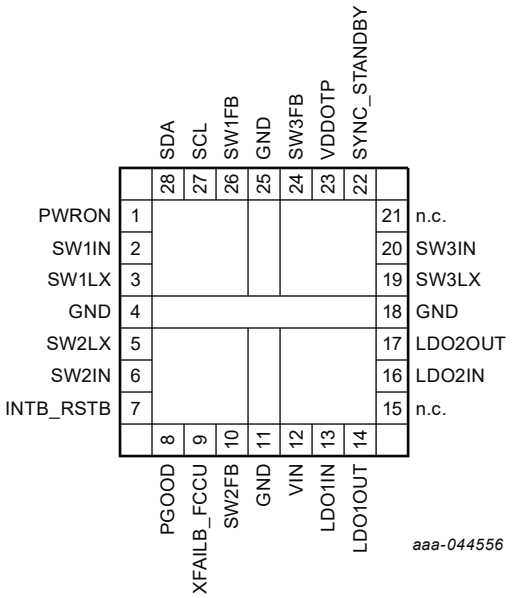

Figure 2. PF5103 pinout

7.2 Pinning description

Table 2. PF5103 pinout

QFN pin number	Pin name	Pin description	Min	Max	Units
1	PWRON	PWRON input	−0.3	5.5	V
2	SW1IN	SW1 input supply	−0.3	5.5	V
3	SW1LX	SW1 switching node	−0.3	5.5	V
4	PGND	Ground	−0.3	0.3	V
5	SW2LX	SW2 switching node	−0.7	5.5	V
6	SW2IN	SW2 input supply	−0.3	5.5	V
7	INTB/RSTB	Interrupt output/External reset input	−0.3	5.5	V
8	PGOOD	PGOOD output	−0.3	5.5	V
9	FCCU/XFAILB	XFAILB bidirectional signal	−0.3	5.5	V
10	SW2FB	SW2 feedback input	−0.3	5.5	V
11	GND	Ground	−0.3	0.3	V
12	VIN	Input supply	−0.3	5.5	V
13	LDO1IN	LDO1 input	−0.3	5.5	V
14	LDO1OUT	LDO1 output	−0.3	5.5	V
15	NC	No connect	−0.3	0.3	V
16	LDO2IN	LDO2 INPUT	-0.3	5.5	V

Table 2. PF5103 pinout*...continued*

QFN pin number	Pin name	Pin description	Min	Max	Units
17	LDO2OUT	LDO2 output	−0.3	5.5	V
18	GND	Ground	−0.3	0.3	V
19	SW3LX	SW3 switching node	−0.7	5.5	V
20	SW3IN	SW3 input supply	−0.3	5.5	V
21	NC	No connect	−0.3	0.3	V
22	SYNC_STANDBY	Clock synchronization input or Standby input	−0.3	5.5	V
23	VDDOTP	Debug mode / OTP programming input supply	−0.3	10	V
24	SW3FB	SW3 feedback input	−0.3	5.5	V
25	GND	Ground	−0.3	0.3	V
26	SW1FB	SW1 feedback input	−0.3	5.5	V
27	SCL	I^2C SCL signal	−0.3	5.5	V
28	SDA	I^2C SDA signal	−0.3	5.5	V

8 Package outline

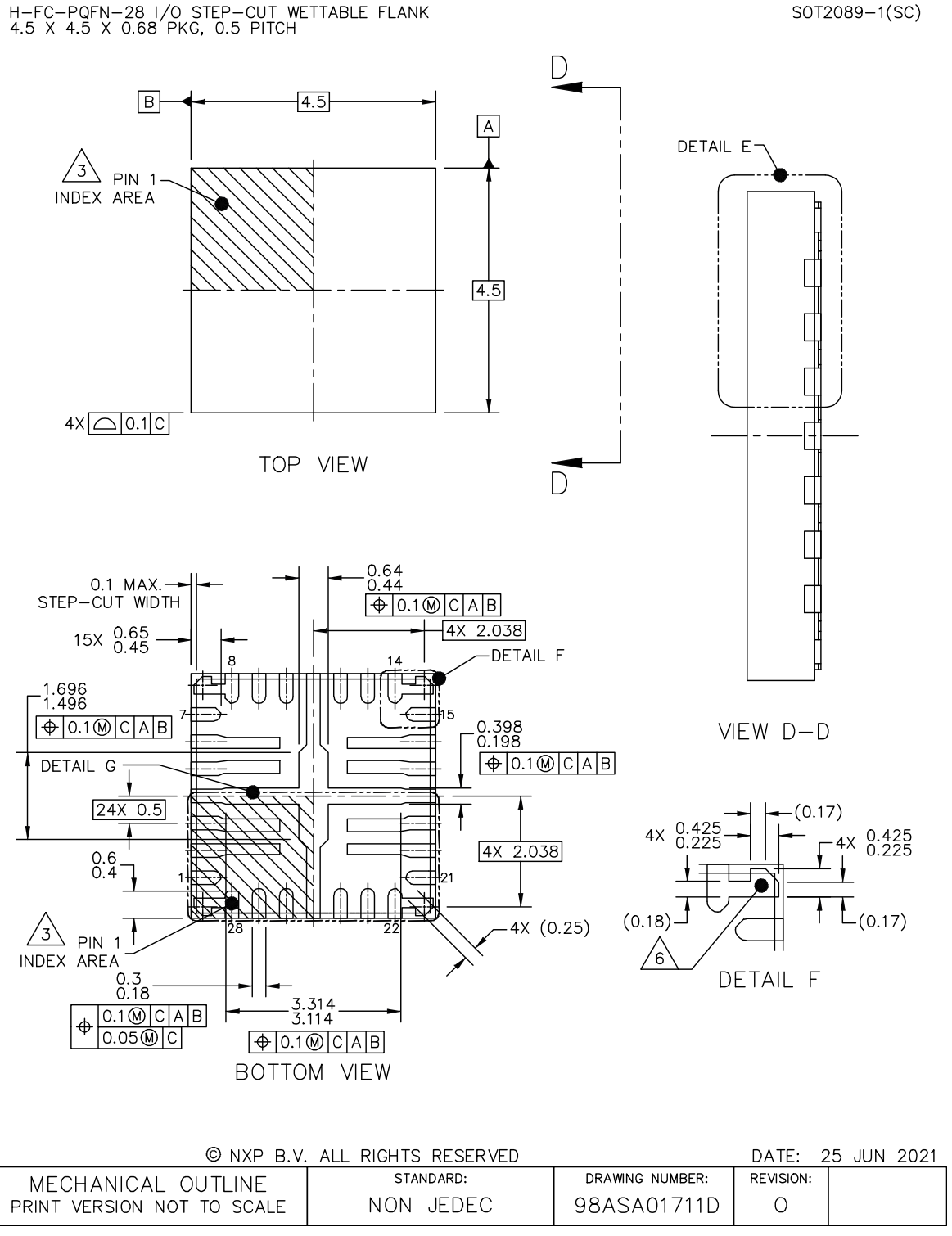

Figure 3. Package outline for PQFN28

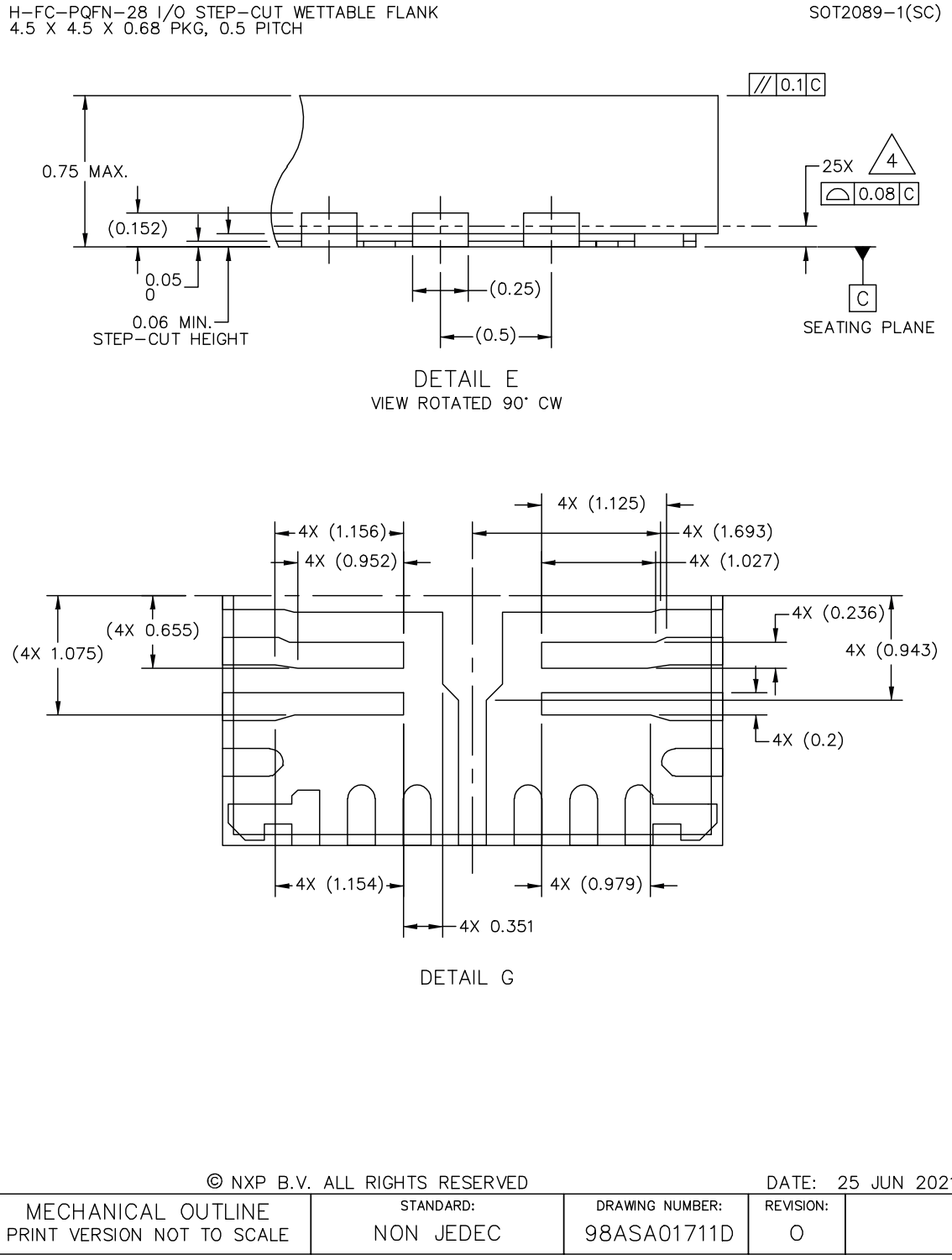

Figure 4. Package outline detail for PQFN28

H–FC–PQFN–28 I/O STEP–CUT WETTABLE FLANK
4.5 X 4.5 X 0.68 PKG, 0.5 PITCH

SOT2089–1(SC)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN 1 FEATURE, SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH PAD.
5. MIN. METAL GAP FOR LEAD TO EXPOSED PAD SHALL BE 0.2 MM.
6. ANCHORING PADS.

DATE: 25 JUN 2021

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01711D	REVISION: O	

Figure 5. Package outline notes for PQFN28

9 Revision history

Table 3. Revision history

Rev	Date	Description of changes
PB_PF5103 v1.1	20231218	Change highest ASIL possible from D to B
PB_PF5103 v.1.0	20230110	Initial release

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