Freescale Semiconductor
Product Brief

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i.MX27 Product Brief

Multimedia Applications Processor

The i.MX27 Multimedia Applications Processor introduces a new level of performance to the Mobile Multimedia Experience as part of the growing i.MX family of multimedia-focused products. This newest i.MX product leverages industry-leading technologies to provide extended battery life together with the video performance needed for the exceptional multimedia experience demanded by today's marketplace.

Whether you are designing a smart phone with high-resolution (VGA resolution, 25 fps—full duplex) or (D1 resolution, 30 fps—half-duplex) videoconferencing at very low power, wireless PDA, mobile entertainment, or any of many other portable multimedia applications, the i.MX27 Multimedia Applications Processor provides design performance to spare, a high degree of integration, and some of the best power management in the industry. This combination of features, design integration, and extended battery life can significantly reduce your design time, and provide your designs with flexibility necessary for today's competitive marketplace.

Contents

1 Application Examples

The flexibility of the i.MX27 Multimedia Applications Processor architecture enables it to be used in a wide variety of applications.

1.1 Video and Voice over IP (V2IP) Powerhouse

As the Voice over IP (VoIP) market grows, Freescale is designing and providing the tools needed for the next evolution of the market—Video and Voice over IP (V2IP). Creating a simple V2IP device requires a minimum number of chips, as shown in Figure 1. The power and versatility of the i.MX27 Multimedia Applications Processor is apparent when it is used as the core of a V2IP solution. When used in a typical V2IP device, the i.MX27 processor delivers the power to drive high-quality audio through wideband audio and wideband acoustic echo cancellers (AECs), in-call audio and video recording on Flash (or other removable media), and decentralized three-way, audio-video calls. It also has the potential to provide the ability to make V2IP calls with Bluetooth™ audio.

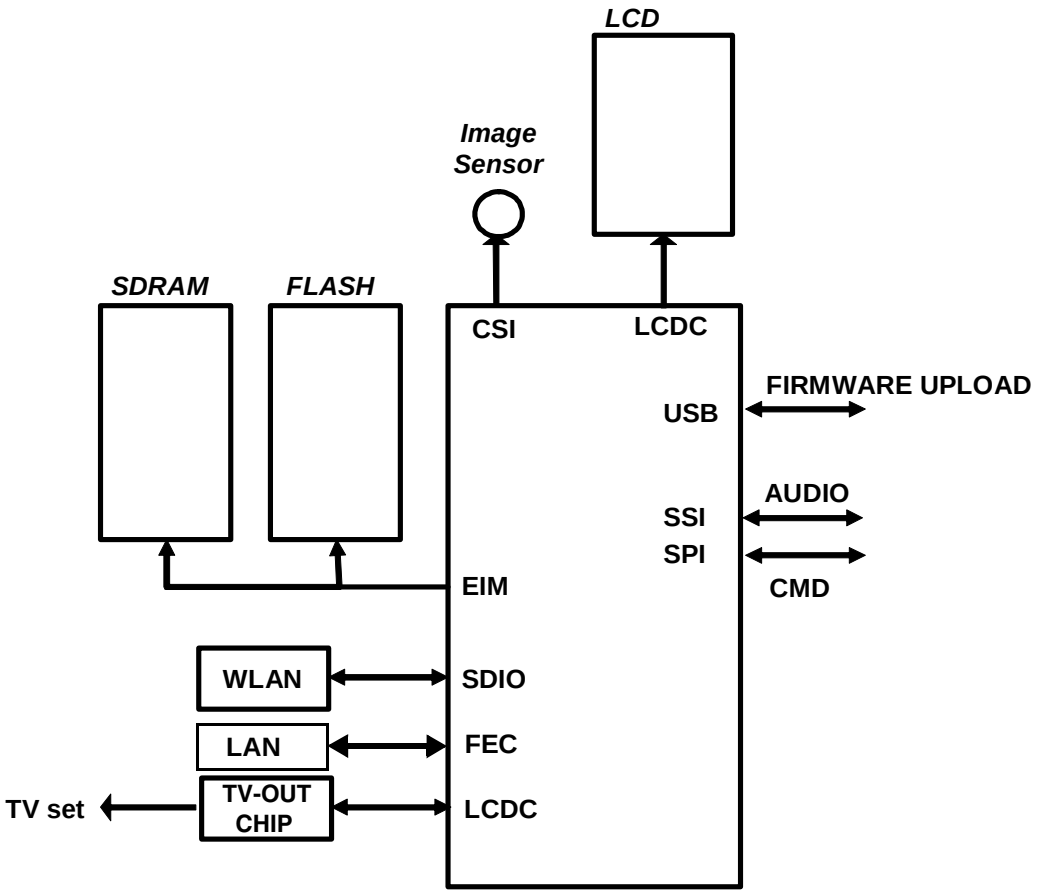

Figure 1. Basic V2IP Phone Layout Using the i.MX27 Processor

2 Features

The i.MX27 Multimedia Applications Processor is targeted for Video and Voice over IP (V2IP) and smart remote controllers. It also provides low-power solutions for any high-performance and demanding multimedia and graphics applications.

The i.MX27 architecture is compatible with the i.MX21 applications processor.

The system includes the following features:

- Multi-standard video codec
  - MPEG-4 part-II simple profile encoding/decoding
  - H.264/AVC (Advanced Video Coding) baseline profile encoding/decoding
  - H.264 encode and decode up to D1 resolution (half duplex mode), VGA resolution full duplex
  - H.263 P3 encoding/decoding
  - Multi-party call: one stream encoding and two streams decoding simultaneously
  - Multi-format: encodes MPEG-4 bitstream, and decodes H.264 bitstream simultaneously
  - On-the-fly video processing that reduces system memory load (for example, the power-efficient viewfinder application with no involvement of either the memory system or the ARM® CPU)
- Advanced power management
  - Dynamic process temperature compensation
  - Multiple clock and power domains
  - Independent gating of power domains
- Multiple communication and expansion ports

2.1 Block Diagram

Figure 2 shows the functional modules of the i.MX27 Multimedia Applications Processor.

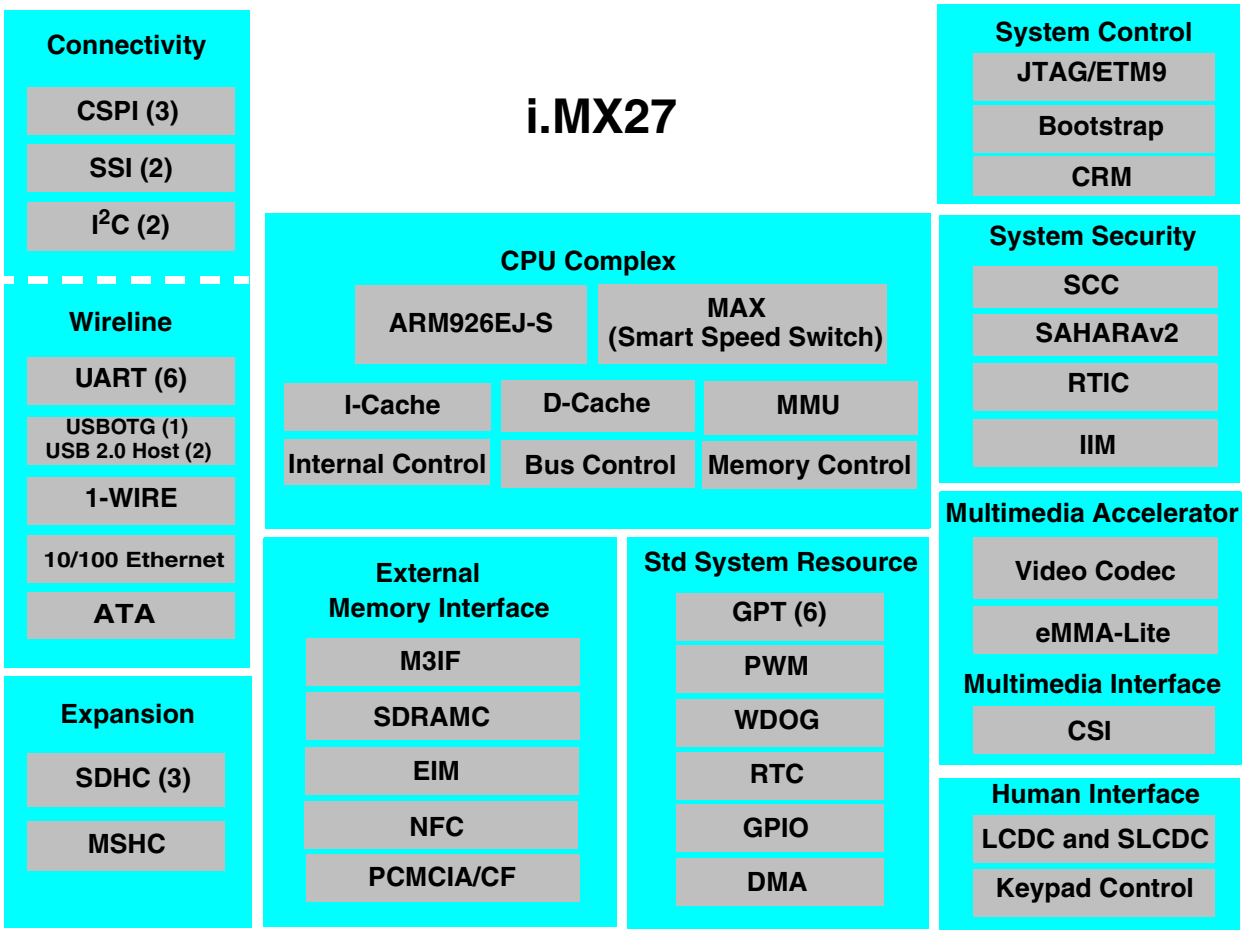

Figure 2. i.MX27 Functional Block Diagram

2.2 Critical Performance Parameters

This section describes the operating voltage, packaging, and operating temperature goals for the i.MX27 processor.

2.2.1 Operating Voltage

The operating voltage is as follows:

- I/O voltage: 1.8 V to 3.0 V
- Internal logic voltage: 1.15 V to 1.65 V

2.2.2 Package Information and Pinout

The i.MX27 processor is available in a 17 mm × 17 mm, .65 pitch, 404-pin MAPBGA package.

2.2.3 Operating Temperature Range

The i.MX27 Multimedia Applications Processor's operating temperature range (and storage temperature range) is –20° C to +85° C.

2.3 Chip-Level Features

2.3.1 Application Processor (AP) Domain

The application processor (AP) domain is responsible for running the operating system and applications software, providing the user interface, and supplying access to integrated and external peripherals. The look and feel of the product depends on the software running on this processor, ultimately tying market acceptance to the availability of a wide variety of off-the-shelf, third-party software and development tools.

ARM's CPU family has emerged as the de facto standard for mobile and wireless product application processors. In order to leverage the growing software base for this family, the application processor in the i.MX27 processor is based on the ARM architecture. With high-frequency operation, the AP achieves multimedia and graphics performance to meet the targets for the low-tier requirements.

The AP domain is built around an ARM926EJ-S™ processor with 16-Kbyte instruction and 16-Kbyte data L1 caches, an MMU, a multi-ported crossbar switch, and advanced debug and trace interfaces.

The processor is intended to operate at a maximum frequency of 400 MHz in order to support the required multimedia use cases. Furthermore, an enhanced Multimedia Accelerator (eMMA) and LCD Controller are included in the application processor domain to offload from the core functions such as color space conversion, image rotation and scaling, graphics overlay, and pre- and post-processing.

2.3.2 Advanced Power Management

To address the continuing need to reduce power consumption, the following techniques are incorporated into the i.MX27 processor:

- Clock Gating: Clock distribution circuits in digital ICs with the complexity of i.MX27 applications processor can consume as much as 40% of the total dissipated power. By inserting gating into the clock paths, unused portions of the chip can be disabled.
- Built-in Well Biasing: Well biasing is a feature incorporated in the design used to reduce the sub-threshold channel leakage. For the 90 nm digital process, the sub-threshold leakage could be reduced by a factor of 10 over the nominal leakage.

2.3.3 Connectivity Peripherals

The i.MX27 processor supports connections to various types of external memories, such as 133-MHz DDR, NAND Flash, NOR Flash, SDRAM, and SRAM. The i.MX27 processor can be connected to a variety of external devices using technology, such as high-speed USBOTG 2.0, the Advanced Technology Attachment (ATA), Multimedia/Secure Data (MMC/SDIO), and CompactFlash.

2.4 Module Features

This section describes further the functional groupings of blocks shown in Figure 2.

Table 1. i.MX27 Multimedia Applications Processor Digital and Analog Modules

Block Mnemonic	Block Name	Subsystem	Brief Description
1-Wire	1-Wire	System Control	The 1-Wire module is a peripheral device that communicates with the ARM926EJ-S Core via the IP interface, and provides a communication line to a 1 Kbit Add-Only Memory (DS2502).
ARM926	ARM926EJ-S Platform	ARM	The ARM926EJ-S platform operates at speeds up to 400 MHz, and is optimized for minimal power consumption using the most advanced techniques for power saving. With 90 nm technology and dual Vt, the i.MX27 processor provides the optimal performance vs. leakage current balance.
ATA	ATA	Peripherals	The ATA block is an AT attachment host interface. Its main use is to interface with hard disc drives and optical disc drives. It interfaces with the ATA device over a number of ATA signals.
AUDMUX	Digital Audio MUX	Peripherals	The Digital Audio MUX (AUDMUX) provides a programmable interconnect fabric for voice, audio, and synchronous data routing between the i.MX27 SSI modules and external SSI, audio codecs, and voice codecs. With the AUDMUX, resources do not need to be hard-wired and can be effectively shared in different configurations. The AUDMUX interconnections enable multiple simultaneous separate audio/voice/data flows between the ports in a point-to-point or point-to-multipoint configuration.
CCM	Clock Controller Module	Clocks	The PLL Clock Controller Module (CCM) produces the clock signals used and distributed by the ARM9 Platform Clock Controller, and generates the clock signals used throughout the i.MX27 chip as well as by external peripherals.
CSI	CMOS Sensor Interface	Peripherals	The CSI is a logic interface that enables the i.MX27 processor to directly connect to external CMOS sensors and CCIR656 video source.
CSPI1 CSPI2 CSPI3	Configurable Serial Peripheral Interface	Interchip Connectivity	The i.MX27 processor has three Configurable Serial Peripheral Interface (CSPI) modules that enable rapid data communication with fewer software interrupts than conventional serial communications. Each CSPI is equipped with two data FIFOs and is a master/slave configurable serial peripheral interface module, allowing the i.MX27 processor to interface with both external SPI master and slave devices.
EMI	External Memory Interface	Connectivity Peripherals	External and Internal Memory Interface. The EMI contains different external memory controllers in order to support several memory devices: • ESDCTL/MDDRC—Enhanced SDRAM/LPDDR memory controller • PCMCIA—PCMCIA memory controller • NFC (also NANDFC)—NAND Flash memory controller • WEIM—Wireless External Interface Module

Table 1. i.MX27 Multimedia Applications Processor Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
eMMA_lt	enhanced Multimedia Accelerator Lite	Peripherals	The enhanced Multimedia Accelerator Lite (eMMA_lt) only consists of the video Pre-processor (PrP) and Post-processor (PP), similar functionalities with original eMMA which also includes MPEG-4 Encoder (EN) and Decoder (DE). These blocks work together to provide video acceleration and off-load the CPU from computation-intensive tasks. The PrP and PP can be used for generic video pre- and post-processing such as scaling, resizing, and color space conversions.
ESDCTL/MDDRC	Enhanced SDRAM/LPDDR Memory Controller	Connectivity Peripherals	The ESDCTL provides an interface, configuration, and control for many different types of synchronous SDRAM and Low Power Mobile DDR (LPDDR) memories.
FEC	10/100 Fast Ethernet Controller	Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support both 10 Mbps and 100 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media.
GPIO	General Purpose Input/Output	System Control	The GPIO module in the i.MX27 provides six general purpose I/O (GPIO) ports (PA, PB, PC, PD, PE, and PF). Each single GPIO port is a 32-bit port that may be multiplexed with one or more dedicated functions.
GPT1 GPT2 GPT3 GPT4 GPT5 GPT6	General Purpose Timers	System Control	The i.MX27 contains six identical 32-bit general-purpose timers (GPT) with programmable prescalers and compare and capture registers. Each timer's counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. Each GPT can also generate an interrupt when the timer reaches a programmed value.
I^2C1 I^2C2	Inter-Integrated Circuit	Inter-Chip Connectivity	The I^2C operates up to 400 kbps but it depends on the pad loading and timing (for pad requirement details, refer to Philips I^2C Bus Specification, Version 2.1). The I^2C system is a true multiple-master bus including arbitration and collision detection that prevents data corruption if multiple devices attempt to control the bus simultaneously. This feature supports complex applications with multiprocessor control and can be used for rapid testing and alignment of end products through external connections to an assembly-line computer.
IIM	IC Identification Module	Security	The IC Identification Module (IIM) provides an interface for reading and in some cases programming and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically-programmable poly fuses (e-Fuses).
JTAGC	JTAG Controller	System Control	The JTAG Controller module supports Debug access to the ARM926 core. The JTAG Controller is compatible with IEEE1149.1 Standard Test Access Port and Boundary Scan Architecture.
KPP	Keypad Port	Connectivity and Expansion	The Keypad Port (KPP) is a 16-bit peripheral that can be used either for keypad matrix interface or as general purpose I/O.
LCDC	Liquid Crystal Display Controller	Peripherals	The Liquid Crystal Display Controller (LCDC) provides display data for external gray-scale or color LCD panels. The LCDC is capable of supporting black-and-white, gray-scale, passive-matrix color (passive color or CSTN), and active-matrix color (active color or TFT) LCD panels.

Table 1. i.MX27 Multimedia Applications Processor Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
MSHC	Memory Stick Host Controller	Connectivity and Expansion	The Memory Stick Host Controller (MSHC) consists of two sub-modules: the MSHC gasket and the Sony Memory Stick Host Controller (SMSC). The SMSC module, which is the actual memory stick host controller, is compatible with Sony Memory Stick Ver. 1.x and Memory Stick PRO.
NFC	NAND Flash Memory Controller	Connectivity Peripherals	The NAND Flash Controller (NFC) interfaces standard NAND Flash devices to the i.MX27 and hides the complexities of accessing the NAND Flash. It provides a glueless interface to both 8-bit and 16-bit NAND Flash parts with page sizes of 512 bytes or 2 Kbytes, and densities of up to 2 Gbits.
PCMCIA	PCMCIA Memory Controller	Connectivity Peripherals	The PCMCIA host adapter module complies to the PCMCIA 2.1 standard and provides the control logic for PCMCIA socket interfaces. It requires some additional external analog power switching logic and buffering. The additional external buffers enable the PCMCIA host adapter module to support one PCMCIA socket.
PWM	Pulse-Width Modulator	System Control	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images. It can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.
RTC	Real-Time Clock	System Control	The Real-Time Clock (RTC) converts a crystal reference clock to a 1-Hz signal, which is used to increment the time-of-day (TOD) counters for seconds, minutes, hours, and days. The alarm functions, when enabled, generate RTC interrupts when the TOD settings reach programmed values. The sampling timer generates fixed-frequency interrupts, and the minute stopwatch allows for efficient interrupts on minute boundaries.
RTIC	Run-Time Integrity Checker	Security	The Run-Time Integrity Checker (RTIC) ensures the integrity of the peripheral memory contents and assists with boot authentication. The RTIC has the ability to verify the memory contents during system boot and during run-time execution. If the memory contents at runtime fail to match the hash signature, an error in the security monitor is triggered.
SAHARA	Symmetric/Asymmetric Hashing and Random Accelerator (SAHARA) Security Accelerator	Security	The SAHARA (Symmetric/Asymmetric Hashing and Random Accelerator) is a security co-processor, which forms part of Freescale's Platform Independent Security Architecture (PISA), and can be used on cell phone baseband processors or wireless PDAs. It implements block encryption algorithms, (AES, DES, and 3DES), hashing algorithms (MD5, SHA-1, SHA-224, and SHA-256), stream cipher algorithm (ARC4), and a hardware random number generator (RNG).
SCC	Security Controller	Security	The Security Controller (SCC) comprises two sub-blocks, the Secure RAM and the Security Monitor. Overall, its primary functionality is associated with establishing the following: • A centralized security state controller and hardware security state with a hardware configured, unalterable security policy • An uninterruptable hardware mechanism to detect and respond to threat detection signals (specifically platform test access signals) • A device unique data protection/encryption resource to enable off-chip storage of security sensitive data • An internal storage resource, which automatically and irrevocably destroys plain text security sensitive data upon threat detection

Table 1. i.MX27 Multimedia Applications Processor Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SDHC1 SDHC2 SDHC3	Security Digital Host Controller	Peripherals	The Security Digital Host Controller (SDHC) integrates both MMC support along with SD memory and I/O functions, including SD memory and I/O combo card.
SLCDC	Smart Liquid Crystal Display Controller	Peripherals	The Smart Liquid Crystal Display Controller (SLCDC) module transfers data from the display memory buffer to the external display device. Direct Memory Access (DMA) transfers the data transparently with minimal software intervention. Bus utilization of the DMA is controllable and deterministic.
SSI1 SSI2	Synchronous Serial Interface	Inter-Chip Connectivity	The Synchronous Serial Interface (SSI) is a full-duplex serial port that allows the chip to communicate with a variety of serial devices. SSI is typically used to transfer samples in a periodic manner. The SSI consists of independent transmitter and receiver sections with independent clock generation and frame synchronization.
UART1 UART2 UART3 UART4 UART5 UART6	Universal Asynchronous Receiver/ Transmitters	Connectivity and Expansion	The UART module is capable of standard RS-232 non-return-to-zero (NRZ) encoding format and IrDA-compatible infrared modes. The UART provides serial communication capability with external devices through an RS-232 cable or through use of external circuitry that converts infrared signals to electrical signals (for reception), or transforms electrical signals to signals that drive an infrared LED (for transmission) to provide low speed IrDA compatibility.
USBOTG	Universal Serial Bus, On-the-Go	Connectivity and Expansion	The Universal Serial Bus, On-The-Go (USBOTG) High-Speed module contains all of the functionality required to support three independent USB ports, compatible with the USB 2.0 specification. In addition to the normal USB functionality, the module also provides support for direct connections to on-board USB peripherals and supports multiple interface types for serial transceivers.
Video Codec	Video_Codec	Connectivity and Expansion	The Video_Codec module can encode/decode image data and support multiple image processing standards, including MPEG-4 SP, H.263 P3 (including annex I, J, K and T), and H.264 BP. VGA full duplex H264 at 25fps and VGA full duplex MPEG-4 at 30fps.
WDOG	Watchdog Timer	System Control	The Watchdog Timer module (WDOG Timer) protects against system failures by providing a method of escaping from unexpected events or programming errors. Once activated, the timer must be serviced by software on a periodic basis.

3 Document Revision History

Table 2 summarizes the document's revision history.

Table 2. Revision History

Revision	Substantive Change(s)
Rev. 1.1	Section 2.2.3, "Operating Temperature Range": The operating temperature range was updated to –20° C to +85° C.

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