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Product Brief

# MCF547X Family Integrated Microprocessor Product Brief

Network connectivity requirements in the factory automation, process control, security, and low-end networking marketplaces are generating demands for high performance, highly integrated, and cost effective microprocessors with connectivity peripherals. The ColdFire MCF547X family was generated to service the needs of emerging high-performance network connected devices.

The MCF547X family integrates a high performance ColdFire V4e processor core with a rich set of connectivity peripherals focused on industrial and consumer networking. The MCF547X family also incorporates an innovative I/O subsystem along with the high performance ColdFire V4e processor core to provide high performance and system throughput.

To locate any published errata or updates for this document, refer to the ColdFire products web site at http://www.freescale.com/ColdFire.

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# 1    MCF547X Family Overview

The MCF547X family is based on the ColdFire V4e Core, a complex which comprises the ColdFire V4 central processor unit (CPU), an enhanced multiply-accumulate unit (EMAC), a memory management unit (MMU), a double-precision floating point unit (FPU) conforming to standard IEEE-754, and controllers for caches and local data memories. The MCF547X family is capable of performing up to an operating frequency of 266 MHz or 410 MIPS (Dhrystone 2.1).

To maximize throughput, the MCF547X Family incorporates three different external bus interfaces:

1. The general purpose local bus (FlexBus) is used for system boot memories and simple peripherals and has up to 6 chip selects.
2. Program code and data are stored in SDRAM connected to a dedicated 32-bit double data rate (DDR) bus that can run at up to one half the CPU core frequency. The glueless DDR SDRAM controller handles all address multiplexing, input and output strobe timing, and memory bus clock generation.
3. A 32-bit PCI bus compliant with the version 2.2 specification and running at a typical frequency of 33 MHz or 66 MHz supports peripherals that require high bandwidth, the ability to arbitrate for bus mastership, and access to internal MCF547X memory resources.

The MCF547X family provides substantial communications functionality by integrating the following connectivity peripherals:

- Up to two (2) 10/100 Mbps Fast Ethernet Controllers (FECs)
- An optional USB 2.0 device (slave) module with seven (7) endpoints and an integrated transceiver
- Up to four (4) UART/USART/IRDA/Modem Programmable Serial Controllers (PSCs)
- A DMA Serial Peripheral Interface (DSPI)
- An Inter-Integrated Circuit ($I^2C$) bus controller

Additionally, hardware support for a range of Internet security standards is provided by an optional bus-mastering cryptopgraphy accelerator. This module incorporates units to speed DES/3DES and AES block ciphers, the RC4 stream cipher, bulk data hashing (MD5/SHA-1/SHA-256/HMAC), and random number generation. Hardware acceleration of these functions is critical to avoiding the throughput bottlenecks associated with software-only implementations of SSH, SSL/TLS, IPsec, SRTP, WEP, and other security standards. The incorporation of cryptography accelration makes the MCF547X family a compelling solution for a wide range of office automation, industrial control, and SOHO networking devices that must have the ability to securely transmit critical equipment control information across typically insecure Ethernet data networks.

Additional features on MCF547X products include a watchdog timer, two 32-bit slice timers for RTOS scheduling and alarm functionality, up to four 32-bit general-purpose timers with capture, compare, and pulse width modulation capability, a multi-source vectored interrupt controller, a phase-locked loop (PLL) to generate the system clock, 32 Kbytes of SRAM for high-speed local data storage, and multiple general-purpose I/O ports. To manage current consumption, MCF547X products provide chip-wide internal clock gating control on a per module basis under software control.

With support for multiple common communications interfaces on-chip, MCF547X products require only the addition of memories and certain physical layer transceivers to be cost-effective system solutions for many applications, such as industrial routers, high-end POS terminals, building automation systems, and process control equipment.

MCF547X products require three supply voltages: 1.5V for the high-performance, low power, internal core logic, 2.5V for the DDR SDRAM bus interface, and, 3.3V for all other I/O functionality, including the PCI and FlexBus interfaces.

# 2    MCF547X Block Diagram

Figure 1 shows a top-level block diagram of the MCF547X products.
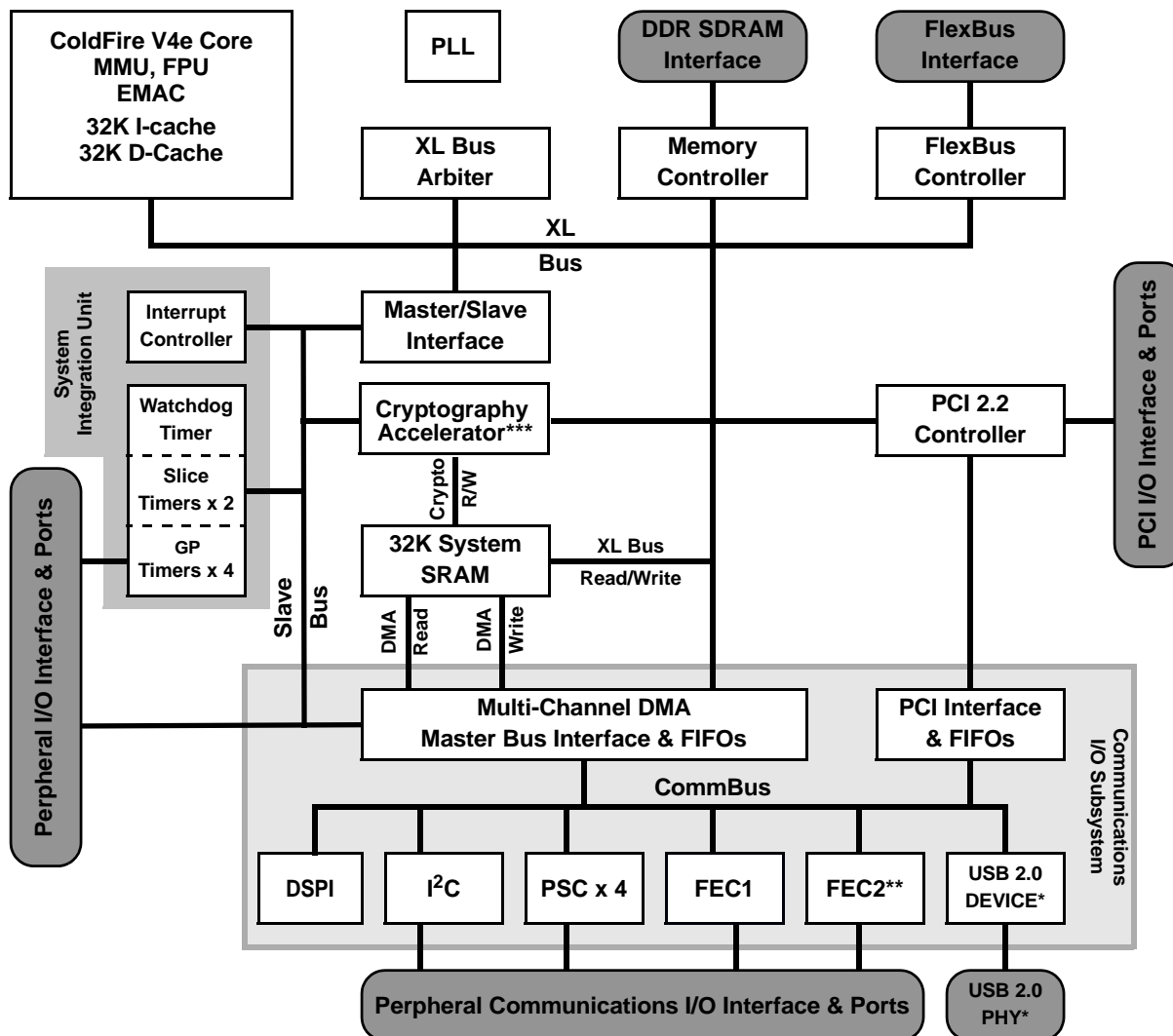


*Available in MCF5475, MCF5474, MCF5473 and MCF5472 devices.

**Available in MCF5475, MCF5474, MCF5471 and MCF5470 devices.

***Available in MCF5475, MCF5473, and MCF5471 devices.

**Figure 1. MCF547X Block Diagram**

# 3    MCF547X Family Products

Table 1 summarizes the products available within the MCF547X Product Family.

**Table 1. MCF547X Family Products**

| Product | Performance | Features | Package | Temperature Range |
|---|---|---|---|---|
| MCF5475 | 410 MIPS 266 MHz | Two 10/100 Ethernet Controllers USB 2.0 Device with Integrated PHY v2.2 PCI Controller DDR Memory Contoller Encryption Accelerator | 388 PBGA | 0 to 70 deg C |
| MCF5474 | 410 MIPS 266 MHz | Two 10/100 Ethernet Controllers USB 2.0 Device with Integrated PHY v2.2 PCI Controller DDR Memory Contoller | 388 PBGA | 0 to 70 deg C |
| MCF5473 | 308 MIPS 200 MHz | One 10/100 Ethernet Controller USB 2.0 Device with Integrated PHY v2.2 PCI Controller DDR Memory Contoller Encryption Accelerator | 388 PBGA | 0 to 70 deg C |
| MCF5472 | 308 MIPS 200 MHz | One 10/100 Ethernet Controller USB 2.0 Device with Integrated PHY v2.2 PCI Controller DDR Memory Contoller | 388 PBGA | 0 to 70 deg C |
| MCF5471 | 308 MIPS 200 MHz | Two 10/100 Ethernet Controllers v2.2 PCI Controller DDR Memory Contoller Encryption Accelerator | 388 PBGA | 0 to 70 deg C |
| MCF5470 | 308 MIPS 200 MHz | Two 10/100 Ethernet Controllers v2.2 PCI Controller DDR Memory Contoller | 388 PBGA | 0 to 70 deg C |

# 4    MCF547X Family Features

- ColdFire V4e Core
    - Limited superscalar V4 ColdFire processor core
    - Up to 266 MHz peak internal core frequency (410 MIPS (Dhrystone 2.1) @ 266 MHz)
    - Harvard architecture
        - 32-Kbyte instruction cache
        - 32-Kbyte data cache
    - Memory Management Unit (MMU)
        - Separate, 32-entry, fully-associative instruction and data translation lookahead buffers
    - Floating point unit (FPU)
        - Double-precision support that conforms to IEE-754 standard
        - 8 floating point registers

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- Internal master bus (XLB) arbiter
  — High performance split address and data transactions
  — Support for various parking modes
- 32-bit double data rate (DDR) synchronous DRAM (SDRAM) controller
  — 66–133 MHz operation
  — Supports both DDR and SDR DRAM
  — Built-in initialization and refresh
  — Up to four (4) chip selects enabling up to one (1) GB of external memory
- Version 2.2 peripheral component interconnect (PCI) bus
  — 32-bit target and initiator operation
  — Support for up to five (5) external PCI masters
  — 33–66 MHz operation with PCI bus to XLB divider ratios of 1:1, 1:2, and 1:4
- Flexible multi-function external bus (FlexBus)
  — Supports operation with:
    – non-multiplexed 32-bit address and 32-bit data (32-bit address muxed over PCI bus)
    – multiplexed 32-bit address and 32-bit data
    – multiplexed 32-bit address and 16-bit data
    – non-multiplexed 24-bit address and 8-bit data
    – non-multiplexed 16-bit address and 16-bit data
  — Provides a glueless interface to boot Flash/ROM, SRAM, and peripheral devices
  — Up to six (6) chip selects
  — 33–66 MHz operation
- Communications I/O subsystem
  — Intelligent 16 channel DMA controller, with support for
  — Dedicated DMA channels for receive and transmit on all subsystem peripheral interfaces
  — Up to two (2) 10/100 Mbps fast Ethernet controllers (FECs) each with separate 2-Kbyte receive and transmit FIFOs
  — Universal serial bus (USB) version 2.0 device controller
    – Support for one (1) control and six (6) programmable endpoints - interrupt, bulk or isochronous
    – 4 Kbytes of shared endpoint FIFO RAM and 1 Kbyte of endpoint descriptor RAM
    – integrated physical layer interface
  — Up to four (4) programmable serial controllers (PSCs) each with separate 512-byte receive and transmit FIFOs for UART, USART, modem, codec, and IrDA 1.1 interfaces
  — I$^2$C peripheral interface
  — DMA Serial Peripheral Interface (DSPI)

- Optional Cryptography accelerator module
  - Execution units for:
    - DES/3DES block cipher
    - AES block cipher
    - RC4 stream cipher
    - MD5/SHA-1/SHA-256/HMAC hashing
    - Random Number Generator compliant with FIPS 140-1 standards for randomness and non-determinism
  - Dual-channel architecture permits single-pass encryption and authentication
- 32-Kbyte system SRAM
  - Arbitration mechanism shares bandwidth between internal bus masters (CPU, Cryptography Accelerator, PCI, and DMA)
- System integration unit (SIU)
  - Interrupt controller
  - Watchdog timer
  - Two (2) 32-bit slice timers for periodic alarm and interrupt generation
  - Up to four (4) 32-bit general-purpose timers with capture, compare, and PWM capability
  - General-purpose I/O ports multiplexed with peripheral pins
- Debug and test features
  - Core debug support via ColdFire background debug mode (BDM) port
  - Chip debug support via JTAG/ IEEE 1149.1 test access port
- PLL and clock generator
  - 30 to 66.67 MHz input frequency range
- Operating Voltages
  - 1.5V internal logic
  - 2.5V DDR SDRAM bus I/O
  - 3.3V PCI, FlexBus, and all other I/O
- Estimated power consumption
  - <1.5W (388 PBGA)
  - <1.0W (324 PBGA)

# 5    ColdFire V4e Core Overview

The ColdFire V4e core is a variable-length RISC, clock multiplied core that includes a Harvard memory architecture, branch cache acceleration logic, and limited superscalar dual-instruction issue capabilities. The limited superscalar design approaches dual-issue performance with the cost of a scalar execution pipeline.

The ColdFire V4e processor core is comprised of two separate pipelines that are decoupled by an instruction buffer. The four-stage Instruction Fetch Pipeline (IFP) prefetches the instruction stream, examines it to predict changes of flow, partially decodes instructions, and packages fetched data into instructions for the Operand Execution Pipeline (OEP). The IFP can prefetch instructions before the OEP needs them, minimizing the wait for instructions. The instruction buffer is a 10 instruction, first-in-first-out (FIFO) buffer that decouples the IFP and OEP by holding prefetched instructions awaiting execution in the OEP. The OEP includes five pipeline stages: the first stage decodes instructions and selects operands (DS); the second stage generates operand addresses (OAG) The third and fourth stages fetch operands (OC1 and OC2), and the fifth stage executes instructions (EX).

The ColdFire V4e processor contains a double precision Floating Point Unit (FPU). The FPU conforms to the American National Standards Institute (ANSI)/Institute of Electrical and Electronics Engineers (IEEE) *Standard for Binary Floating-Point Arithmetic* (ANSI/IEEE Standard 754). The FPU operates on 64-bit, double-precision floating-point data and supports single-precision and signed integer input operands. The FPU programming model is like that in the MC68060 microprocessor. The FPU is intended to accelerate the performance of certain classes of embedded applications, especially those requiring high-speed floating-point arithmetic computations.

The ColdFire V4e processor also incoporates the ColdFire Memory Management Unit (MMU), which provides virtual-to-physical address translation and memory access control. The MMU consists of memory-mapped control, status, and fault registers that provide access to translation-lookaside buffers (TLBs). Software can control address translation and access attributes of a virtual address by configuring MMU control registers and loading TLBs. With software support, the MMU provides demand-paged, virtual addressing.

The ColdFire V4e core implements the ColdFire Instruction Set Architecture Revision B with support for Floating Point instructions. Additionally, the ColdFire V4e core includes the enhanced multiply-accumulate unit (EMAC) for improved signal processing capabilities. The EMAC implements a 4-stage execution pipeline, optimized for 32 x 32 bit operations, with support for four 48-bit accumulators. Supported operands include 16- and 32-bit signed and unsigned integers as well as signed fractional operands as well as a complete set of instructions to process these data types. The EMAC provides superb support for execution of DSP operations within the context of a single processor at a minimal hardware cost.

# 6    Debug Module - BDM

The ColdFire processor core debug interface is provided to support system debugging in conjunction with low-cost debug and emulator development tools. Through a standard debug interface, users can access real-time trace and debug information. This allows the processor and system to be debugged at full speed without the need for costly in-circuit emulators.

The on-chip breakpoint resources include a total of 6 programmable registers—a set of address registers (with two 32-bit registers), a set of data registers (with a 32-bit data register plus a 32-bit data mask register), and one 32-bit PC register plus a 32-bit PC mask register. These registers can be accessed through the dedicated debug serial communication channel or from the processor's supervisor mode programming model. The breakpoint registers can be configured to generate triggers by combining the address, data, and

PC conditions in a variety of single or dual-level definitions. The trigger event can be programmed to generate a processor halt or initiate a debug interrupt exception.

To support program trace, the Version 4 debug module provides a processor status (PSTDDATA[7:0]) port. This bus and the PSTCLK output provide execution status, captured operand data, and branch target addresses defining processor activity at the CPU's clock rate.

# 7    JTAG

The MCF547X family supports circuit board test strategies based on the Test Technology Committee of IEEE andthe Joint Test Action Group (JTAG). The test logic includes a test access port (TAP) consisting of a 16-state controller, an instruction register, and three test registers (a 1-bit bypass register, a 256-bit boundary-scan register, and a 32-bit ID register). The boundary scan register links the device's pins into one shift register. Test logic, implemented using static logic design, is independent of the device system logic. The MCF547X implementation can do the following:

- Perform boundary scan operations to test circuit board electrical continuity
- Sample MCF547X system pins during operation and transparently shift out the result in the boundary scan register
- Bypass the MCF547X for a given circuit board test by effectively reducing the boundary-scan register to a single bit
- Disable the output drive to pins during circuit-board testing
- Drive output pins to stable levels

# 8    On-Chip Memories

## 8.1    Caches

There are two independant caches associated with the ColdFire V4e core complex: a 32 Kbyte instruction cache and a 32 Kbyte data cache. Caches improve system performance by providing single-cycle access to the instruction and data pipelines. This decouples processor performance from system memory performance, increasing bus availability for on-chip DMA or external devices.

## 8.2    32KB System SRAM

The SRAM module provides a general-purpose 32 Kbyte memory block that the ColdFire core can access in a single cycle. The location of the memory block can be set to any 32 Kbyte address boundary within the 4-Gbyte address space. The memory is ideal for storing critical code or data structures, for use as the system stack, or for storing FEC data buffers. Because the SRAM module is physically connected to the processor's high-speed local bus, it can quickly service core-initiated accesses or memory-referencing commands from the debug module.

The SRAM module is also accessible by multiple non-core bus masters, such as the DMA controller, the encryption accelerator, and the PCI Controller.

# 9 PLL and Chip Clocking Options

MCF547X products contain an on-chip PLL capable of accepting input frequencies from 30 to 66.67 MHz. Table 2 contains the frequencies of the system buses for the members of the MCF547X family under various Core/SDRAM/PCI/Flexbus clocking options.

**Table 2. MCF547X Family Clocking Options**

| Core (MHz) | Internal and SDRAM Bus Frequency (MHz) | PCI and FlexBus Frequency (MHz) | Clock Ratio |
|---|---|---|---|
| 266 | 133 | 66 | 1:2 |
| 266 | 133 | 33 | 1:4 |
| 200 | 100 | 50 | 1:2 |

# 10 Communications I/O Subsystem

## 10.1 DMA Controller

The communications subsystem contains an intelligent DMA unit that provides front-line interrupt control and data movement interface via a separate peripheral bus to the on-chip peripheral functions, leaving the processor core free to handle higher level activities. This concurrent operation enables a significant boost in overall systems performance.

The communications subsystem can support up to sixteen (16) simultaneously enabled DMA tasks, with support for up to two (2) external DMA requests. It uses internal buffers to prefetch reads and post writes such that bursting is used whenever possible. This optimizes both internal and external bus activity. The following communications and computer control peripheral functions are integrated and controlled by the communications subsystem:

- Up to two (2) 10/100 Mbps Fast Ethernet Controllers (FECs)
- Optional universal serial bus (USB) version 2.0 device controller
- Up to four (4) programmable serial controllers (PSCs)
- $I^2C$ peripheral interface
- DMA Serial Peripheral Interface (DSPI)

## 10.2 10/100 Ethernet Controller

The Ethernet controller supports the following standard MAC/PHY interfaces:10/100 Mbps IEEE 802.3 MII, and 10 Mbps 7-wire interface. The controller is full duplex, supports a programmable max frame length and retransmission from the transmit FIFO following a collision.

- Support for different Ethernet physical interfaces:
  — 100 Mbps IEEE 802.3 MII
  — 10 Mbps IEEE 802.3 MII

— 10 Mbps 7-wire interface

- IEEE 802.3 full duplex flow control.

- Support for full duplex operation (200 Mbps throughput) with a minimum system clock frequency of 50Mhz.

- Support for half duplex operation (100 Mbps throughput) with a minimum system clock frequency of 25Mhz.

- Retransmit from transmit FIFO following collision.

- Internal Loop back for diagnostic purposes.

## 10.3  USB 2.0 Device (Universal Serial Bus)

The USB module implementation on the MCF547X Product Family provides all the logic necessary to process the USB protocol as defined by version 2.0 specification for peripheral devices.

- Supports high speed operation up to 480 Mbps, full speed operation at 12 Mbps, and low speed operation at 1.5 Mbps.

- Physical interface on chip.

- Bulk, Interrupt and Isochronous transport modes.

- Six (6) programmable in/out endpoints and one (1) control endpoint

- 4 Kbytes of shared endpoint FIFO RAM and 1 Kbyte of endpoint descriptor RAM

## 10.4  Programmable Serial Controllers (PSC's)

The MCF547X Product Family supports up to four Programmable Serial Controllers (PSC's) that can be independantly configured to operate in the following modes:

- Universal Asynchronous Receiver Transmitter (UART) mode
    - 5,6,7,8 bits data plus parity
    - Odd, even, none, or force parity
    - Stop bit width programmable in 1/16 bit increments
    - Parity, framing, and overrun error detection
    - Automatic PSC_CTS and PSC_RTS modem control signals
- IrDA 1.0 SIR mode (SIR)
    - Baud rate range: 2400 to 115200 bps
    - Selectable pulse width: either 3/16 bit duration or 1.6 us
- IrDA 1.1 MIR mode (MIR)
    - Baud rate: 0.576 Mbps or 1.152 Mbps.
- IrDA 1.1 FIR mode (FIR)
    - Baud rate: 4.0 Mbps
- 8-bit soft modem mode (modem8)

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- 16-bit soft modem mode (modem16)
- AC97 soft modem mode (AC97)

Each PSC supports both synchronous (USART) and asynchronous (UART) protocols. The PSC's can be used to interface to external full function modems or external codecs for soft modem support, as well as IrDA 1.1 or 1.0 interfaces. Both 8 bit and 16 bit data widths are supported. PSC's can be configured to support 1200 baud POTS modem, V.34 or V.90 protocols. The standard UART interface supports connection to an external terminal/computer for debug support.

Table 3 indicates the number of PSC's on each member of the MCF547X Product Family.

**Table 3. PSCs for each member of MCF547X Product Family**

| MCF5475<br>MCF5474 | MCF5473<br>MCF5472 | MCF5471<br>MCF5470 |
|---|---|---|
| Up to 4 PSCs | Up to 4 PSCs | Up to 3 PSCs |

# 10.5  I$^2$C (Inter Integrated Circuit)

The MCF547X Product Family provides an I$^2$C two-wire, bi-directional serial bus for on-board communication.

- Multi-master operation with arbitration and collision detection
- Calling address recognition and interrupt generation
- Automatic switching from master to slave on arbitration loss
- Software selectable acknowledge bit
- Start and stop signal generation and detection
- Bus busy status detection

# 10.6  DMA Serial Peripheral Interface (DSPI)

The DSPI block operates as a basic SPI block with FIFOs providing support for external queue operation. Data to be transmitted and data received reside in separate FIFOs. The FIFOs can be popped and pushed by host software or by the system DMA controller. The DSPI supports these SPI features:

- Full-duplex, three-wire synchronous transfers
- Master and Slave Mode - 2 peripheral chip selects in Master Mode
- DMA support

# 11    DDR SDRAM Memory Controller

The DDR SDRAM memory controller is a glueless interface to both SDR and DDR memories.  The module uses a 32 bit memory port and can address a maximum of 1 Gbyte of data with sixteen 64M x 8 (512-Mbit) devices, 4 per chip select. The controller supplies two clock lines and a respective clock(bar) lines to help minimize system complexity when using DDR.  The module supports either DDR or SDR but not both. This is due to voltage differences between the memory technologies. The supported memory

clock rate is up to 133 MHz.  At this memory clock rate, DDR memory can receive data at an effective rate of 266 MHz.

- Support for up to 13 lines of row address, 11 lines of column address, 2 lines of bank address, and up to 4 chip selects.

- Memory bus width fixed at 32 bits.

- Support for page mode to maximize the data rate.  Page mode remembers active pages for all four chip selects.

- Support for sleep mode and self refresh.

- Cache Line reads can use critical word first.  These reads can start in the center of a burst and will wrap to the beginning.  This allows the processor quicker access to a needed instruction.

All on-chip bus masters have access to DRAM.  This includes PCI, the ColdFire V4e Core, the Cryptography Accelerator, and the DMA controller.

Table 4 indicates the amount of external memory supported on each member of the MCF547X Product Family

**Table 4. MCF547X External Memory Support**

| MCF5475<br>MCF5474 | MCF5473<br>MCF5472 | MCF5471<br>MCF5470 |
|---|---|---|
| Four (4) Chip Selects<br>Up to 1GB External Memory | Four (4) Chip Selects<br>Up to 1GB External Memory | Two (2) Chip Selects<br>Up to 512MB External Memory |

# 12    Peripheral Component Interconnect (PCI)

The PCI controller is a PCI 2.2 compliant bus controller and arbiter.  The PCI bus is capable of 66 MHz operation with a 32 bit address/data bus.  Table 5 indicates the number of external masters supported for each member of the MCF547X product Family.

**Table 5. PCI Controller External Master Support**

| MCF5475<br>MCF5474 | MCF5473<br>MCF5472 | MCF5471<br>MCF5470 |
|---|---|---|
| Up to 5 external masters | Up to 3 external masters | Up to 4 external masters |

The PCI module includes an inbound FIFO to increase performance when using an external bus master. The bus can address all 4GB of PCI addressable space.

The PCI bus is also multiplexed with the Flexible Local Bus (FlexBus) address lines - if 32-bit non-muxed local address and data is required it can be obtained at the expense of utilizing the PCI bus.

When implemented, the PCI controller acts as the central resource, bus arbiter, and configuring master on the PCI bus.

# 13    Flexible Local Bus (FlexBus)

The FlexBus module is intended to provide the user with basic functionality to interface to target devices. The FlexBus interface is a multiplexed or non-multiplexed bus, with an operating frequency from 33 to 66 MHz.  The Flexbus is targeted to support external Flash memories, boot ROMs, gate-array logic, or other simple target interfaces. There are up to six (6) chip selects supported by the FlexBus.

Possible combinations of address and data bits are:

- non-multiplexed 32-bit address and 32-bit data (32-bit address muxed over PCI bus - PCI not usable)
- multiplexed 32-bit address and 32-bit data (PCI usable)
- multiplexed 32-bit address and 16-bit data
- non-multiplexed 24-bit address and 8-bit data
- non-multiplexed 16-bit address and 16-bit data

The non-multiplexed 32-bit address and 32-bit data mode is determined at chip reset. All other modes listed are determined on a chip select by chip select basis.

# 14    Cryptography Accelerator

As consumers and businesses have embraced the Internet, the need for secure point-to-point communications across what is an entirely insecure network has been met by the development of a range of standard protocols. Computer cryptography fundamentally involves calculations with very large numbers. Personal computers have sufficient processing power to implement these algorithms entirely in software. When placed upon the embedded devices typically used for routing and remote access functions, this same computational burden will drag the throughput of a 100 Mbps Ethernet interface down to 10 Mbps.

Hardware acceleration of common cryptography algorithms is the solution to the computational bandwidth requirements of Internet security standards. Discrete solutions currently address this problem, but the next logical step is to integrate a cryptography accelerator on an embedded processor, such as the MCF547X family.

Freescale has developed the Cryptography Accelerator Module on the MCF547X family for this purpose. This block accelerates the core cryptography algorithms that underlie standard Internet security protocols like SSL/TLS, IPSec, IKE, and WTLS/WAP.

- The Cryptography Accelerator includes execution units for:
  — DES/3DES block cipher
  — AES block cipher
  — RC4 stream cipher
  — MD5/SHA-1/SHA-256/HMAC hashing
  — Random Number Generator compliant with FIPS 140-1 standards for randomness and non-determinism

- Dual-channel architecture permits single-pass encryption and authentication

# 15 System Integration Unit (SIU)

## 15.1 Timers

The MCF547X family integrates several timer functions required by most embedded systems. Two internal Slice Timers are provided to create short cycle periodic interrupts, typically utilized for RTOS scheduling and alarm functionality. A WatchDog timer is included which will reset the processor if not regularly serviced, catching software hang-ups. Up to four 32-bit general purpose timers are included, which are capable of input capture, output compare, and PWM functionality.

## 15.2 Interrupt Controller

The interrupt controller on the MCF547X family can support up to 63 interrupt sources. The interrupt controller is organized as 7 levels with 9 interrupt sources per level. Each interrupt source has a unique interrupt vector, and 56 of the 63 sources of a given controller provide a programmable level [1-7] and priority within the level.

- Support for up to 63 interrupt sources organized as follows:
    — 56 fully-programmable interrupt sources
    — 7 fixed-level interrupt sources
- Seven external interrupt signals
- Unique vector number for each interrupt source
- Ability to mask any individual interrupt source or all interrupt sources (global mask-all)
- Support for hardware and software interrupt acknowledge (IACK) cycles
- Combinatorial path to provide wake-up from low power modes

## 15.3 General Purpose I/O

All peripheral I/O pins on the MCF547X family are muxed with GPIO, adding flexibility and usability to all signals on the chip.

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