MAC71*x*1 Microcontroller Device Product Brief

Covers MAC7101, MAC7111, MAC7121, MAC7131, MAC7141

32-bit Embedded Controller Division

MAC71*x*1 microcontrollers (MCUs) are members of a pin-compatible family of 32-bit Flash-memory-based devices developed specifically for embedded automotive applications. The pin-compatible family concept enables users to select between different memory and peripheral options for scalable designs. All MAC71*x*1 devices are composed of an ARM7TDMI-S™ 32-bit central processing unit, 512 Kbytes of high performance embedded Flash memory for program storage, an optional 32 Kbytes of embedded Flash for data and/or program storage, and 32 Kbytes of RAM.

As shown in Table 1 and Figure 1, the MAC71*x*1 family is implemented with a variety of on-chip peripherals. An enhanced DMA (eDMA) controller executes in parallel with the CPU to improve the performance of data transfers between memory and many of the peripherals. DMA transfers may be triggered by various peripheral events, such as data frame transmission or reception, elapsed timer periods, and analog-to-data conversion completions. The peripheral set includes enhanced asynchronous serial communications interfaces (eSCI) with Local Interconnect Network (LIN) support hardware to reduce interrupt overhead, serial peripheral interfaces (DSPI) with flexible chip selects and fast baud

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Table 1. MAC71*x*1 Device Derivatives

		MAC7101	MAC7111	MAC7121	MAC7131	MAC7141
Program Flash		512 Kbytes				
Data Flash		32 Kbytes				
SRAM		32 Kbytes				
External Bus		—	Yes	—	Yes	—
ATD Modules[1]	A	Yes	Yes	Yes	Yes	Yes
	B	Yes	—	—	Yes	—
CAN Modules	A	Yes	Yes	Yes	Yes	Yes
	B	Yes	Yes	Yes	Yes	Yes
	C	Yes	Yes	Yes	Yes	—
	D	Yes	Yes	Yes	Yes	—
eSCI Modules	A	Yes	Yes	Yes	Yes	Yes
	B	Yes	Yes	Yes	Yes	Yes
	C	Yes	Yes	Yes	Yes	—
	D	Yes	Yes	Yes	Yes	Yes
DSPI Modules	A	Yes	Yes	Yes	Yes	Yes
	B	Yes	Yes	Yes[2]	Yes	Yes
I^2C Module		Yes	Yes	Yes	Yes	Yes
eMIOS Module		16 channels, 16-bit				
Timer Module		10 channels, 24-bit				
GPIO Pins (max.)[3]		112	112	85	128	72
Package		144 LQFP	144 LQFP	112 LQFP	208 MAP BGA	100 LQFP

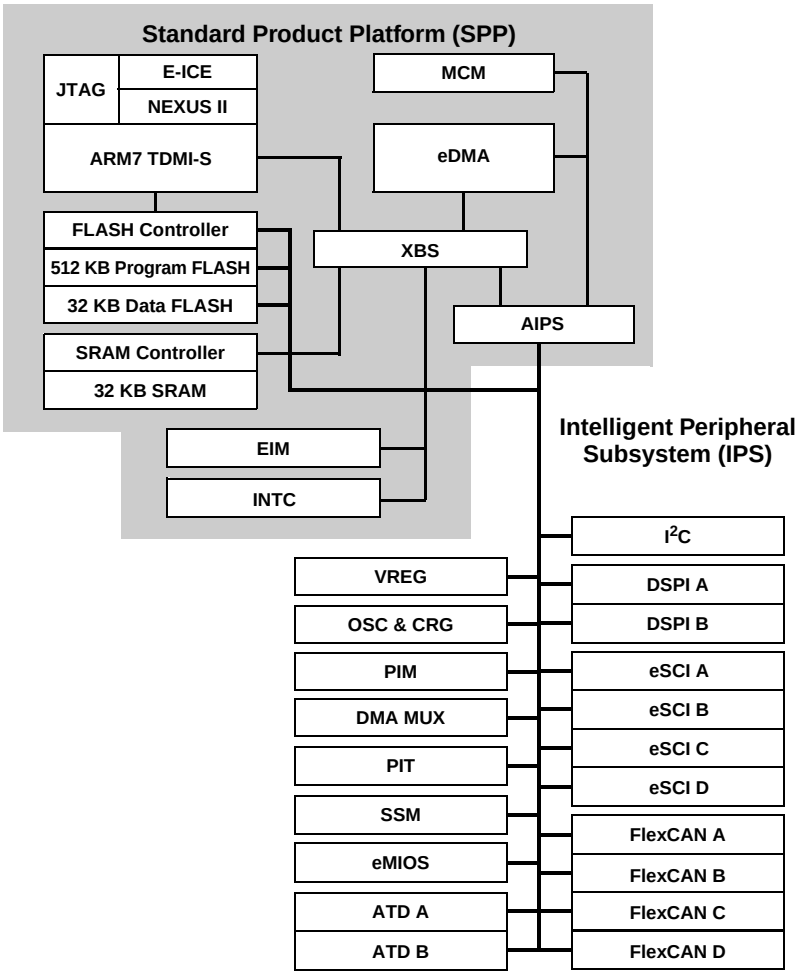
NOTES:
1. 16 channels, 8/10-bit, per module.
2. Only three chip select signals available.
3. Early mask set devices (L49P) reduce these values by one.

rate switching, inter-integrated circuit (I^2C™) bus controllers, FlexCAN interfaces with flexible message buffering, an enhanced modular I/O subsystem (eMIOS) with sixteen high-performance 16-bit timers, one or two sixteen-channel 10-bit analog-to-digital converters (ATD), general-purpose timers (Programmable Interrupt Timer (PIT)) and two special-purpose timers (Real Time Interrupt (RTI) and Software Watchdog Timer (SWT)). The peripherals share a large number of general purpose input-output (GPIO) pins, all of which are bidirectional and available with interrupt capability to trigger wake-up from low-power chip modes.

Internal data paths between the CPU core, eDMA, memory and peripherals are all 32 bits wide, further improving performance for 32-bit applications. The MAC7111 and MAC7131 also offer a 16-bit wide external data bus with 22 address lines, allowing access of up to 4 MBytes of external address space. The inclusion of a programmable PLL module allows power consumption and performance to be adjusted to suit operational requirements. Both E-ICE and Nexus 2 interfaces are implemented to support development and debug tool chains.

MAC71*x*1 devices include an on-chip multi-output voltage regulator, thus requiring only a single external 3.3V to 5V power supply. The maximum operating range of devices in the family covers a junction temperature of –40° C to 150° C and CPU clock frequencies up to 50 MHz (below 105° C, frequency is limited to 40 MHz @ 150° C). Packaging options range from 100-pin LQFP up to 208-pin MAP BGA.

1 Block Diagram



Note: Refer to Table 1 for details of peripheral and memory configurations

Figure 1. MAC71x1 Device Block Diagram

2 Features

As shown in Figure 1, MAC7100 family devices are organized into two major blocks:

- Standard Product Platform (SPP) — The SPP consists of the ARM7TDMI-S processor core and an enhanced direct memory access controller connected to a high-performance 32-bit bus through a cross-bar bus switch to the rest of the chip modules. The SPP also contains an interrupt controller, SRAM controller, Flash memory controller, external bus interface, peripheral bus bridge, and miscellaneous control module.
- Intelligent Peripheral Subsystem (IPS) — The IPS consists of the voltage regulator, oscillator, clock and reset generator, port integration module, DMA request multiplexer, analog to digital converter((s)), enhanced modular I/O subsystem, enhanced serial communications controllers, serial peripheral interface(s), FlexCAN controller(s), an inter-integrated circuit (I^2C) bus controller, programmable interrupt timer, and system services module.

The primary features of MAC71*x*1 integrated processors include the following:

- General MAC7100 family features
  - Up to 50 MHz operating frequency
  - RISC core, eDMA, and memory connected via high performance 32-bit bus
  - Separate 32-bit bus interface for slower system peripherals
  - External bus interface available to support off-chip devices (on selected devicesMAC7111 and MAC7131 only)
- 32-bit ARM7TDMI-S RISC core
  - Supports 32-bit and 16-bit (THUMB) instruction sets for code size efficiency
  - 32 bit wide data path
  - Alternate general-purpose registers
  - Byte (8-bit), halfword (16-bit), and word (32-bit) data types supported
- Enhanced Direct Memory Access (eDMA) and Channel Multiplexer (DMA MUX)
  - Supports transfers between system memories, external devices, peripheral modules (ATD, DSPI, eMIOS, eSCI, and I^2C), and general-purpose I/O using a dual-address transfer protocol
  - DMA MUX allows assignment of any DMA request source to any available eDMA channel
  - Programmable transfer control descriptors stored in local eDMA memory
  - Programmable source and destination address with configurable offset
  - Programmable transfer size and nesting via 32-bit major and 16-bit minor loop counters
  - Different final source and destination addresses allow circular queue operation
  - Programmable priority levels for each channel
  - Bandwidth control for each channel
  - Independently programmable read/write sizes
  - Periodic triggering of up to 8 channels
- Memory options
  - 512 Kbyte program Flash EEPROM
    - 50 MHz single-cycle non-sequential access for aligned halfword and aligned word data
    - State machine controlled program/erase operations
    - Internal programming voltage generator
    - Small Flash sector protection sizes
    - Configurable flexible Flash protection fields
    - Protection violation flag
    - 10,000 program / erase cycle endurance
    - 15-year data retention
  - 32 Kbyte data Flash EEPROM
    - 16-bit wide memory accessed via peripheral bus interface
    - Relocatable to page zero to provide data Flash boot operation
    - State machine controlled program/erase operations
    - Internal programming voltage generator
    - Up to 8 protected sectors in the data Flash
    - 10,000 program / erase cycle endurance
    - 15-year data retention
  - 32 Kbyte RAM
    - Single cycle accesses to RAM for byte, halfword, and word reads and writes

- Interrupt Controller (INTC)
  - 64 vectored interrupt sources
  - 44 peripheral, 17 DMA, 1 software watchdog timer, 2 external sources
  - 16 programmable interrupt priorities for every source, even in low-power modes
  - Multiple level interrupt nesting, with hardware support for first nesting level
  - Normal and Fast interrupt support
- General purpose input/output
  - Up to 128 port pins shared with peripherals
  - All ports are 16 bits wide, with pins bidirectional and independently selectable
  - Wake-up interrupt available on all port pins
- Analog-to-Digital Converter(s) (ATD)
  - One or two ATD modules
  - 16 analog input channels per ATD module
  - 10-bit resolution with ± 2 counts accuracy
  - 7µS minimum conversion time
  - Internal sample and hold circuitry
  - Programmable input sample time for various source impedances
  - Queued conversion sequences supported by eDMA controller
  - Unused analog channels can be used as digital I/O
  - External and on-chip sample triggers, including periodic triggering via the PIT module
  - Synchronized sampling between ATD modules using external or on-chip triggers
- CAN 2.0 software compatible modules (FlexCAN)
  - Two or four CAN modules
  - Full implementation of the CAN 2.0 protocol specification
  - Programmable bit rate up to 1M bps
  - Up to 32 flexible message buffers of 0 to 8 bytes data length for each module
  - All message buffers configurable for either Rx/Tx
  - Unused message buffer space can be used as general purpose RAM
  - Supports standard or extended messages
  - Time stamp, based on a 16-bit free-running counter
  - Maskable interrupts, including low-power mode wake up on bus activity
  - Programmable I/O modes
- Enhanced Modular I/O Subsystem (eMIOS)
  - 16 unified channels, each of which can be enabled for eDMA service
  - Three 16-bit counter buses, with synchronization between timebases
  - One global prescaler plus prescaler available on each channel
  - Channels can be individually disabled to assist with power saving
  - Fourteen channel operating modes available:
    - General-purpose input/output
    - Single-action input capture
    - Single-action output compare
    - Input pulse width measurement
    - Input period measurement
    - Double-action output compare

  - Pulse/edge accumulation
  - Pulse/edge counting
  - Quadrature decode
  - Windowed programmable time accumulation
  - Modulus counter
  - Output pulse width modulation
  - Output pulse width modulation, center aligned
  - Output pulse width and frequency modulation

- Serial Peripheral Interfaces (DSPI)
  - Two DSPI modules
  - Full duplex, synchronous transfers
  - Master or slave operation
  - Programmable master bit rates
  - Programmable clock polarity and phase
  - End-of-transmission interrupt flag
  - Flexible baud rates available
  - Programmable data frames from 4 bits to 16 bits
  - Up to 4 chip select lines enable 16 external devices to be selected using external multiplexer
  - Two DMA request signals per module for message frame support
  - Separate transmit and receive FIFOs for improved system performance
  - Queueing operation possible through use of eDMA controller channels
  - Fast switching between SPI slave device types via transfer attributes coupled with data
  - General purpose I/O functionality on pins when not used for DSPI
- Enhanced Serial Communications Interfaces (eSCI)
  - Three or four eSCI modules
  - Standard non-return-to-zero (NRZ) mark/space format
  - Full-duplex operation
  - Software selectable word length (8- or 9-bit words)
  - 10/11- or 13/14-bit break character formats available
  - 13-bit programmable baud-rate modulus counter
  - Separately enabled transmitter and receiver
  - Separate receiver and transmitter CPU interrupt requests
  - Programmable transmitter output polarity
  - Two receiver wake-up methods
  - Interrupt-driven operation with eight flags
  - Receiver framing error detection
  - Hardware parity checking
  - 1/16-bit time noise reduction
  - Two DMA request lines per module (one each for receive and transmit data)
  - Support for LIN bus protocol (version 1.2 and version 2.0).
    - Full LIN master node autonomous message frame handling.
    - Frame hardware significantly reduces interrupt overhead.
    - LIN message header generation.
    - Slave timeout detection.

  - Optional CRC message checking.
  - Detection and flagging of LIN errors.
- Inter-Integrated Circuit (I^2C) Bus module
  - Two wire bi-directional serial bus for on-board communications
  - Compatibility with I^2C Bus standard
  - Multi-master operation
  - Software-programmable for one of 256 different serial clock frequencies
  - Interrupt-driven byte-by-byte data transfer
  - Arbitration-lost interrupt with automatic mode switching from master to slave
  - Calling address identification interrupt
  - Start and stop signal generation/detection
  - Repeated START signal generation
  - Acknowledge bit generation/detection
  - Bus-busy detection
  - Two DMA request lines to receive and transmit data
- Periodic Interrupt Timer (PIT) Module
  - Independent timeout periods for each of the ten 24-bit timers
  - One real-time interrupt (RTI) timer to wake up the CPU in wait mode or pseudo-stop mode
  - Eight timers that can be configured to generate DMA trigger pulses
  - Four timers that can be configured to generate interrupts instead of triggers
  - Two timers that can be configured to generate ATD trigger pulses
- Miscellaneous Control Module (MCM)
  - Program-visible information regarding the device configuration and revision
  - SPP module configuration and reset status
  - Software watchdog timer with programmable, staged response
  - Wake-up control for exiting sleep modes
  - Cross-bar switch remapping
  - Address information for faulted memory accesses
- System Services Module (SSM)
  - Memory sizes and status
  - Device mode and security status
  - eDMA status
  - Reserved address space protection
  - Debug status port configuration
- Development support
  - Real-time instruction trace support via Nexus II interface
  - Selectable Nexus port position on 208-pin MAP BGA and 144-pin LQFP packaged device
  - ARM Embedded ICE debug interface
  - JTAG Test Access Port (TAP) interface
  - Debug mode access to CPU registers
  - Real Time memory access
  - Hardware Breakpoints

- Clock generation
  - Selectable Standard Pierce or low-power Amplitude Loop Controlled (ALC) Pierce oscillator
  - Phase-locked loop clock frequency multiplier
  - Self-clocking mode available in absence of external clock
  - Low power 0.5 to 16 MHz crystal oscillator reference clock
  - Clock generation and monitor, reset control, and software watchdog timer (SWT)
- I/O lines with 5 V input and drive capability, 5 V ATD converter inputs
- 2.5 V logic supply, with internal 5 V to 2.5 V Regulator
- 208-pin MAP BGA, 144-pin LQFP, 112-pin LQFP, and 100-pin LQFP package options

3 Modes of Operation

3.1 Chip Configuration Modes

Devices in the MAC700 family operate in several different modes, depending on the particular application and stage of development. There are 6 modes available for MAC71*x*1 devices, as determined via external input during reset as well as the security state of the on-chip program Flash memory. The selected mode affects the memory map, debug features, and security features:

- Normal Single-Chip Mode
  - All debug features available
  - Boot from program Flash
- Normal Expanded Mode
  - All debug features available
  - Boot from off-chip device using the external bus interface
  - Program and data Flash memory available
- Secured Single-Chip Mode
  - No debug features available
  - No external bus interface
  - Boot from program Flash
  - JTAG lockout recovery available
- Secured Expanded Mode
  - All debug features available.
  - Boot from off-chip device using the external bus interface
  - Program and data Flash memory not available
- Data Flash Boot Mode
  - All debug features available
  - Boot from data Flash
- Secured Data Flash Boot Mode
  - No debug features available
  - No external bus interface

— Boot from data Flash
— JTAG lockout recovery available

3.2 Low-Power Modes

There are three low-power modes available:

- Stop Mode (provides the lowest power consumption)

  This is a mode in which all MCU clocks are stopped for maximum power savings. Typically, when stop mode is requested, each module puts itself in a known state and then sends a stop acknowledge signal to inform the clock module that it can stop the clocks.
- Pseudo-Stop Mode

  The oscillator continues to run and most of the system and peripheral clocks are stopped. If the respective enable bits are set, the SWT and RTI will continue to run, otherwise they also stop.
- Doze Mode

  This is a mode in which the CPU bus is kept alive and a global doze mode request is sent to all peripherals asking them to enter low power mode. Typically, when doze mode is requested, each peripheral can be enabled to enter low power mode or continue normal operation.

4 Functional Overview

The following is a brief summary of the functional blocks in the MAC7100 devices. For more details refer to the *MAC7100 Microcontroller Family Reference Manual* (MAC7100RM).

4.1 32-bit ARM7TDMI-S RISC Core

The MAC7100 family is implemented with an ARM7 CPU. This is a 32-bit RISC core with a three-stage pipeline for high instruction throughput. The core used across the family is the ARM7TDMI-S, which supports both 32-bit and 16-bit (THUMB) instruction sets for optimum code density. No architectural modifications have been made to this core during implementation, enabling the MAC7100 family to remain compliant to the ARM ISA V4T and existing tool chains. The core is implemented to support big endian memory systems.

4.2 Enhanced Direct Memory Access (eDMA) and Channel Multiplexer (DMA MUX)

The implementation of the eDMA on the MAC7100 family is targeted towards cost-sensitive applications while providing a high level of functionality. The eDMA executes in parallel with the CPU, which enables transfers of data between the memory, peripherals, and off-chip devices with little intervention from the core; thus increasing system performance as well as simplifying software development. The eDMA is capable of performing complex data transfers with minimal intervention from a host processor via 16 programmable DMA channels. The hardware microarchitecture includes the eDMA engine (which performs source / destination address calculations and data movement operations), and a dedicated

memory array containing transfer control descriptors. The SRAM-based implementation is utilized to minimize overall module size.

4.3 External Interface Module (EIM)

The EIM connects the device to off-chip resources and is not available in all MAC71*x*1 packages. Two components make up this module: a user-programmable chip select module and the bus controller. The bus controller uses a simple, flexible bus protocol that supports a variety of external memory devices with little or no external logic needed, and is based on the external bus of the 68K/Coldfire® family of devices. All transfers on the external bus are controlled by the MCU masters (CPU or eDMA).

The EIM supports a normal three clock-cycle access, but a two cycle fast termination can also be used if the transfer acknowledge signal is asserted before the rising edge of the second CLKOUT cycle. The EIM also provides support for burst transfers of up to 16 bytes of data with the proper external support logic.

4.4 Common Flash Module (CFM)

The CFM provides 512 Kbytes of 32-bit program Flash memory and 32 Kbytes of 16-bit data Flash memory. The Flash memory serves as electrically erasable and programmable, non-volatile memory. It is ideal for program and data storage for single-chip applications allowing for field reprogramming without requiring external programming voltage sources.

4.5 Interrupt Controller (INTC)

MAC7100 family devices implement an Interrupt Controller (INTC) Module which supports 64 interrupt requests. The INTC is a highly-programmable controller, collecting interrupt requests, mapping the requests into 16 priority levels, and then signalling the ARM processor when a properly enabled unmasked request is active. In response to the service routine’s memory mapped interrupt acknowledge read cycle, the INTC returns a unique vector for each interrupt request and automatically manages masking of lower level requests. As any interrupt source can be assigned to any of the sixteen priority levels, and the INTC enables the definition of which priority levels are assigned to fast or normal interrupts, each interrupt source can be selected to generate either a fast or normal interrupt to the core by its assigned level.

4.6 Port Integration Module (PIM)

The Port Integration Module (PIM) provides the interface between the physical pins and either the general purpose I/O signals or the various peripherals which provide alternate signal functions. MAC71*x*1 devices implement up to 8 ports, each of which is 16-bits wide (all pins are not available in some packages). Each pin can be independently configured to be either in port mode or peripheral mode. When peripheral mode is selected, the pin’s output and configuration are both controlled by the peripheral module. Each pin is also capable of being used as an interrupt source with a filter available to help eliminate instances of noise-generated false interrupts. For some devices, GPIO Port H is available rather than Port C; the PIM enables swapping of Port H and Port C in the address map to assist transparent porting of code between various devices. Following a reset into any mode other than normal or secured expanded mode, all pins are

configured as general purpose inputs. Following a reset into normal or secured expanded mode, some pins are controlled by the External Interface Module (EIM) and are not available for general purpose functions.

In order to improve software performance, all pins can be controlled either in a port-wise or bit-wise manner in general purpose I/O mode. Registers are provided which allow each pin to be independently controlled by writing to a separate register. Mirror registers are also available to simplify read and write operations by accessing all pins in a port at one time.

4.7 Analog-to-Digital Converters (ATD)

The Analog-to-Digital Converter (ATD) Module is a 16-channel, multiplexed input, successive approximation analog-to-digital converter with a programmable resolution of 8 or 10 bits. MAC71*x*1 devices implement one or two Analog to Digital (ATD) Converter modules; refer to Table 1 for the ATD configuration of a specific device.

The ATD modules may be serviced by the eDMA in order to improve overall system performance. Two DMA request channels may be used by each of the ATDs (on devices with two ATDs): one channel per ATD to move conversion command words to the ATD command registers, and one channel per ATD to move conversion results out of the ATD result registers.The conversion command word is used to define parameters such as the mode of conversion, the channel to be converted and the length of the conversion. By defining a number of conversion words in the MCUs system memory, it is possible to build a predefined sequence of conversions which will be executed without the intervention of the CPU. It is also possible for the CPU to write the conversion command word and to read the conversion results directly without the need to use the eDMA.

MAC71*x*1 ATD modules include the ability to trigger a conversion sequence based on either an external signal or by one of two internal signals, SYSTRG0 or SYSTRG1. In order to use an external trigger source to initiate a conversion, any one of the analog channels can be used as an off-chip trigger. The internal trigger signal lines are connected to the Programmable Interrupt Timer (PIT), which provides two dedicated programmable 24-bit timers to trigger the ATD. The counter associated with the SYSTRG*n* signals can be programmed with the desired conversion trigger periods. This counter will count down from the preloaded value to zero at the rate defined by the system clock frequency. When the counter reaches zero the trigger signal is asserted to the ATD, then it is reloaded and the count down continues. For those devices that implement two ATD modules, when it is necessary to perform synchronous conversion by both, ATD_A and ATD_B can use the same external source, with one channel from each module assigned as the input for this trigger. Alternatively, both modules can use the same internal system trigger.

4.8 CAN 2.0 Software Compatible (FlexCAN) Modules

There are two or four FlexCAN modules on MAC71*x*1 devices; refer to Table 1 for the number of FlexCAN channels implemented on a specific device. The CAN protocol is primarily, but not only, designed to be used as a vehicle serial data bus, meeting the specific requirements of this application: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness, and required bandwidth. The FlexCAN module is a full implementation of the CAN protocol specification, Version 2.0 B, which supports both standard and extended message frames. A flexible number of message buffers (up to 32 MBs)

is also supported, which are stored in an embedded RAM dedicated to the FlexCAN module (up to 544 bytes capability).

On MAC7100 devices, the clock source for the FlexCAN can be selected to be derived either from the PLL clock or the oscillator clock. The FlexCAN also implements a low pass filter which can be used to wake up the device when activity is detected on the bus, while also enabling rejection of bus noise to help eliminate instances of false wake. MAC7100 devices implement 32 mailboxes on each CAN module.

4.9 Enhanced Modular I/O Subsystem (eMIOS)

The Enhanced Modular I/O Subsystem (eMIOS) provides functionality to generate or measure time-based events. The eMIOS module implemented on MAC7100 family devices has 16 unified timer channels (UCs), each with a 16-bit counter. Each UC is identical and can be configured to provide a wide range of timer functions. The module implements 3 counter busses for inter-channel synchronization and sharing common time bases.

Each of the UCs has a single input/output signal associated with it, resulting in a module with 16 external signals available for the user. The eMIOS module can be independently disabled. Disabling the module turns off the clock to the module, although some of the module registers remain available to be accessed by the core via the peripheral bus.

4.10 Serial Peripheral Interfaces (DSPI)

MAC71*x*1 devices implement two (Deserial) Serial Peripheral Interface modules (DSPI). Only the SPI configuration is implemented in the MAC7100 family of devices. Each DSPI supports up to four peripheral chip select lines, offering selection of up to 4 external devices without external hardware, expandable to 16 with an external demultiplexer. One of the chip select signals can be used to provide a strobe for the other chip selects in order to eliminate decoding glitches generated when the chip selects change. This allows glitch-free selection of up to 8 external devices via external hardware.

The DSPI is implemented with separate transmit and receive FIFOs with a depth of up to four entries. These FIFOs can be accessed either by the CPU or the eDMA to enable queued operations to be performed. Each DSPI has a separate DMA request channel for the transmit and the receive sides of the module. For queued operations the SPI queues reside in system RAM external to the DSPI. Data transfers between the queues and the DSPI FIFOs are accomplished through the use of the eDMA controller or through host software. Each queue entry contains both configuration information and data, enabling fast baud rate and chip select switching between frames with no CPU overhead and no SPI channel dead time.

4.11 Enhanced Serial Communications Interfaces (eSCI)

There are three or four Enhanced Serial Communications Interfaces (eSCI) implemented on MAC71*x*1 devices. Refer to Table 1 for the number of eSCI channels implemented on a specific device. The eSCI provides full duplex, asynchronous, NRZ serial communication with remote devices, including other MPUs. The eSCI transmitter and receiver operate independently, although they use the same baud rate generator. The CPU monitors the status of the eSCI, writes the data to be transmitted, and processes received data. The enhancement offered by this module over other Freescale SCIs is the inclusion of

additional features which support a Local Interconnect Network (LIN) bus master, and complies with the LIN 2.0 specification. LIN master mode enables handling message frames rather than individual data packets, thus significantly reducing interrupt overhead (for example, from 13 individual interrupts to one).

4.12 Inter-Integrated Circuit (I^2C) Bus Module

The Inter-Integrated Circuit Bus (I^2C or IIC) is a two-wire bidirectional serial bus that provides a simple and efficient method of data exchange between devices. It minimizes the number of external connections between devices and does not require an external address decoder. The I^2C bus is suitable for applications requiring occasional communications over a short distance between a number of devices. It also provides flexibility, allowing additional devices to be connected to the bus for further expansion and system development. The interface is designed to operate at up to 100 Kbps with maximum bus loading and timing. MAC7100 family devices are capable of operating at higher baud rates, up to a maximum of the module clock divided by 20, with reduced bus loading. The maximum communication length and the number of devices that can be connected are limited by the maximum bus capacitance of 400 pF.

4.13 Periodic Interrupt Timer (PIT) Module

The PIT is an array of timers that can be used to generate interrupts and trigger eDMA channels. It also provides a dedicated Real-Time Interrupt (RTI) timer, which runs on a separate clock and can be used for system wake-up from low-power modes.

The PIT provides eleven programmable timers offering a range of functions. All of the timers are 24-bit wide down-counters. Once zero is reached, a trigger can be generated, then the counter is reloaded with the start value and continues to be decremented. The value of the decrementer can be read at any time. The eleven timers provide one Real Time Interrupt (RTI), four general purpose timers, four eDMA trigger timers, and two timers used to trigger ATD conversions.

4.14 Miscellaneous Control Module (MCM) and Cross-Bar Switch (XBS)

The Miscellaneous Control Module (MCM) provides several control functions for the MAC7100 family Standard Product Platform (SPP), including program-visible information regarding configuration and revision levels, a reset status register, a software watchdog timer, wake-up control for exiting sleep modes, the control registers for the crossbar switch, and generic access error information for the processor core.

The software watchdog timer (SWT) is contained within the MCM and supports either interrupt or reset generation on the occurrence of a time-out event. The SWT also supports a windowed time period, requiring the writing of the watchdog key within a specified time window. The source for the SWT clock is controlled by the clock and reset generator module (CRG).

The MCM also configures the crossbar switch (XBS) address map to steer access to the crossbar slave ports in order to provide remapping operations. Following reset, the mapping is determined by the chip mode entered. Following reset the Flash, external bus, and RAM can be remapped as necessary.

4.15 System Services Module (SSM)

The SSM contains information on device configuration and the status of the eDMA controller.

4.16 Voltage Regulator Module (VREG)

The voltage regulator (VREG) module provides the internal voltage for the on-chip logic, which enables devices in the MAC7100 family to be supplied with a single 5V power supply source. The VREG module is a dual output voltage regulator providing two 2.5 V (typical) supplies that differ in the amount of current that can be sourced by each. The regulator input voltage range is from 3.3 V up to 5 V. In low-power modes of operation the voltage regulator output can be reduced in order to further assist with power saving. The VREG can also be shut down by connecting the $V_{DD}R$ pin to $V_{SS}R$.

4.17 System Clocks (OSC and CRG)

The Pierce oscillator (OSC) coupled with the Clock and Reset Generator (CRG) provide the internal clock signals for the core and all peripheral modules. The system clock can be supplied to the MCU in several ways, enabling support for a range of system operating frequencies:

- From the oscillator, with a frequency set by an external, 16 MHz maximum, crystal reference
- From the on-chip phase-locked loop, using the oscillator clock as a reference
- From the PLL in self-clocking mode

The clock generated by the oscillator or the phase-locked loop (PLL) provides the main system clock frequency, f_{SYS}. The system clock is used throughout the device to drive the core and the memories. The IPS peripherals use a clock equal to $f_{SYS} \div 2$.

The program Flash memory is supplied by both f_{SYS} and $f_{SYS} \div 2$. f_{SYS} is used for access to the Flash controller, but the interleaved Flash arrays operate at half the system frequency to allow enough time to access the array, enabling the memory controller to achieve close to single-cycle access times.

The CAN modules may be configured to utilize either the peripheral clock ($f_{SYS} \div 2$) or the oscillator clock (OSCCLK). This allows the user to select the CAN clock based on the required jitter performance.

The Periodic Interrupt Timer (PIT) and Software Watchdog Timer (SWT) can be configured to run from the oscillator or the PLL generated clock. This allows these functions to continue to run during low-power operating modes if required.

4.18 Development Support

The MAC7100 family of devices offers debugging with the EmbeddedICE (E-ICE) and a NEXUS 2 Plus interface. EmbeddedICE offers debug features such as setting breakpoints or watchpoints, modifying and reading memory contents. EmbeddedICE uses the standard JTAG serial interface and Test Access Port (TAP) and is compatible with existing ARM tool chains. The NEXUS interface provides real-time program trace capability and also uses the JTAG port, while also providing an auxiliary port for additional debug capabilities. The auxiliary port can be provided in two pin positions depending on the device and package. In the 208 MAP BGA and 144 LQFP packages, it is possible for the NEXUS port to be available

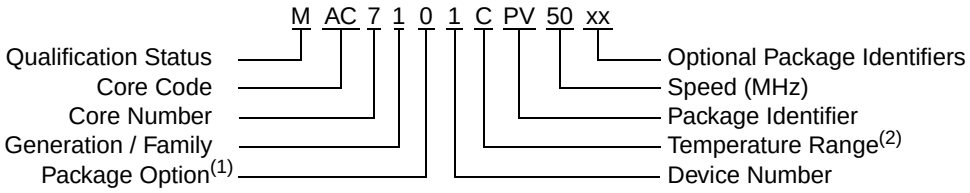
on either the low byte of Port A or the low byte of Port E. On smaller packages, the Nexus port is available only in the Port E position.

5 Documentation and Ordering

Table 2 lists the documents that provide a complete description of the MAC7100 microcontroller family and are required to design properly with devices in the family. Documentation is available from a local Freescale Semiconductor sales office or distributor, the Freescale Literature Distribution Center, or through the Freescale web site at http://www.freescale.com. Figure 2 shows an example orderable part number and description that is used to completely specify a MAC7100 family device.

Table 2. MAC7100 Family Documentation

Document Name	Order Number
MAC7100 Microcontroller Family Reference Manual	MAC7100RM
MAC7100 Hardware Specifications	MAC7100EC
ARM Architecture Reference Manual (Second Edition)	ARM DDI 0100E
ARM7TDMI-S (Rev 4) Technical Reference Manual (Issue A)	ARM DDI 0234A
LIN Specification 2.0	
CAN protocol specification, Version 2.0 B	



1. Package Option
FU = 100 LQFP
PV = 112 / 144 LQFP
VF = 208 MAP BGA

2. Temperature Option
C = –40°C to 85°C
V = –40°C to 105°C
M = –40°C to 125°C

Figure 2. Orderable Part Number Example

HOW TO REACH US:

USA/Europe/Locations not listed:
Freescale Semiconductor Literature Distribution
P.O. Box 5405, Denver, Colorado 80217
1-800-521-6274 or 480-768-2130

Japan:
Freescale Semiconductor Japan Ltd.
Technical Information Center
3-20-1, Minami-Azabu, Minato-ku
Tokyo 106-8573, Japan
81-3-3440-3569

Asia/Pacific:
Freescale Semiconductor H.K. Ltd.
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Tai Po, N.T. Hong Kong
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