

Kinetis KV1x Family Product Brief

ARM Cortex M0+, 75 MHz, Motor Control MCU with CAN

1 Introduction

The Kinetis KV1x family of microcontrollers is a cost-optimized solution specifically designed for motor control applications. Built upon the ARM® Cortex®-M0+ core running at 75 MHz, it is the fastest ARM Cortex-M0+ MCU in the market. With hardware square root and divide capability, it delivers a 27% increase in performance in math-intensive applications versus comparable MCUs, allowing it to target BLDC as well as more computationally demanding PMSM motors. Additional features include:

- 16 to 128 KB of flash memory and optional FlexCAN
- dual 16-bit analog-to-digital controllers with 835 ns conversion time in 12-bit mode
- Programmable delay block

Kinetis KV1x MCUs are offered in 64 LQFP, 48 LQFP, 32 LQFP and 32 QFN packages and comes with a comprehensive enablement suite from Freescale and third-parties that include reference designs, software solutions and tools making motor control simple.

2 Block diagram

The block diagram shows the features of the KV1x series MCU. Within each category, the diagram shows the superset of modules and number of module instances on the 64-pin member of the family.

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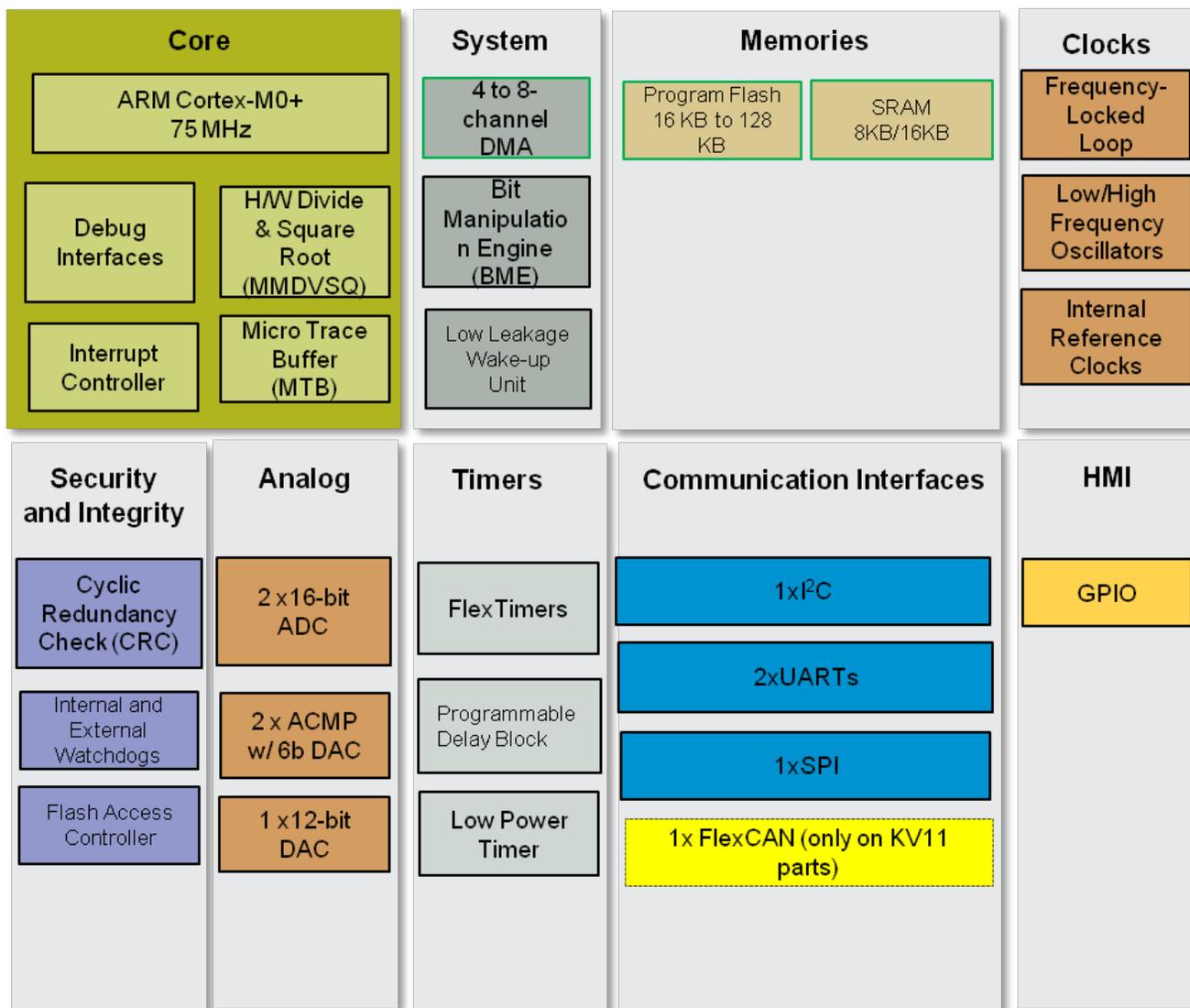


Figure 1. KV1x series block diagram

3 Features

3.1 KV1x High-Level Feature Comparison

Table 1. KV1x—75 MHz devices (16K to 128K)

Family	KV10				KV11	
	16 KB	32 KB	64KB	128 KB	64 KB	128 KB
Flash Memory	16 KB	32 KB	64KB	128 KB	64 KB	128 KB
CPU Frequency	75 MHz					
Hardware Square Root and Divide	Yes	Yes	Yes	Yes	Yes	Yes

Table continues on the next page...

Table 1. KV1x—75 MHz devices (16K to 128K) (continued)

Family	KV10				KV11	
	4-ch	4-ch	8-ch	8-ch	8-ch	8-ch
DMA	4-ch	4-ch	8-ch	8-ch	8-ch	8-ch
FLL	Yes	Yes	Yes	Yes	Yes	Yes
FlexTimers	1x6ch; 2x2ch	1x6ch; 2x2ch	Up to 2x6ch; 4x2ch	Up to 2x6ch; 4x2ch	Up to 2x6ch; 4x2ch	Up to 2x 6ch; 4x2ch
DAC	1x 12bit	1x 12bit	1x 12bit	1x 12bit	1x 12bit	1x 12bit
UARTS	2	2	2	2	2	2
I2C	1	1	1	1	1	1
DSPI	1	1	1	1	1	1
FlexCAN	0	0	0	0	1	1
64LQFP	No	No	Yes	Yes	Yes	Yes
48LQFP	Yes	Yes	Yes	Yes	Yes	Yes
32LQFP	Yes	Yes	Yes ¹	Yes ¹	Yes ¹	Yes ¹
32QFN	Yes	Yes	Yes	Yes	Yes	Yes

1. The 32-pin LQFP package supporting this part number is not yet available, however it is included in a Package Your Way program for Kinetis MCUs. Please visit <http://www.freescale.com/KPYW> for more details.

3.2 Common feature summary

The following table lists the features of the KV1x devices. The device features may vary by package.

Table 2. Common feature summary

Feature	Details
Hardware characteristics	
Packages	64-pin LQFP (10 x 10 x 1.4) 48-pin LQFP (7 x 7 x 1.4) 32-pin LQFP (7 x 7 x 1.4) 32-pin QFN (5 x 5 x 1.23)
Voltage range	1.71 V to 3.6 V
Temperature range (T _A)	-40 °C to 105 °C
Temperature range (T _J)	-40 °C to 125 °C
System	
Central processing unit (CPU)	ARM Cortex M0+
Max. CPU frequency	75 MHz
32-bit integer divide and square root arithmetic module	Yes
Nested vectored interrupt controller (NVIC)	32
Direct memory access (DMA)	4/8 channels
DMA request multiplex	64 sources
Non-maskable interrupt (NMI)	Yes
Software watchdog (iWDOG)	Independent clock source with windowed mode

Table continues on the next page...

Table 2. Common feature summary (continued)

Feature	Details
External Watchdog Monitor	Yes with independent clock source
Debug	2-pin serial wire debug (SWD)
Trace	Data watchpoint and trace (DWT)
Boundary scan	No boundary scan, no JTAG
Unique identification (ID) number	128-bit wide
Memory	
Flash memory	16 to 128 KB
Random-access memory (RAM)	8 or 16 KB
Cyclic redundancy check (CRC)	16- or 32-bit CRC with programmable generator polynomial
Clocks	
External crystal oscillator or resonator	Low range, low power or full-swing: 32 - 40 kHz High range, low power or full-swing: 4 - 20 MHz
External square wave input clock	DC to 20 MHz
Internal clock references	4M Hz IRC 32 kHz IRC 1 kHz LPO
Frequency-locked loop (FLL)	Range: 8 - 75 MHz
Human-machine interface (HMI)	
General-purpose input/output (GPIO)	3 V I/O Pin interrupt / DMA request capability Digital glitch filter on all input pins Configurable pull up device on all input pins
Analog	
Power management controller (PMC)	Low voltage warning and detect with selectable trip points
16-bit analog-to-digital converter (ADC)	2 x 16-bit SAR ADC Upto 15/18 channels single-ended/2 sets of differential inputs, with dual acquisition/result registers. 835 ns conversion time in 12-bit mode
High-speed comparator (HSCMP) with internal 6-bit digital-to-analog converter (DAC)	2
12 bit DAC	1
Timers	
Motor Control Timer	One/two 6-channel FlexTimer
Additional timers	Two/four 2-channel FlexTimer with quadrature decoding
Programmable delay block (PDB)	One/Two PDB with 15 inputs supporting multiple pulse to two ADCs
LPTimer	Low power timer wakes up CPU from low power modes
Communication interfaces	
Serial peripheral interface (DSPI)	One with four word FIFO
Inter-integrated circuit (I ² C)	One with SMBUS support

Table continues on the next page...

Table 2. Common feature summary (continued)

Feature	Details
Flexible Serial Communications Interface (FlexSCI)	Two SCIs
FlexCAN	One FlexCAN ¹

1. Available only in KV11 parts

3.3 Orderable part numbers

The following table summarizes the part numbers of the devices covered by this document.

Table 3. Orderable part numbers summary

Freescall part number	CPU frequency	Pin count	Package	Total flash memory	FlexCAN	SRAM	GPIO
MKV11Z128VLH7	75 MHz	64	LQFP	128 KB	Yes	16 KB	54
MKV11Z128VLF7	75 MHz	48	LQFP	128 KB	Yes	16 KB	40
MKV11Z128VLC7	75 MHz	32	LQFP	128 KB	Yes	16 KB	28
MKV11Z128VFM7	75 MHz	32	QFN	128 KB	Yes	16 KB	28
MKV11Z64VLH7	75 MHz	64	LQFP	64 KB	Yes	16 KB	54
MKV11Z64VLF7	75 MHz	48	LQFP	64 KB	Yes	16 KB	40
MKV11Z64VLC7 ¹	75 MHz	32	LQFP	64 KB	Yes	16 KB	28
MKV11Z64VFM7	75 MHz	32	QFN	64 KB	Yes	16 KB	28
MKV10Z64VLH7	75 MHz	64	QFP	64 KB	No	16 KB	28
MKV10Z64VLF7	75 MHz	48	QFP	64 KB	No	16 KB	28
MKV10Z64VLC7 ¹	75 MHz	32	LQFP	64 KB	No	16 KB	28
MKV11Z64VFM7	75 MHz	32	QFN	64 KB	No	16 KB	28
MKV10Z128VLH7	75 MHz	64	QFP	128 KB	No	16 KB	54
MKV10Z128VLF7	75 MHz	48	QFP	128 KB	No	16 KB	40
MKV10Z128VLC7 ¹	75 MHz	32	LQFP	128 KB	No	16 KB	28
MKV10Z128VFM7	75 MHz	32	QFN	128 KB	No	16 KB	28
MKV10Z16VFM7	75 MHz	32	QFP	16 KB	No	8 KB	28
MKV10Z16VLC7	75 MHz	32	QFP	16 KB	No	8 KB	28
MKV10Z16VLF7	75 MHz	48	QFP	16 KB	No	8 KB	40
MKV10Z32VFM7	75 MHz	32	QFP	32 KB	No	8 KB	28
MKV10Z32VLC7	75 MHz	32	QFP	32 KB	No	8 KB	28
MKV10Z32VLF7	75 MHz	48	QFP	32 KB	No	8 KB	40

1. The 32-pin LQFP package supporting this part number is not yet available, however it is included in a Package Your Way program for Kinetis MCUs. Please visit <http://www.freescale.com/KPYW> for more details

3.4 Module-by-module feature list

3.4.1 Core Modules

3.4.1.1 ARM Cortex-M0+ Core

- Supports up to 75MHz frequency
- Support up to 32 interrupt request sources
- 2-stage pipeline microarchitecture for reduced power consumption and improved architectural performance (cycles per instruction)
- Decorated Memory Controller for improved bit handling of peripheral modules
- Binary compatible instruction set architecture with the CM0 core
- Thumb instruction set combines high code density with 32-bit performance
- Serial Wire Debug (SWD) reduces the number of pins required for debugging
- Basic Branch Buffer (BBB) provides lightweight program trace capabilities using system RAM as the destination memory
- ARMv6M architecture based all features/ISA present in Cortex-M0 to be preserved
- Microcontroller cores focused on very cost sensitive, deterministic, interrupt driven environments
- Configurable nested vectored interrupt controller (NVIC)

3.4.1.2 Nested Vectored Interrupt Controller (NVIC)

- Up to 32 interrupt sources
- Includes a single nonmaskable interrupt

3.4.1.3 Wake-Up Interrupt Controller (WIC)

- Supports interrupt handling when system clocking is disabled in low-power modes
- Takes over and emulates the NVIC behavior when correctly primed by the NVIC on entry to Very-Deep-Sleep mode
- A rudimentary interrupt masking system with no prioritization logic signals for wake-up as soon as a nonmasked interrupt is detected.
- Contains no programmer's model visible state and is therefore invisible to end users of the device other than through the benefits of reduced power consumption while sleeping

3.4.1.4 Debug Controller

- Serial Wire JTAG Debug Port (SWJ-DP) combines
 - external interface that provides a serial-wire bidirectional debug interface

3.4.2 Memory

3.4.2.1 On-Chip Memory

- Up to 128 KB program flash memory

- Up to 16 KB SRAM
- Security circuitry to prevent unauthorized access to RAM and flash contents

3.4.2.2 Cyclic Redundancy Check (CRC)

- Hardware CRC generator circuit using 16/32-bit shift register
- User Configurable 16/32 bit CRC
- Programmable Generator Polynomial
- Error detection for all single, double, odd, and most multi-bit errors
- Programmable initial seed value
- High-speed CRC calculation
- Optional feature to transpose input data and CRC result via transpose register, required on applications where bytes are in lsb format

3.4.3 Human-machine interface

3.4.3.1 General Purpose Input/Output (GPIO)

- Programmable glitch filter and interrupt with selectable polarity on all input pins
- Hysteresis and configurable pull up/down device on all input pins

3.4.4 Analog

3.4.4.1 16-bit Analog-to-Digital Converter (ADC)

- 835 ns conversion in 12-bit mode, 1.1 μ s conversion in 16-bit mode.
- Linear successive approximation algorithm with up to 16-bit resolution
- Output modes:
 - Differential 16-bit, 13-bit, 11-bit, and 9-bit modes, in two's complement 16-bit sign-extended format
 - Single-ended 16-bit, 12-bit, 10-bit, and 8-bit modes, in right-justified unsigned format
- Single or continuous conversion
- Configurable sample time and conversion speed/power
- Conversion complete and hardware average complete flag and interrupt
- Input clock selectable from up to four sources
- Operation in low power modes for lower noise operation
- Dual acquisition mode with two result registers.
- Asynchronous clock source for lower noise operation with option to output the clock
- Selectable asynchronous hardware conversion trigger with hardware channel select
- Automatic compare with interrupt for various programmable values
- Temperature sensor
- Hardware average function
- Selectable voltage reference
- Self-calibration mode

3.4.4.2 High-Speed Analog Comparator (CMP)

- Up to six selectable comparator inputs; each input can be compared with any input by any polarity sequence
- Selectable interrupt on rising edge, falling edge, or either rising or falling edges of comparator output

- Comparator output may be sampled, windowed (ideal for zero cross detection) or digitally filtered
- Remains operational in low power mode
- Internal 6-bit DAC programmable reference on 4th input

3.4.4.3 6-bit digital-to-analog converter (DAC)

- On-chip programmable reference generator output
- Typically 5 mV of input offset
- Less than 40 μ A power consumption in enable mode and less than 1 nA in disable mode (excluding programmable reference generator)
- Fixed ACMP hysteresis from 3 mV to 20 mV
- Up to eight selectable comparator inputs; each input can be compared with any input by any polarity sequence
- Selectable interrupt on rising edge, falling edge, or either rising or falling edges of comparator output
- Remains operational in low power mode

3.4.4.4 12-bit Digital-to-Analog Converter

- 12-bit resolution
- Powerdown mode
- Automatic mode allows the DAC to automatically generate pre-programmed output waveforms, including square, triangle, and sawtooth waveforms (for applications like slope compensation)
- Programmable period, update rate, and range
- Output can be routed to an internal comparator, ADC, or optionally to an off-chip destination

3.4.5 Timers

3.4.5.1 FlexTimers (FTM)

- Upto 2x 6-channel FlexTimers
- Selectable FTM source clock
- Programmable prescaler
- 16-bit counter supporting free-running or initial/final value, and counting is up or up-down
- Input capture, output compare, and edge-aligned and center-aligned PWM modes
- Input capture and output compare modes
- Operation of FTM channels as pairs with equal outputs, pairs with complimentary outputs, or independent channels with independent outputs
- Deadtime insertion is available for each complementary pair
- Generation of hardware triggers
- Software control of PWM outputs
- Configurable channel polarity
- Programmable interrupt on input capture, reference compare, overflowed counter, or detected fault condition
- Quadrature decoder with input filters, relative position counting, and interrupt on position count or capture of position count on external event
- DMA support for FTM events
- Global time base mode shares single time base across multiple FTM instances

3.4.5.2 FlexTimers (FTM)

- Upto 4 x 2-channel FlexTimer
- Selectable FTM source clock
- Programmable prescaler

- 16-bit counter supporting free-running or initial/final value, and counting is up or up-down
- Input capture, output compare, and edge-aligned and center-aligned PWM modes
- Input capture and output compare modes
- Operation of FTM channels as pairs with equal outputs, pairs with complimentary outputs, or independent channels with independent outputs
- Deadtime insertion is available for each complementary pair
- Generation of hardware triggers
- Software control of PWM outputs
- Configurable channel polarity
- Programmable interrupt on input capture, reference compare, overflowed counter, or detected fault condition
- Quadrature decoder with input filters, relative position counting, and interrupt on position count or capture of position count on external event
- Hall Sensor speed/position support via ORing of 3 input capture pins to one channel - NEW feature.
- Modulation mode support - New feature.
- DMA support for FTM events
- Global time base mode shares single time base across multiple FTM instances

3.4.5.3 Programmable Delay Block (PDB)

- Upto two PDBs
- Up to 15 trigger input sources and software trigger source
- PDB channel for ADC hardware trigger
 - One PDB channel is associated with two ADCs.
 - One trigger output for ADC hardware trigger and up to four pre-trigger outputs for ADC trigger select per PDB channel
 - Trigger outputs can be enabled or disabled independently.
 - One 16-bit delay register per pre-trigger output
 - Optional bypass of the delay registers of the pre-trigger outputs
 - Operation in One-Shot or Continuous modes
 - One programmable delay interrupt
 - One sequence error interrupt
 - One channel flag and one sequence error flag per pre-trigger
 - DMA support
- pulse output (pulse-out's)
 - Pulse-out's can be enabled or disabled independently.
 - Programmable pulse width

3.4.5.4 Watchdog Timer (WDOG)

- Independent, configurable clock source input
- Write-once control bits with unlock sequence
- Programmable timeout period
- Ability to test watchdog timer and reset
- Windowed refresh option
- Robust refresh mechanism
- Cumulative count of watchdog resets between power-on resets
- Configurable interrupt on timeout

3.4.5.5 External Watchdog Monitor (EWM)

- Independent 1 kHz LPO clock source
- Output signal to gate an external circuit which is controlled by CPU service or external input

3.4.5.6 Low-Power Timer (LPTimer)

- Operation as timer or pulse counter
- Selectable clock for prescaler/glitch filter
- 1 kHz internal LPO
- External low power crystal oscillator
- Internal reference clock (not available in low leakage power modes)
- Configurable glitch filter or prescaler
- Interrupt generated on timer compare
- Hardware trigger generated on timer compare

3.4.6 Communication interfaces

3.4.6.1 Serial Peripheral Interface (SPI)

- Master and slave mode
- Full-duplex, three-wire synchronous transfers
- Programmable transmit bit rate
- Double-buffered transmit and receive data registers
- Serial clock phase and polarity options
- Slave select output
- Mode fault error flag with CPU interrupt capability
- Control of SPI operation during wait mode
- Selectable MSB-first or LSB-first shifting
- Programmable 8-bit or 16-bit data transmission length
- Receive data buffer hardware match feature
- 64-bit FIFO mode for high speed transfers of large amounts of data
- Support for both transmit and receive by DMA

3.4.6.2 UART

- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format
- 13-bit baud rate selection with fractional divide of 32
- Programmable 8-bit or 9-bit data format
- Separately enabled transmitter and receiver
- Programmable transmitter output polarity
- Programmable receive input polarity
- 13-bit break character option
- 11-bit break character detection option
- Parameterizable buffer support for one dataword for each transmit and receive
- Independent FIFO structure for transmit and receive
- Two receiver wakeup methods:
 - Idle line wakeup
 - Address mark wakeup
- Address match feature in receiver to reduce address mark wakeup ISR overhead
- Hardware flow control support for request to send (RTS) and clear to send (CTS) signals
- Interrupt or DMA driven operation
- Receiver framing error detection
- Hardware parity generation and checking
- 1/16 bit-time noise detection

3.4.6.3 Flex Controller Area Network (FlexCAN) module

- Implementation of CAN protocol Version 2.0 A/B
- Standard and extended data frames
- Data length of 0 to 8 bytes
- Programmable bit rate up to 1 Mbps
- Support for remote frames
- Sixteen Message Buffers: each Message Buffer can be configured as receive or transmit, and supports standard and extended messages
- Individual Rx Mask Registers per Message Buffer
- Internal timer for time-stamping of received and transmitted messages
- Listen-only mode capability
- Programmable loopback mode, supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number, or highest priority
- Global network time, synchronized by a specific message
- Low power modes, with programmable wakeup on bus activity

3.4.6.4 Inter-Integrated Circuit (I²C)

- Compatible with I²C bus standard and SMBus version 2 features
- Up to 100 kbps with maximum bus loading, 400kbps supported with limited bus loading
- Multi-master operation
- Software programmable for one of 64 different serial clock frequencies
- Programmable slave address and glitch input filter
- Interrupt driven byte-by-byte data transfer
- Arbitration lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Bus busy detection broadcast and 10-bit address extension
- Address matching causes wake-up when processor is in low power mode
- DMA support

4 Part identification

4.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

4.2 Format

Part numbers for this device have the following format:

Q KV## M FFF R T PP CC N

4.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Part identification

Field	Description	Values
Q	Qualification status	<ul style="list-style-type: none"> • M = Fully qualified, general market flow • P = Prequalification
KV##	Kinetis family	<ul style="list-style-type: none"> • KV10 and KV11
M	Key attribute	<ul style="list-style-type: none"> • Z = M0+ core
FFF	Program flash memory size	<ul style="list-style-type: none"> • 128 = 128 KB
T	Temperature range (°C)	<ul style="list-style-type: none"> • V = -40 to 105
PP	Package identifier	<ul style="list-style-type: none"> • LC = 32 LQFP (7 mm x 7 mm) • FM = 32 QFN (5 mm x 5 mm) • LF = 48 LQFP (7 mm x 7 mm) • LH = 64 LQFP (10 mm x 10 mm)
CCC	Maximum CPU frequency (MHz)	<ul style="list-style-type: none"> • 7 = 75 MHz
N	Packaging type	<ul style="list-style-type: none"> • R = Tape and reel • (Blank) = Trays

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