

SOT2003-1

FOWLP249, fan-out wafer-level package, 249 terminals, 0.4 mm pitch, 7 mm x 7 mm x 0.725 mm body

15 September 2020

Package information

1 Package summary

Terminal position code	B (bottom)
Package type descriptive code	FOWLP249
Package style descriptive code	FOWLP (fan-out wafer-level package)
Mounting method type	S (surface mount)
Issue date	17-06-2020
Manufacturer package code	98ASA01357D

Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	6.95	7	7.05	mm
package width	6.95	7	7.05	mm
seated height	-	0.725	0.76	mm
nominal pitch	-	0.4	-	mm
actual quantity of termination	-	249	-	



FOWLP249, fan-out wafer-level package, 249 terminals, 0.4 mm pitch, 7 mm x 7 mm x 0.725 mm body

2 Package outline

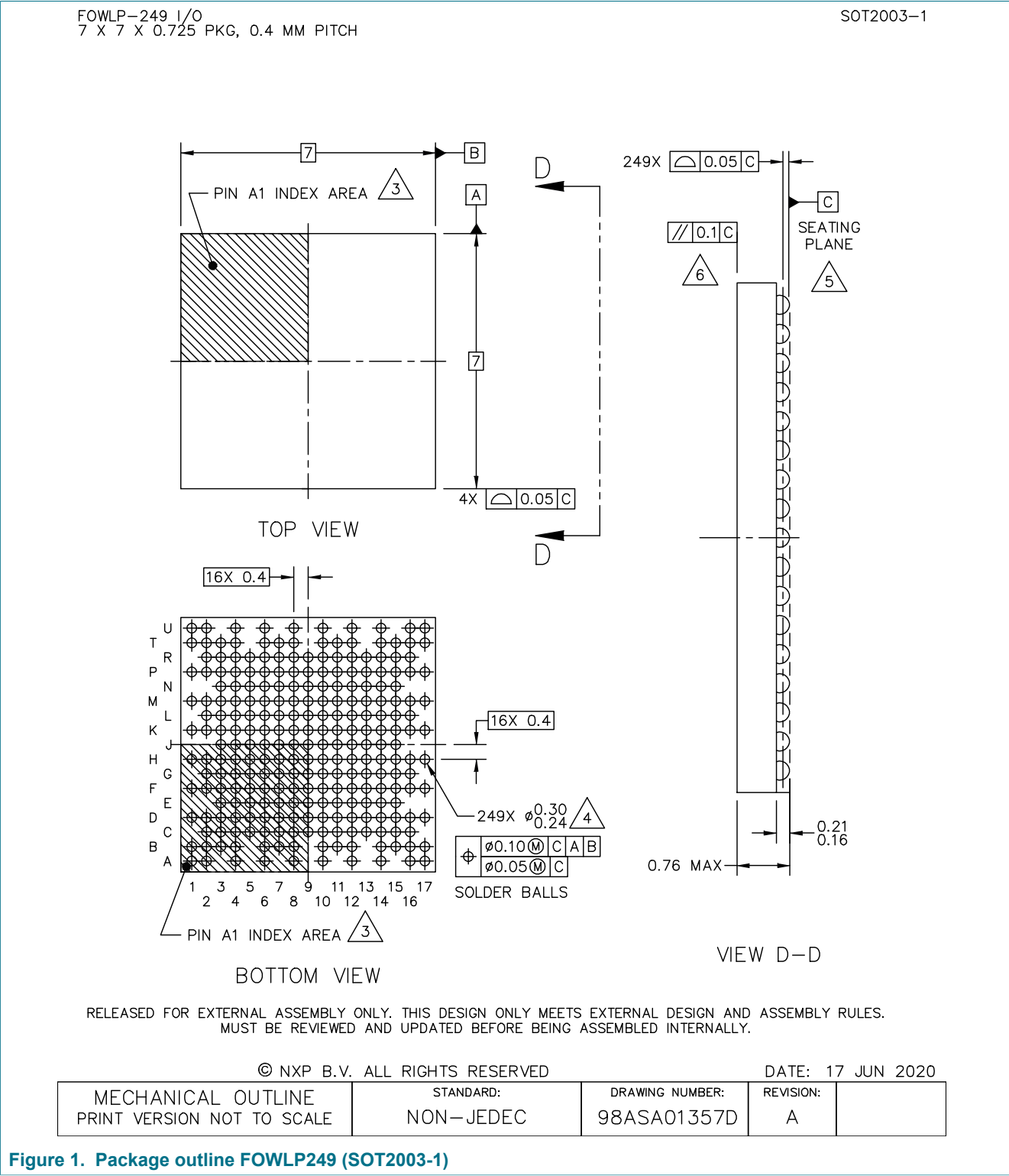
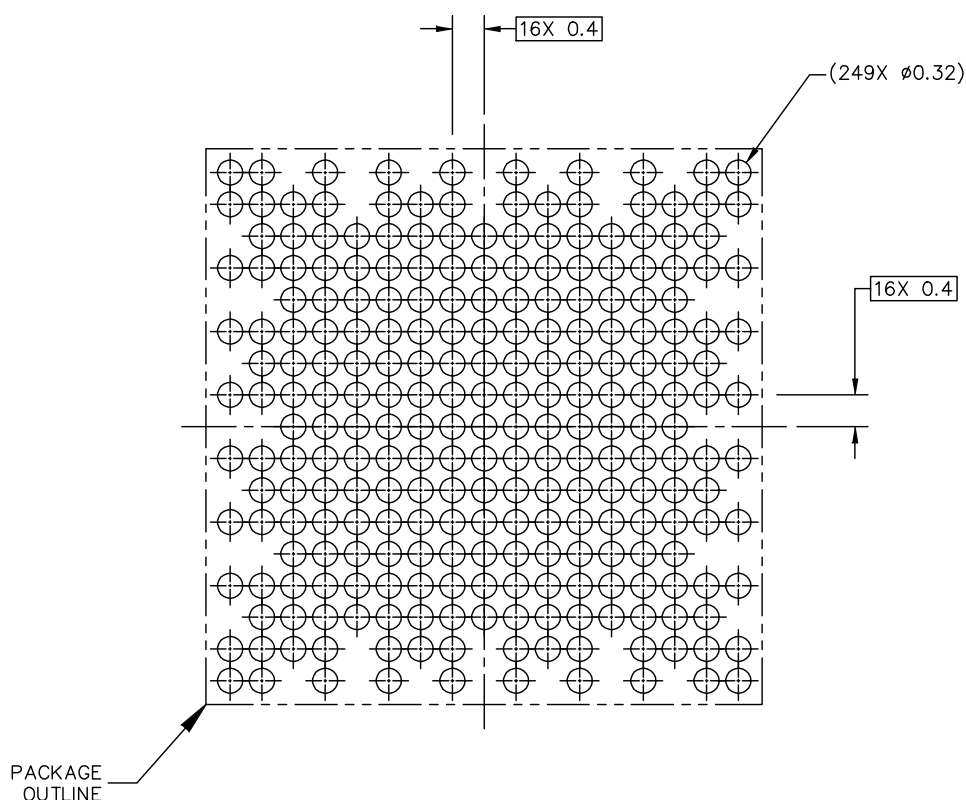


Figure 1. Package outline FOWLP249 (SOT2003-1)

3 Soldering

FOWLP-249 I/O
7 X 7 X 0.725 PKG, 0.4 MM PITCH

SOT2003-1



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

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PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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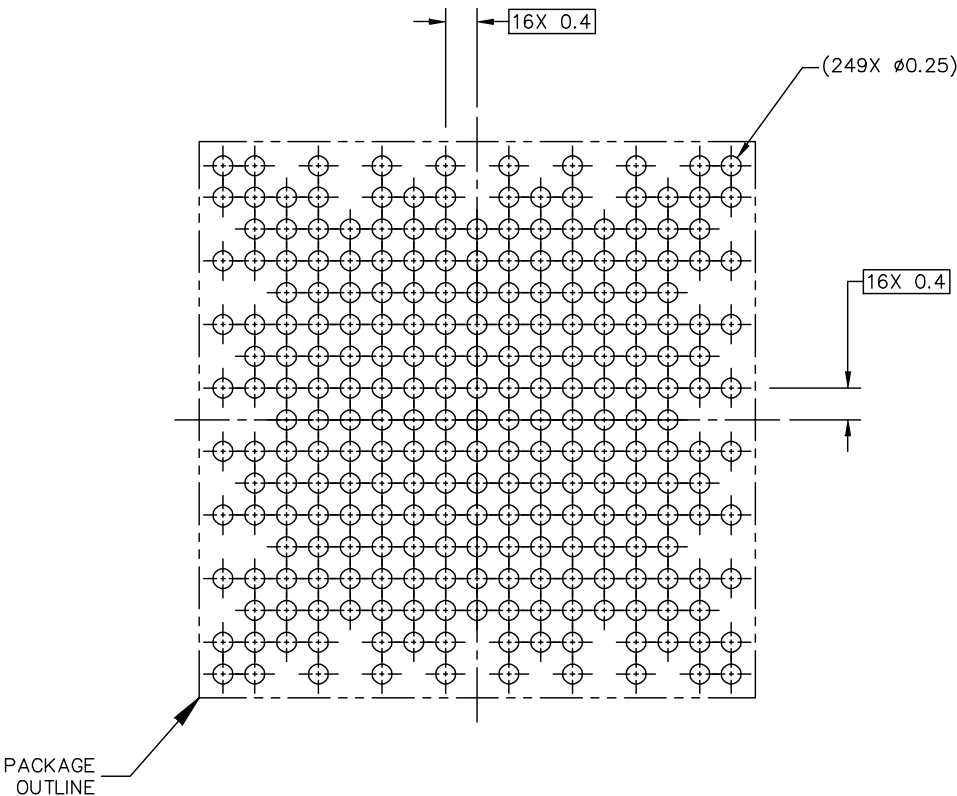
MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON-JEDEC	DRAWING NUMBER: 98ASA01357D	REVISION: A
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Figure 2. Reflow soldering footprint part1 for FOWLP249 (SOT2003-1)

FOWLP249, fan-out wafer-level package, 249 terminals, 0.4 mm pitch, 7 mm x 7 mm x 0.725 mm body

FOWLP-249 I/O
7 X 7 X 0.725 PKG, 0.4 MM PITCH

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PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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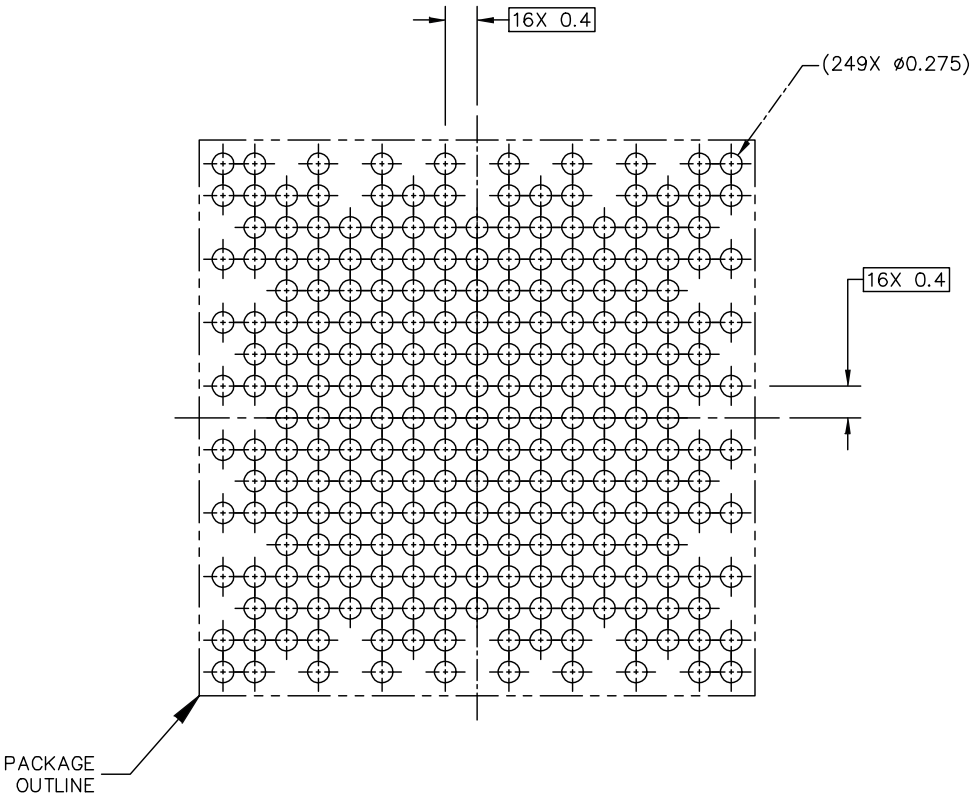
MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON-JEDEC	DRAWING NUMBER: 98ASA01357D	REVISION: A	
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Figure 3. Reflow soldering footprint part2 for FOWLP249 (SOT2003-1)

FOWLP249, fan-out wafer-level package, 249 terminals, 0.4 mm pitch, 7 mm x 7 mm x 0.725 mm body

FOWLP-249 I/O
7 X 7 X 0.725 PKG, 0.4 MM PITCH

SOT2003-1



RECOMMENDED STENCIL THICKNESS 0.1

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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Figure 4. Reflow soldering footprint part3 for FOWLP249 (SOT2003-1)

FOWLP249, fan-out wafer-level package, 249 terminals, 0.4 mm pitch, 7 mm x 7 mm x 0.725 mm body

FOWLP-249 I/O
7 X 7 X 0.725 PKG, 0.4 MM PITCH

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NOTES:

- 1. ALL DIMENSIONS IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- 3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
- 4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
- 5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
- 6. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

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Figure 5. Package outline note FOWLP249 (SOT2003-1)

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FOWLP249, fan-out wafer-level package, 249 terminals, 0.4 mm pitch, 7 mm x 7 mm x 0.725 mm body

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