



MPC850 PBGA PIN ASSIGNMENT

(C) 1998 Motorola

PIN	NAME	PIN	NAME
A1	VSSSYN	B1	VDDSYN
A2	VSSSYN1	B2	XFC
A3	KAPWR	B3	<u>PORESET</u>
A4	XTAL	B4	<u>SRESET</u>
A5	EXTAL	B5	HRESET
A6	EXTCLK	B6	OP3/MODCK2/DSDO
A7	VDDL	B7	KR/IRQ4/SPKROUT
A8	IP_B0/IWP0/VFLS0	B8	ALE_B/DSCK/AT1
A9	IP_B3/IWP2/VF2	B9	IP_B4/LWP0/VF0
A10	FRZ/ <u>IRQ6</u>	B10	<u>BURST</u>
A11	<u>BB</u>	B11	<u>BR</u>
A12	<u>TA</u>	B12	<u>BI</u>
A13	<u>BDIP/GPL_B5</u>	B13	UPWAITB/ <u>GPL_B4</u>
A14	<u>CS1</u>	B14	<u>CS2</u>
A15	<u>CS3</u>	B15	<u>CS7/CE2_B</u>
A16	NC	B16	<u>CS4</u>
C1	NC	D1	CLKOUT
C2	DP3/ <u>IRQ6</u>	D2	D30
C3	DP0/ <u>IRQ3</u>	D3	DP2/ <u>IRQ5</u>
C4	<u>WAIT_B</u>	D4	DP1/ <u>IRQ4</u>
C5	<u>RSTCONF</u>	D5	TEXP
C6	NC	D6	OP2/MODCK1/ <u>STS</u>
C7	IP_B6/DSDI/AT0	D7	IP_B2/ <u>IOIS16_B/AT2</u>
C8	IP_B1/IWP1/VFLS1	D8	IP_B7/ <u>PTR/AT3</u>
C9	IP_B5/LWP1/VF1	D9	<u>IRQ2/RSV</u>
C10	<u>BG</u>	D10	<u>TS</u>
C11	<u>TEA</u>	D11	UPWAITA/ <u>GPL_A4/AS</u>
C12	<u>GPL_A5</u>	D12	<u>CS0</u>
C13	<u>RD/WR</u>	D13	<u>CS5</u>
C14	<u>CS6/CE1_B</u>	D14	<u>GPL_A3/GPL_B3</u>
C15	<u>GPL_A2/GPL_B2</u>	D15	<u>WE2/BS_AB2/PCOE</u>
C16	<u>OE/GPL_A1/GPL_B1</u>	D16	<u>WE0/BS_AB0/IORD</u>



<u>PIN</u>	<u>NAME</u>	<u>PIN</u>	<u>NAME</u>
E1	D7	F1	D6
E2	D29	F2	D21
E3	D31	F3	D24
E4	D26	F4	D28
E5	VDDH	F5	VDDH
E6	VDDH	F6	GND
E7	VDDH	F7	GND
E8	VDDH	F8	GND
E9	VDDH	F9	GND
E10	VDDH	F10	GND
E11	VDDH	F11	GND
E12	VDDH	F12	VDDH
E13	GPL_A0/GPL_B0	F13	WE3/BS_AB3/PCWE
E14	NC	F14	A26
E15	TSIZ1	F15	TSIZ0/REG
E16	WE1/BS_AB1/IOWR	F16	A31
G1	VDDL	H1	D5
G2	D19	H2	D16
G3	D20	H3	D18
G4	D25	H4	D22
G5	VDDH	H5	VDDH
G6	GND	H6	GND
G7	GND	H7	GND
G8	GND	H8	GND
G9	GND	H9	GND
G10	GND	H10	GND
G11	GND	H11	GND
G12	VDDH	H12	VDDH
G13	A18	H13	A24
G14	A22	H14	A25
G15	A30	H15	A23
G16	A28	H16	A29
J1	D3	K1	D11
J2	D2	K2	D9
J3	D14	K3	D10
J4	D15	K4	D17
J5	VDDH	K5	VDDH
J6	GND	K6	GND
J7	GND	K7	GND
J8	GND	K8	GND
J9	GND	K9	GND
J10	GND	K10	GND
J11	GND	K11	GND
J12	VDDH	K12	VDDH
J13	NC	K13	A17
J14	A21	K14	A16
J15	A20	K15	A19
J16	VDDL	K16	A27

<u>PIN</u>	<u>NAME</u>	<u>PIN</u>	<u>NAME</u>
L1	D1	M1	D0
L2	D4	M2	D8
L3	D27	M3	D13
L4	D23	M4	D12
L5	VDDH	M5	VDDH
L6	GND	M6	VDDH
L7	GND	M7	VDDH
L8	GND	M8	VDDH
L9	GND	M9	VDDH
L10	GND	M10	VDDH
L11	GND	M11	VDDH
L12	VDDH	M12	VDDH
L13	A10	M13	A6
L14	A13	M14	A12
L15	A14	M15	A9
L16	A15	M16	A11
N1	<u>IRQ0</u>	P1	NC
N2	<u>IRQ1</u>	P2	PD[5]/UTPB[6]
N3	<u>IRQ7</u>	P3	PD[4]/UTPB[7]
N4	PD[3]/SOC	P4	PD[9]/UTPCLK
N5	PD[11]/RXENB	P5	PD[13]/UTPB[2]
N6	PC[6]/USBTXN	P6	PC[5]/L1TSYNCA/ <u>SDACK1/CTS3</u>
N7	PB[17]/L1ST3	P7	PB[18]/ <u>RTS2/L1ST2</u>
N8	PC[8]/ <u>CD2/TGATE1</u>	P8	PA[6]/CLK2/ <u>TOUT1/TIN3</u>
N9	NC	P9	PC[10]/ <u>TGATE1/USBRXN</u>
N10	PA[9]/L1TXDA/SMRXD2	P10	NC
N11	PB[25]/SMTXD1/TXD3	P11	<u>TRST</u>
N12	TDO/DSDO	P12	PB[26]/I2CSCL/BRGO2
N13	NC	P13	PC[13]/L1ST7/ <u>RTS3</u>
N14	PB[31]/ <u>SPISEL</u>	P14	PB[29]/SPIMOSI/RXD3
N15	A7	P15	PB[30]/SPICLK/TXD3
N16	A8	P16	PA[15]/USBRXD
R1	PD[6]/UTPB[5]	T1	PD[8]
R2	PD[7]/UTPB[4]	T2	PD[10]/TXENB
R3	PD[12]/UTPB[3]	T3	PD[14]/UTPB[1]
R4	PD[15]/UTPB[0]	T4	PC[4]/L1RSYNCA/ <u>CD3</u>
R5	PB[16]/L1RQA/L1ST4	T5	PC[7]/USBTXP
R6	PA[4]/CLK4/ <u>TOUT2/TIN4</u>	T6	PA[5]/CLK3/BRGO2/L1TCLKA/TIN2
R7	PB[19]/L1ST1	T7	VDDL
R8	PC[9]/ <u>CTS2</u>	T8	PA[7]/CLK1/BRGO1/L1RCLKA/TIN1
R9	PB[22]/ <u>SDACK2/SMSYN2</u>	T9	PA[8]/L1RXDA/SMTXD2
R10	PC[11]/USBRXP	T10	PB[23]/ <u>SDACK1/SMSYN1</u>
R11	TDI/DSDI	T11	PB[24]/SMRXD1/RXD3
R12	TMS	T12	TCK/DSCK
R13	PA[12]/TXD2	T13	PC[12]/TXCAV/L1RQA/L1ST8
R14	PA[13]/RXD2	T14	PB[27]/I2CSDA/BRGO1
R15	PA[14]/ <u>USBOE</u>	T15	PB[28]/SPIMISO/BRGO3
R16	PC[15]/RXCAV/ <u>DREQ1/L1ST5</u>	T16	PC[14]/ <u>DREQ2/RTS2/L1ST6</u>